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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, I²S, PWM
Number of I/O	85
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 20x12b
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m0564vg4ae

1 GENERAL DESCRIPTION

The NuMicro® M0564 series microcontroller based on the ARM® Cortex®-M0 core operates at up to 72 MHz. It features adjustable V_{DDIO} pins for specific I/O pins with a wide range of voltage from 1.8V to 5.5V for various operating voltages of external components, a unique high-speed PWM with clock frequency up to 144 MHz for precision control, and an integrated hardware divider to speed up the calculation for the control algorithms. Apart from that, the M0564 also integrates SPROM (Security Protection ROM) which provides a secure code execution area to protect the intelligent property of developers. The M0564 series is ideal for industrial control, motor control and metering applications.

The M0564 series supports the wide voltage range from 2.5V to 5.5V and temperature ranging from -40℃ to 105℃, up to 256 Kbytes of Flash memory, 20 Kbytes of SRAM , 4 Kbytes of ISP (In-System Programming) ROM as well as ICP (In-Circuit Programming) ROM and IAP (In-Application Programming) ROM in 48-, 64- or 100-pin packages. It also supports high immunity of 8KV ESD (HBM)/4KV EFT. It is also equipped with plenty of peripherals such as Timers, Watchdog Timers, RTC, PDMA, EBI, UART, Smart Card Interface, SPI, I²S, I²C, GPIO, up to 12 channels of 16-bit PWM, up to 20 channels of 12-bit ADC, analog comparator, temperature sensor, LVR (Low Voltage Reset), BOD (Brown-out Detector), 96-bit UID (Unique Identification), and 128-bit UCID (Unique Customer Identification).

- Packages
  - All Green package (RoHS)
  - LQFP 100-pin
  - LQFP 64-pin(7mmx7mm)
  - LQFP 48-pin

4.1.2 NuMicro® M0564 Base Series (M051 Compatible) Selection Guide

Part Number	Flash (KB)	SRAM (KB)	Data Flash(KB)	SPROM(KB)	ISP ROM (KB)	I/O	Timer/PWM	PWM	Connectivity					ADC(12-Bit)	ACMP	PDMA	VBAT(RTC)	LVIO	EBI	ICP/IAP/ISP	Package
									USCI*	UART	SC/UART	SPI/I^2S	I^2C								
M0564LE4AE	128	20	**Conf***	2	4	41	4	12	3	3	2	2	2	10-ch	2	5	--	√	√	√	LQFP48
M0564LG4AE	256	20	**Conf***	2	4	41	4	12	3	3	2	2	2	10-ch	2	5	--	√	√	√	LQFP48
M0564SE4AE	128	20	**Conf***	2	4	53	4	12	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP64*
M0564SG4AE	256	20	**Conf***	2	4	53	4	12	3	3	2	2	2	15-ch	2	5	√	√	√	√	LQFP64*
M0564VG4AE	256	20	**Conf***	2	4	85	4	12	3	3	2	2	2	20-ch	2	5	√	√	√	√	LQFP100

Conf*: Configurable
USCI*: support UART, SPI or I^2C
LQFP64*: 7x7 mm

4.2.3 NuMicro® M0564 Base Series LQFP100 Pin Diagram

Corresponding Part Number: M0564VG4AE

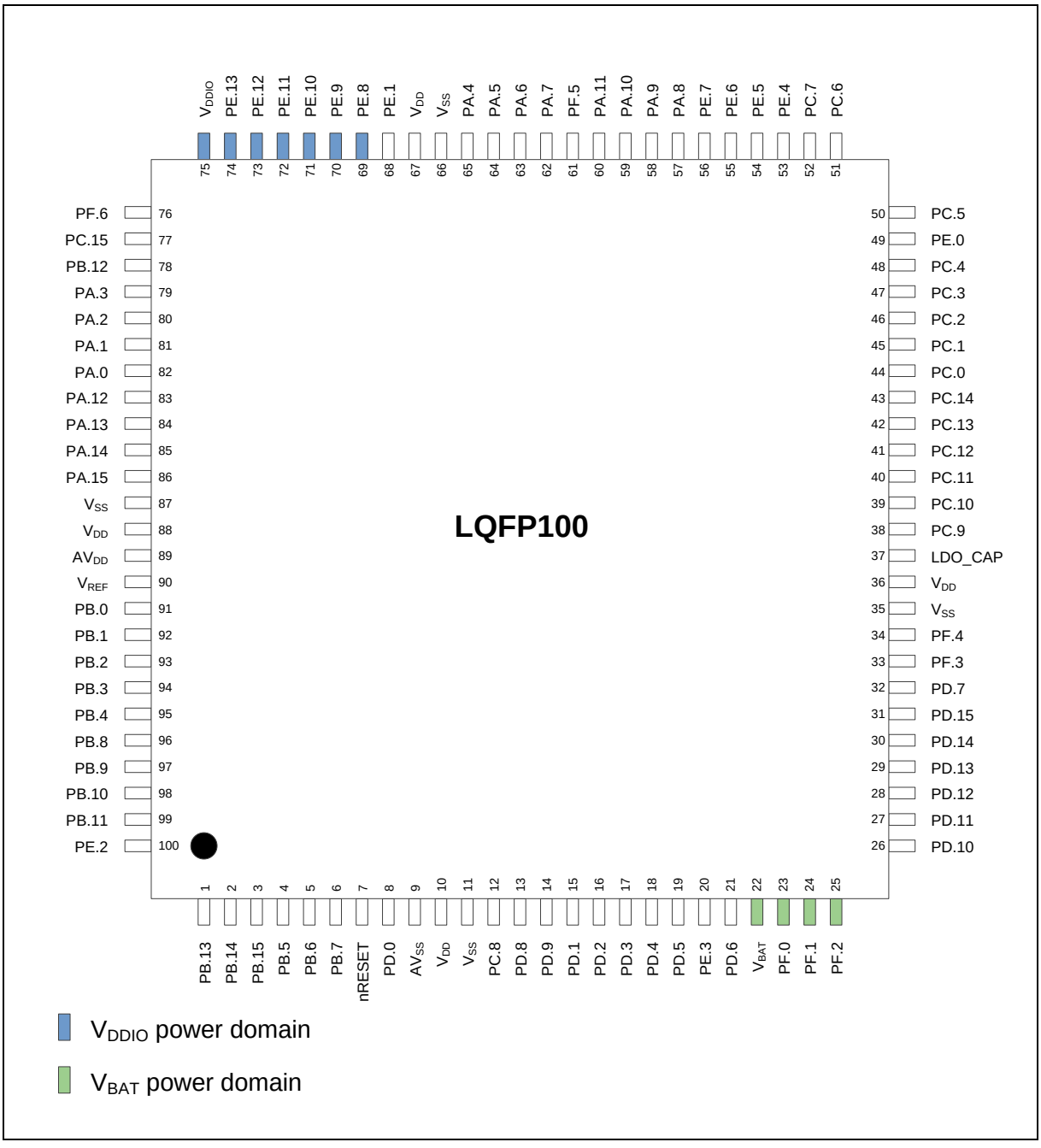


Figure 4.2-3 NuMicro® M0564 Base Series LQFP 100-pin Diagram

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			USCI2_CLK	I/O	MFP5	USCI2 clock pin.
			PWM1_BRAKE1	I	MFP6	PWM1 Brake 1 input pin.
		26	PD.10	I/O	MFP0	General purpose digital I/O pin.
			TM2	I/O	MFP4	Timer2 event counter input/toggle output pin.
			USCI2_DAT0	I/O	MFP5	USCI2 data 0 pin.
		27	PD.11	I/O	MFP0	General purpose digital I/O pin.
			TM3	I/O	MFP4	Timer3 event counter input/toggle output pin.
			USCI2_DAT1	I/O	MFP5	USCI2 data 1 pin.
	17	28	PD.12	I/O	MFP0	General purpose digital I/O pin.
			USCI1_CTL0	I/O	MFP1	USCI1 control 0 pin.
			SPI1_SS	I/O	MFP2	SPI1 slave select pin.
			UART0_TXD	O	MFP3	UART0 data transmitter output pin.
			PWM1_CH0	I/O	MFP6	PWM1 channel 0 output/capture input.
			EBI_ADR16	O	MFP7	EBI address bus bit 16.
	18	29	PD.13	I/O	MFP0	General purpose digital I/O pin.
			USCI1_DAT1	I/O	MFP1	USCI1 data 1 pin.
			SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
			UART0_RXD	I	MFP3	UART0 data receiver input pin.
			PWM1_CH1	I/O	MFP6	PWM1 channel 1 output/capture input.
			EBI_ADR17	O	MFP7	EBI address bus bit 17.
	19	30	PD.14	I/O	MFP0	General purpose digital I/O pin.
			USCI1_DAT0	I/O	MFP1	USCI1 data 0 pin.
			SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
			UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
			PWM1_CH2	I/O	MFP6	PWM1 channel 2 output/capture input.
			EBI_ADR18	O	MFP7	EBI address bus bit 18.
	20	31	PD.15	I/O	MFP0	General purpose digital I/O pin.
			USCI1_CLK	I/O	MFP1	USCI1 clock pin.
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
			UART0_nRTS	O	MFP3	UART0 request to Send output pin.
			PWM1_CH3	I/O	MFP6	PWM1 channel 3 output/capture input.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			UART2_TXD	O	MFP3	UART2 data transmitter output pin.
			USCI0_CTL1	I/O	MFP4	USCI0 control 1 pin.
			ACMP1_O	O	MFP5	Analog comparator 1 output pin.
			PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
			EBI_AD10	I/O	MFP7	EBI address/data bus bit 10.
22	30	47	PC.3	I/O	MFP0	General purpose digital I/O pin.
			SC0_PWR	O	MFP1	Smart Card 0 power pin.
			SPI0_MOSI	I/O	MFP2	SPI0 MOSI (Master Out, Slave In) pin.
			UART2_RXD	I	MFP3	UART2 data receiver input pin.
			USCI0_CTL0	I/O	MFP5	USCI0 control 0 pin.
			PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
			EBI_AD11	I/O	MFP7	EBI address/data bus bit 11.
23	31	48	PC.4	I/O	MFP0	General purpose digital I/O pin.
			SC0_nCD	I	MFP1	Smart Card 0 card detect pin.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			I2C1_SCL	I/O	MFP3	I2C1 clock pin.
			USCI0_CLK	I/O	MFP5	USCI0 clock pin.
			PWM0_CH4	I/O	MFP6	PWM0 channel 4 output/capture input.
			EBI_AD12	I/O	MFP7	EBI address/data bus bit 12.
24	32	49	PE.0	I/O	MFP0	General purpose digital I/O pin.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
			TM2_EXT	I/O	MFP4	Timer2 external capture input/toggle output pin.
			SC0_nCD	I	MFP5	Smart Card 0 card detect pin.
			PWM0_CH0	I/O	MFP6	PWM0 channel 0 output/capture input.
			EBI_nCS1	O	MFP7	EBI chip select 1 output pin.
			INT4	I	MFP8	External interrupt 4 input pin.
25	33	50	PC.5	I/O	MFP0	General purpose digital I/O pin.
			SPI0_I2SMCLK	I/O	MFP2	SPI0 I2S master clock output pin
			I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
			USCI0_DAT0	I/O	MFP4	USCI0 data 0 pin.

48 Pin	64 Pin	100 Pin	Pin Name	Type	MFP	Description
			EBI_nWRL	O	MFP7	EBI low byte write enable output pin.
			INT1	I	MFP8	External interrupt 1 input pin.
44	58	92	PB.1	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
			VDET_P1	A	MFP2	Voltage detector positive input 1 pin.
			UART2_TXD	O	MFP3	UART2 data transmitter output pin.
			TM3	I/O	MFP4	Timer3 event counter input/toggle output pin.
			SC0_RST	O	MFP5	Smart Card 0 reset pin.
			PWM0_SYNC_OUT	O	MFP6	PWM0 counter synchronous trigger output pin.
			EBI_nWRH	O	MFP7	EBI high byte write enable output pin
			USCI1_DAT1	I/O	MFP8	USCI1 data 1 pin.
45	59	93	PB.2	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
			SPI0_CLK	I/O	MFP2	SPI0 serial clock pin.
			SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.
			UART1_RXD	I	MFP4	UART1 data receiver input pin.
			SC0_nCD	I	MFP5	Smart Card 0 card detect pin.
			TM_BRAKE0	I	MFP6	Timer Brake 0 input pin.
			EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
			USCI0_DAT0	I/O	MFP8	USCI0 data 0 pin.
46	60	94	PB.3	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
			SPI0_MISO	I/O	MFP2	SPI0 MISO (Master In, Slave Out) pin.
			SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
			UART1_TXD	O	MFP4	UART1 data transmitter output pin.
			TM_BRAKE1	I	MFP6	Timer Brake 1 input pin.
			EBI_ALE	O	MFP7	EBI address latch enable output pin.
			USCI0_DAT1	I/O	MFP8	USCI0 data 1 pin.
47	61	95	PB.4	I/O	MFP0	General purpose digital I/O pin.
			ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
			SPI0_SS	I/O	MFP2	SPI0 slave select pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PB.4	MFP6	I	
SPI0	SPI0_CLK	PB.7	MFP2	I/O	SPI0 serial clock pin.
		PC.12	MFP2	I/O	
		PC.0	MFP2	I/O	
		PE.0	MFP2	I/O	
		PE.13	MFP2	I/O	
		PB.2	MFP2	I/O	
	SPI0_I2SMCLK	PD.0	MFP1	I/O	SPI0 I2S master clock output pin
		PD.3	MFP2	I/O	
		PD.7	MFP2	I/O	
		PC.9	MFP2	I/O	
		PC.5	MFP2	I/O	
	SPI0_MISO	PB.6	MFP2	I/O	SPI0 MISO (Master In, Slave Out) pin.
		PC.11	MFP2	I/O	
		PC.4	MFP2	I/O	
		PE.10	MFP2	I/O	
		PB.3	MFP2	I/O	
	SPI0_MOSI	PB.5	MFP2	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		PC.10	MFP2	I/O	
		PC.3	MFP2	I/O	
		PE.11	MFP2	I/O	
	SPI0_SS	PC.13	MFP2	I/O	SPI0 slave select pin.
		PC.2	MFP2	I/O	
		PE.12	MFP2	I/O	
		PB.4	MFP2	I/O	
SPI1	SPI1_CLK	PB.7	MFP3	I/O	SPI1 serial clock pin.
		PD.4	MFP2	I/O	
		PD.15	MFP2	I/O	
		PA.7	MFP2	I/O	
		PE.10	MFP6	I/O	
		PE.13	MFP1	I/O	
		PB.2	MFP3	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	SPI1_I2SMCLK	PD.0	MFP2	I/O	SPI1 I2S master clock output pin
		PA.12	MFP2	I/O	
	SPI1_MISO	PB.6	MFP3	I/O	SPI1 MISO (Master In, Slave Out) pin.
		PD.5	MFP2	I/O	
		PD.14	MFP2	I/O	
		PA.6	MFP2	I/O	
		PE.10	MFP1	I/O	
		PE.11	MFP6	I/O	
		PB.3	MFP3	I/O	
	SPI1_MOSI	PB.5	MFP3	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PE.3	MFP2	I/O	
		PD.13	MFP2	I/O	
		PA.5	MFP2	I/O	
		PE.11	MFP1	I/O	
		PE.12	MFP6	I/O	
	SPI1_SS	PD.6	MFP2	I/O	SPI1 slave select pin.
		PD.12	MFP2	I/O	
		PA.4	MFP2	I/O	
		PE.12	MFP1	I/O	
		PE.13	MFP6	I/O	
		PB.4	MFP3	I/O	
TM0	TM0	PD.1	MFP6	I/O	Timer0 event counter input/toggle output pin.
		PD.4	MFP6	I/O	
		PE.8	MFP3	I/O	
	TM0_EXT	PD.2	MFP3	I/O	Timer0 external capture input/toggle output pin.
		PA.7	MFP3	I/O	
		PE.10	MFP8	I/O	
TM1	TM1	PD.5	MFP6	I/O	Timer1 event counter input/toggle output pin.
		PD.7	MFP4	I/O	
		PE.9	MFP3	I/O	
	TM1_EXT	PD.3	MFP3	I/O	Timer1 external capture input/toggle output pin.
		PA.6	MFP3	I/O	

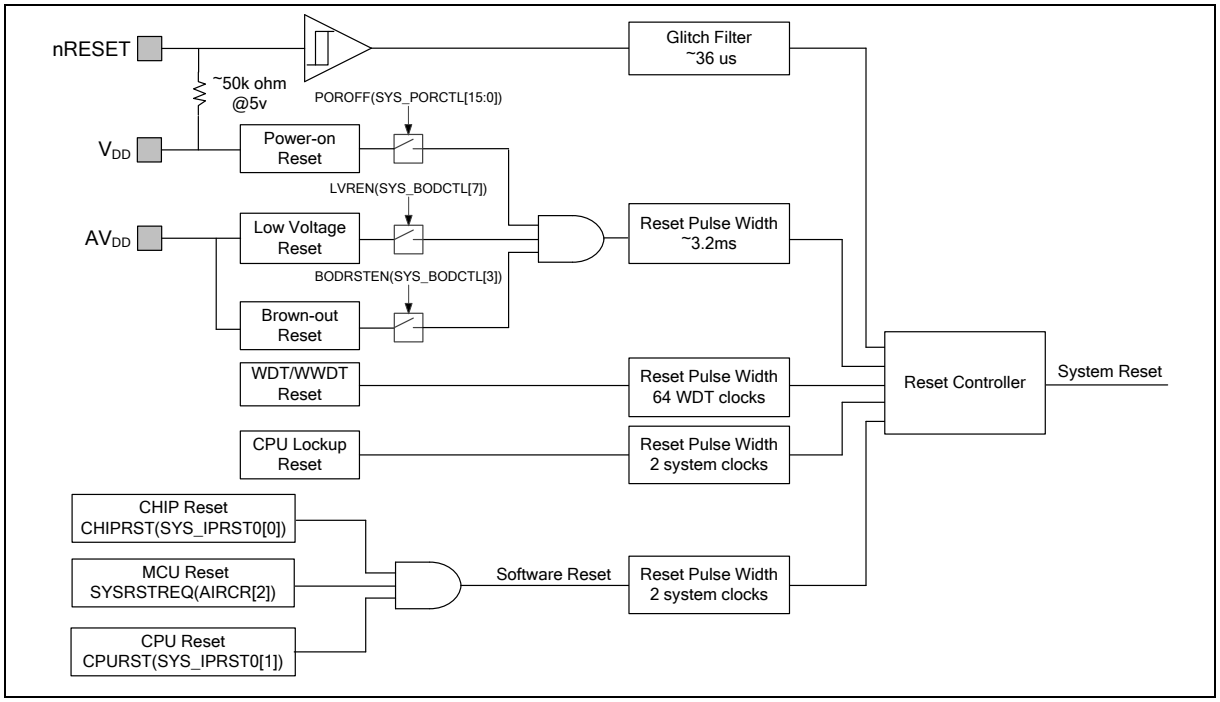


Figure 6.2-1 System Reset Sources

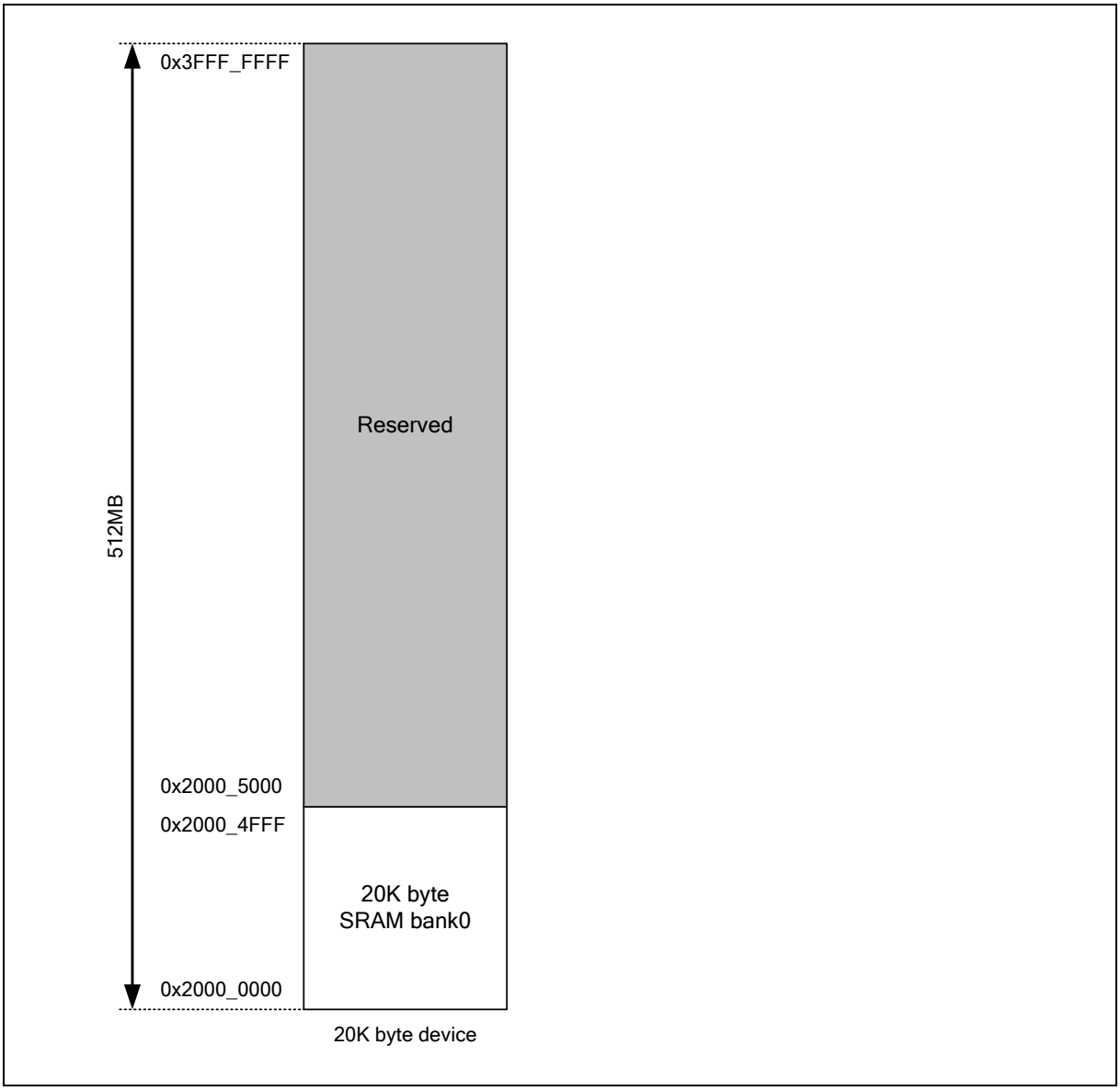


Figure 6.2-9 SRAM Memory Organization

6.2.7 Register Lock

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x5000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

After the protection is disabled, user can check the protection disable bit at address 0x5000_0100 bit0, 1 is protection disable, and 0 is protection enable. Then user can update the target protected register value and then write any data to the address “0x5000_0100” to enable register protection.

6.2.8 Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz and 22.1184 MHz RC oscillator),

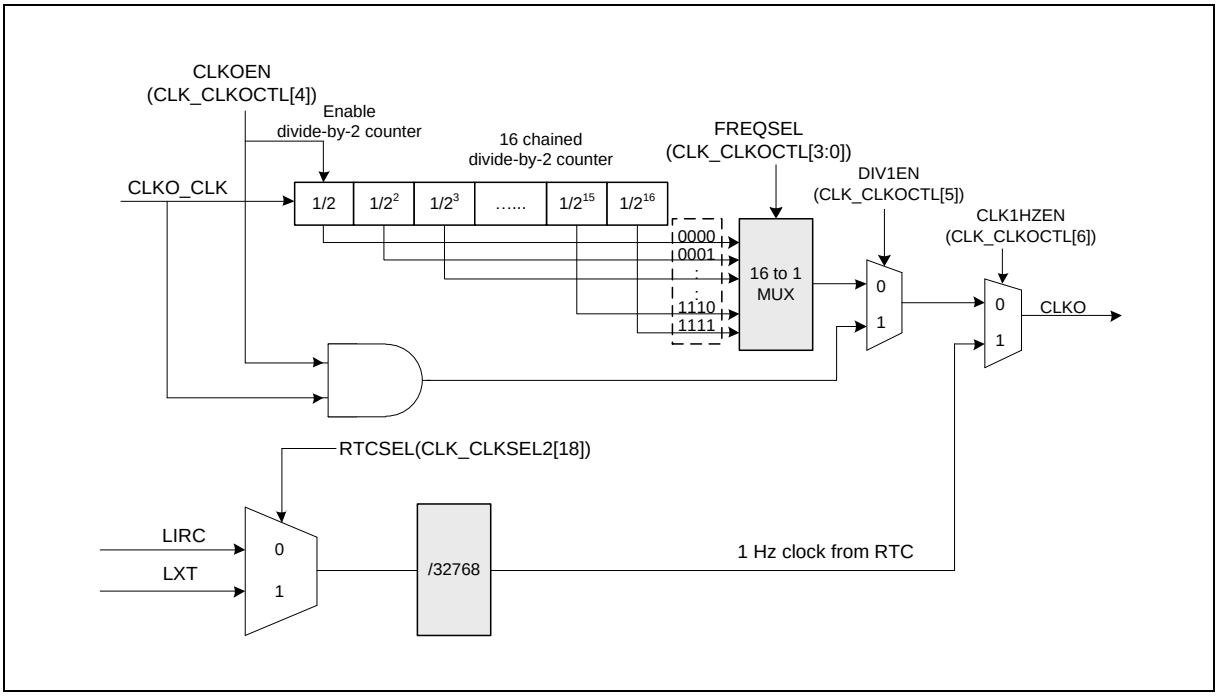


Figure 6.3-7 Clock Output Block Diagram

6.12 PDMA Controller (PDMA)

6.12.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 5 channels and each channel can perform transfer between memory and peripherals or between memory and memory. The PDMA supports time-out function for channel 0 and channel 1.

6.12.2 Features

- Supports 5 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI, UART, I^2S, I^2C, ADC, PWM and TIMER request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function for channel0 and channel 1

6.13 PWM Generator and Capture Timer (PWM)

6.13.1 Overview

The M0564 provides two PWM generator: PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

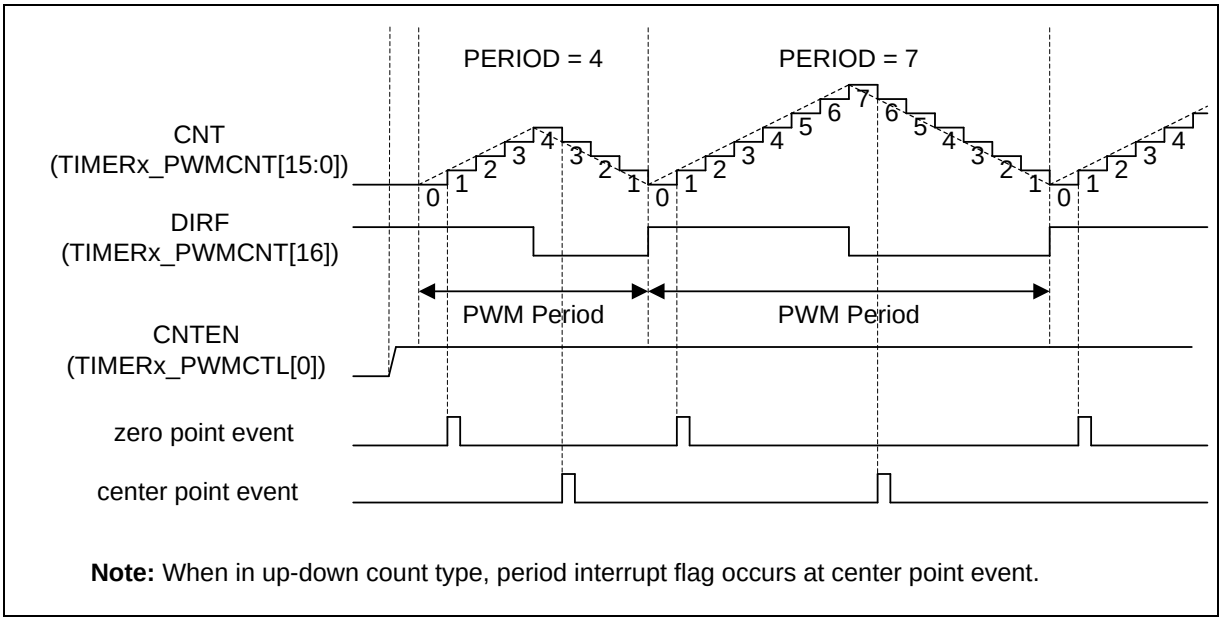
The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various PWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for ADC. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function. It supports latch PWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.13.2 Features

6.13.2.1 PWM function features

- Supports maximum clock frequency up to144MHz
- Supports up to two PWM modules, each module provides 6 output channels.
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channels:
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up-down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator, ADC result monitor and system safety events (clock failed, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared



Note: When in up-down count type, period interrupt flag occurs at center point event.

Figure 6.17-4 PWM Up-Down Count Type

6.17.3.6 PWM Counter Operation mode

The PWM counter supports two operation modes: one-shot mode and auto-reload mode. PWM counter will operate in one-shot mode if CNTMODE (TIMERx_PWMCTL[3]) bit is set to 1, and operate in auto-reload mode if CNTMODE bit is set to 0.

In both modes, CMP (TIMERx_PWMCMPDAT[15:0]) and PERIOD (TIMERx_PWMPERIOD[15:0]) should be written first and then set CNTEN (TIMERx_PWMCTL[0]) bit to 1 to start counter running.

In one-shot mode, PWM counter value will reload to default value according count type after one PWM period is completed. User can write CMP to continuous one-shot operation to generate next one-shot pulse once no matter current one-shot counter is running or completed.

In auto-reload mode, PWM counter is continuous running with current active PERIOD and CMP. If user set PERIOD to zero in auto-reload mode, PWM counter value will reload to default value according count type after one PWM period is completed.

6.17.3.7 PWM Comparator

The CMP (TIMERx_PWMCMPDAT[15:0]) is comparator register of PWM. The CMP value is continuously compared to the corresponding counter value. When the counter is equal to CMP, PWM generates a compared point event. This event will generate PWM output pulse, interrupt signal or trigger ADC start convert. In up-down count type, two events will be generated in a PWM period as shown in Figure 6.17-5. The CMPU is up count compared point event and CMPD is down count compared point event.

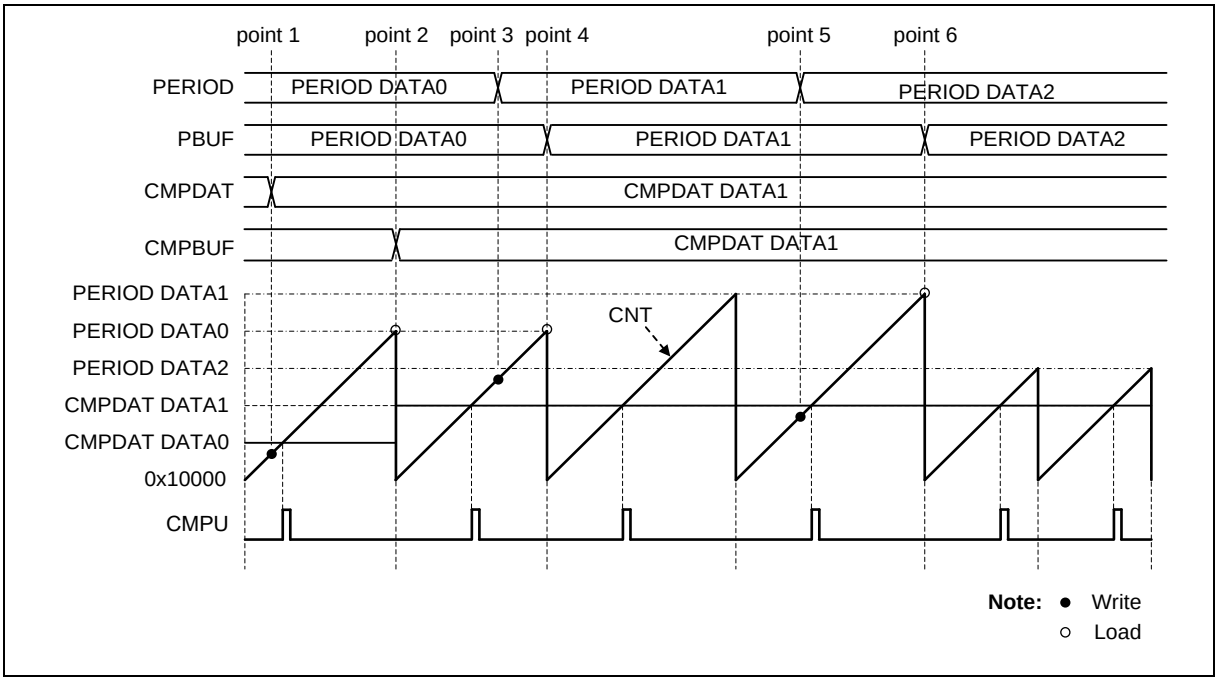


Figure 6.17-6 Period Loading Mode with Up Count Type

6.17.3.9 Immediately Loading Mode

When the IMMLDEN (TIMERx_PWMCTL[9]) bit set to 1, PWM operates at immediately loading mode. In immediately loading mode, when user update PERIOD (TIMERx_PWMPERIOD[15:0]) or CMP (TIMERx_PWMCMPDAT[15:0]), PERIOD or CMP will be load to active PBUF (TIMERx_PWMPBUF[15:0]) or CMPBUF (TIMERx_PWMCMPBUF[15:0]) after current counter count is completed. If the update PERIOD value is less than current counter value, counter will count wraparound. The following steps are the sequence of Figure 6.17-7.

1. User writes CMP DATA1 at point 1 and hardware will load CMP DATA1 to CMPBUF after current counter count is completed.
2. User writes PERIOD DATA1 at point 2 and PERIOD DATA1 is greater than current counter value, PWM counter will continuously count until equal to PERIOD DATA1 to complete one PWM period.
3. User writes PERIOD DATA2 at point 3 and PERIOD DATA2 is less than the current counter value, PWM counter will continuously count to maximum counter value 0x1FFFF and wraparound from 0x10000 to PERIOD DATA2 to complete one PWM period.

will occurred when TM_BRAKEx (x=0~3) pin status from high to low.

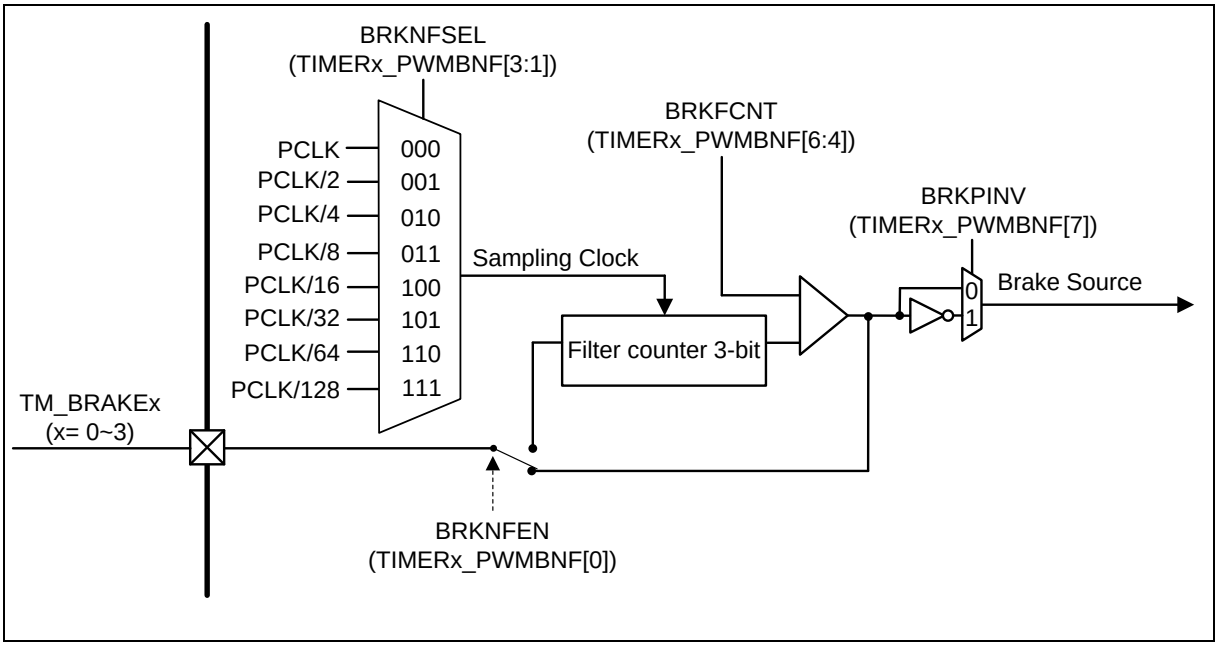


Figure 6.17-16 Brake Pin Noise Filter Block Diagram

User can set BRKAEVEN (TIMERx_PWMBRKCTL[17:16]) for PWMx_CH0 output state and BRKAODD (TIMERx_PWMBRKCTL[19:18]) for PWMx_CH1 output state when PWM brake event happened. There are two brake detector sources, edge detect brake source and level detect brake source when brake event happened. Figure 6.17-17 shows the brake event block diagram for PWMx_CH0 and PWMx_CH1.

8.4 Analog Characteristics

8.4.1 LDO

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Temperature	T_A	-40	-	+105	°C	
DC Power Supply	V_{DD}	2.5	-	5.5	V	
Output Voltage	V_{LDO}	1.62	1.8	1.98	V	

Note 1: It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

Note 2: For ensuring power stability, a 1μF Capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

8.4.2 Temperature Sensor

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Detection Temperature	T_{DET}	-40	-	+105	°C	
Gain	V_{TG}	-1.76	-1.70	-1.64	mV/°C	
Offset	V_{TO}	-	745	-	mV	Temperature at 0 °C
Operating current	I_{TEMP}	6.4	-	10.5	μA	

Note 1: The temperature sensor formula for the output voltage (Vtemp) is as below equation.

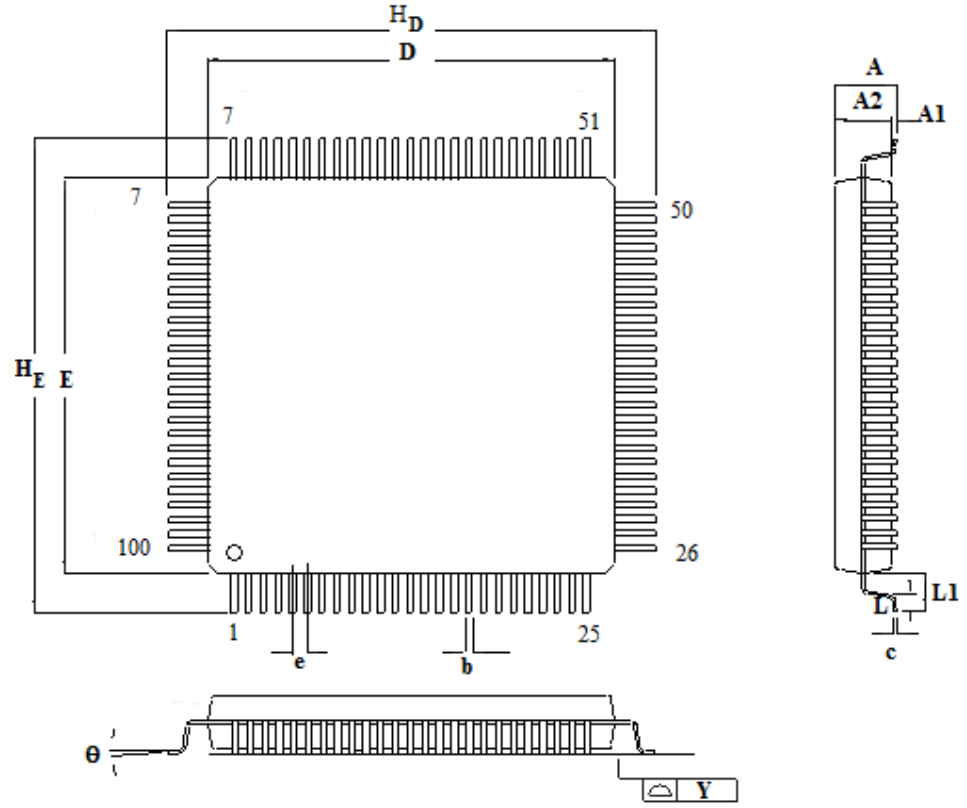
Vtemp (mV) = Gain (mV/℃) x Temperature (℃) + Offset (mV)

8.4.3 Internal Voltage Reference (Int_V_{REF})

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
V_{REF} (2.048V)	V_{REF1}	1.986	-	2.151	V	VREFCTL = 3, AV_{DD}≥2.5V
V_{REF} (2.56V)	V_{REF2}	2.483	-	2.637	V	VREFCTL = 3, AV_{DD}≥2.9V
V_{REF} (3.072V)	V_{REF3}	2.98	-	3.164	V	VREFCTL = 3, AV_{DD}≥3.4V
V_{REF} (4.096V)	V_{REF4}	3.973	-	4.219	V	VREFCTL = 3, AV_{DD}≥4.5V
Start-up Time	T_{VREF_Start}	-	700	2000	uS	C_{VREF} = 4.7uF
Operating current	I_{VREF}		100		μA	

9 PACKAGE DIMENSIONS

9.1 LQFP 100L (14x14x1.4 mm footprint 2.0 mm)



Controlling Dimension : Millimeters

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	-
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.10	0.15	0.20
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e	-	0.50	-
HD	15.80	16.00	16.20
HE	15.80	16.00	16.20
L	0.45	0.60	0.75
L1	-	1	-
y	-	-	0.10
θ	0°	-	7°

10 REVISION HISTORY

Date	Revision	Description
2017.05.05	1.00	Preliminary version