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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4/M0+ |
| Core Size | 32-Bit Dual-Core |
| Speed | 100MHz |
| Connectivity | I²C, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 96K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 12x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54113j128bd64ql |

- ARM Cortex-M0+ core
  - ARM Cortex-M0+ processor, running at a frequency of up to 100 MHz (uses the same clock as Cortex-M4) with a single-cycle multiplier and a fast single-cycle I/O port.
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
  - Non-maskable Interrupt (NMI) input with a selection of sources.
  - Serial Wire Debug with four breakpoints and two watch points.
  - System tick timer.
- On-chip memory:
  - Up to 256 KB on-chip flash program memory with flash accelerator and 256 byte page erase and write.
  - Up to 192 KB total SRAM consisting of 160 KB contiguous main SRAM and an additional 32 KB SRAM on the I&D buses.
- ROM API support:
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
  - ROM-based USB drivers (HID, CDC, MSC, and DFU). Flash updates via USB is supported.
  - Supports booting from valid user code in flash, USART, SPI, and $I^2C$.
  - Legacy, Single, and Dual image boot.
- Serial interfaces:
  - Flexcomm Interface contains eight serial peripherals. Each can be selected by software to be a USART, SPI, or $I^2C$ interface. Two Flexcomm Interfaces also include an $I^2S$ interface. Each Flexcomm Interface includes a FIFO that supports USART, SPI, and $I^2S$ if supported by that Flexcomm Interface. A variety of clocking options are available to each Flexcomm Interface and include a shared fractional baud-rate generator.
  - $I^2C$-bus interfaces support Fast-mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Two sets of true $I^2C$ pads also support high speed mode (3.4 Mbit/s) as a slave.
  - USB 2.0 full-speed device controller with on-chip PHY and dedicated DMA controller supporting crystal-less operation in device mode using software library. See Technical note TN00031 for more details.
- Digital peripherals:
  - DMA controller with 20 channels and 20 programmable triggers, able to access all memories and DMA-capable peripherals.
  - Up to 48 General-Purpose Input/Output (GPIO) pins. Most GPIOs have configurable pull-up/pull-down resistors, programmable open-drain mode, and input inverter.
  - GPIO registers are located on the AHB for fast access.
  - Up to eight GPIOs can be selected as pin interrupts (PINT), triggered by rising, falling or both input edges.
  - Two GPIO grouped interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
  - CRC engine.

## 6.2 Pin description

On the LPC5411x, digital pins are grouped into two ports. Each digital pin may support up to four different digital functions and one analog function, including General Purpose I/O (GPIO).

**Table 4. Pin description**

| Symbol | 49-pin | 64-pin | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|
| PIO0_0 | A6 | 31 | [2] | PU | I/O | **PIO0_0 —** General-purpose digital input/output pin.<br>**Remark:** In ISP mode, this pin is set to the Flexcomm Interface 0 USART RXD function. |
| | | | | | I/O | **FC0_RXD_SDA_MOSI —** Flexcomm Interface 0: USART RXD, I2C SDA, SPI MOSI. |
| | | | | | I/O | **FC3_CTS_SDA_SSEL0 —** Flexcomm Interface 3: USART CTS, I2C SDA, SPI SSEL0. |
| | | | | | I | **CTimer0_CAP0 —** 32-bit CTimer0 capture input 0. |
| | | | | | | **R —** Reserved. |
| | | | | | O | **SCT0_OUT3 —** SCT0 output 3. PWM output 3. |
| PIO0_1 | B6 | 32 | [2] | PU | I/O | **PIO0_1 —** General-purpose digital input/output pin.<br>**Remark:** In ISP mode, this pin is set to the Flexcomm Interface 0 USART TXD function. |
| | | | | | I/O | **FC0_TXD_SCL_MISO —** Flexcomm Interface 0: USART TXD, I2C SCL, SPI MISO. |
| | | | | | I/O | **FC3_RTS_SCL_SSEL1 —** Flexcomm Interface 3: USART RTS, I2C SCL, SPI SSEL1. |
| | | | | | I | **CTimer0_CAP1 —** 32-bit CTimer0 capture input 1. |
| | | | | | | **R —** Reserved. |
| | | | | | O | **SCT0_OUT1 —** SCT0 output 1. PWM output 1. |
| PIO0_2 | - | 36 | [2] | PU | I/O | **PIO0_2 —** General-purpose digital input/output pin. |
| | | | | | I/O | **FC0_CTS_SDA_SSEL0 —** Flexcomm Interface 0: USART CTS, I2C SDA, SPI SSEL0. |
| | | | | | I/O | **FC3_SSEL3 —** Flexcomm Interface 3: SPI SSEL3. |
| | | | | | I | **CTimer2_CAP1 —** 32-bit CTimer2 capture input 1. |
| PIO0_3 | - | 37 | [2] | PU | I/O | **PIO0_3 —** General-purpose digital input/output pin. |
| | | | | | I/O | **FC0_RTS_SCL_SSEL1 —** Flexcomm Interface 0: USART RTS, I2C SCL, SPI SSEL1. |
| | | | | | I/O | **FC2_SSEL2 —** Flexcomm Interface 2: SPI SSEL2. |
| | | | | | O | **CTimer1_MAT3 —** 32-bit CTimer1 match output 3. |
| PIO0_4 | C7 | 38 | [2] | PU | I/O | **PIO0_4 —** General-purpose digital input/output pin.<br>**Remark:** The state of this pin at Reset in conjunction with PIO0_31 and PIO1_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM10914 for more details. |
| | | | | | I/O | **FC0_SCK —** Flexcomm Interface 0: USART or SPI clock. |
| | | | | | I/O | **FC3_SSEL2 —** Flexcomm Interface 3: SPI SSEL2. |
| | | | | | I | **CTimer0_CAP2 —** 32-bit CTimer0 capture input 2. |

**Table 4. Pin description** *…continued*

| Symbol | 49-pin | 64-pin | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|
| PIO0_11 | E5 | 46 | [2] | PU | I/O | **PIO0_11 —** General-purpose digital input/output pin. In ISP mode, this pin is set to the Flexcomm 3 SPI SCK function. |
| | | | | | I/O | **FC3_SCK —** Flexcomm Interface 3: USART or SPI clock. |
| | | | | | I/O | **FC6_RXD_SDA_MOSI_DATA —** Flexcomm Interface 6: USART RXD, I2C SDA, SPI MOSI, I2S DATA. |
| | | | | | O | **CTimer2_MAT1 —** 32-bit CTimer2 match output 1. |
| PIO0_12 | F7 | 47 | [2] | PU | I/O | **PIO0_12 —** General-purpose digital input/output pin. In ISP mode, this pin is set to the Flexcomm 3 SPI MOSI function. |
| | | | | | I/O | **FC3_RXD_SDA_MOSI —** Flexcomm Interface 3: USART RXD, I2C SDA, SPI MOSI. |
| | | | | | I/O | **FC6_TXD_SCL_MISO_WS —** Flexcomm Interface 6: USART TXD, I2C SCL, SPI MISO, I2S WS. |
| | | | | | O | **CTimer2_MAT3 —** 32-bit CTimer2 match output 3. |
| PIO0_13 | G7 | 48 | [2] | PU | I/O | **PIO0_13 —** General-purpose digital input/output pin. In ISP mode, this pin is set to the Flexcomm 3 SPI MISO function. |
| | | | | | I/O | **FC3_TXD_SCL_MISO —** Flexcomm Interface 3: USART TXD, I2C SCL, SPI MISO. |
| | | | | | O | **SCT0_OUT4 —** SCT0 output 4. PWM output 4. |
| | | | | | O | **CTimer2_MAT0 —** 32-bit CTimer2 match output 0. |
| PIO0_14/ TCK | F6 | 49 | [2] | PU | I/O | **PIO0_14 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock In). In ISP mode, this pin is set to the Flexcomm 3 SPI SSELN0 function. |
| | | | | | I/O | **FC3_CTS_SDA_SSEL0 —** Flexcomm Interface 3: USART CTS, I2C SDA, SPI SSEL0. |
| | | | | | O | **SCT0_OUT5 —** SCT0 output 5. PWM output 5. |
| | | | | | O | **CTimer2_MAT1 —** 32-bit CTimer2 match output 1. |
| | | | | | | **R —** Reserved. |
| | | | | | I/O | **FC1_SCK —** Flexcomm Interface 1: USART or SPI clock. |
| PIO0_15/ TDO | G6 | 50 | [2] | PU | I/O | **PIO0_15 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out). |
| | | | | | I/O | **FC3_RTS_SCL_SSEL1 —** Flexcomm Interface 3: USART RTS, I2C SCL, SPI SSEL1. |
| | | | | | I/O | **SWO —** Serial wire trace output. |
| | | | | | O | **CTimer2_MAT2 —** 32-bit CTimer2 match output 2. |
| | | | | | | **R —** Reserved. |
| | | | | | I/O | **FC4_SCK —** Flexcomm Interface 4: USART or SPI clock. |

**Table 4. Pin description** *…continued*

| Symbol | 49-pin | 64-pin | | Reset state [1] | Type | Description |
|---|---|---|---|---|---|---|
| PIO1_5/ ADC0_8 | B3 | 19 | [4] | PU | I/O; AI | **PIO1_5/ADC0_8 —** General-purpose digital input/output pin. ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. |
| | | | | | I | **PDM1_DATA —** Data for PDM interface 1, digital microphone input. Also PDM clock input in bypass mode. |
| | | | | | I/O | **FC7_CTS_SDA_SSEL0 —** Flexcomm Interface 7: USART CTS, I2C SDA, SPI SSEL0. |
| | | | | | I | **CTimer1_CAP0 —** 32-bit CTimer1 capture input 0. |
| | | | | | | **R —** Reserved. |
| | | | | | O | **CTimer1_MAT3 —** 32-bit CTimer1 match output 3. |
| | | | | | | **R —** Reserved. |
| | | | | | O | **USB_FRAME —** USB start-of-frame signal derived from host signaling. |
| PIO1_6/ ADC0_9 | A5 | 26 | [4] | PU | I/O; AI | **PIO1_6/ADC0_9 —** General-purpose digital input/output pin. ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.<br>**Remark:** This pin is also used as part of secondary selection of boot source for ISP mode after device reset, in connection with PIO0_31 and PIO0_4. See the Boot Process chapter in UM10914 for more details. |
| | | | | | | **R —** Reserved. |
| | | | | | I/O | **FC7_SCK —** Flexcomm Interface 7: USART, SPI, or I2S clock. |
| | | | | | I | **CTimer1_CAP2 —** 32-bit CTimer1 capture input 2. |
| | | | | | | **R —** Reserved. |
| | | | | | O | **CTimer1_MAT2 —** 32-bit CTimer1 match output 2. |
| | | | | | | **R —** Reserved. |
| | | | | | I | **USB_VBUS —** Monitors the presence of USB bus power. This signal must be HIGH for USB reset to occur. |
| PIO1_7/ ADC0_10 | B5 | 27 | [4] | PU | I/O; AI | **PIO1_7/ADC0_10 —** General-purpose digital input/output pin. ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. |
| | | | | | | **R —** Reserved. |
| | | | | | I/O | **FC7_RXD_SDA_MOSI_DATA —** Flexcomm Interface 7: USART RXD, I2C SDA, SPI MOSI, I2S DATA. |
| | | | | | O | **CTimer1_MAT2 —** 32-bit CTimer1 match output 2. |
| | | | | | | **R —** Reserved. |
| | | | | | I | **CTimer1_CAP2 —** 32-bit CTimer1 capture input 2. |
| PIO1_8/ ADC0_11 | C5 | 28 | [4] | PU | I/O; AI | **PIO1_8/ADC0_11 —** General-purpose digital input/output pin. ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. |
| | | | | | | **R —** Reserved. |
| | | | | | I/O | **FC7_TXD_SCL_MISO_WS —** Flexcomm Interface 7: USART TXD, I2C SCL, SPI MISO, I2S WS. |
| | | | | | O | **CTimer1_MAT3 —** 32-bit CTimer1 match output 3. |
| | | | | | | **R —** Reserved. |
| | | | | | I | **CTimer1_CAP3 —** 32-bit CTimer1 capture input 3. |

Table 9 describes signals on the clocking diagram.

**Table 7. Clocking diagram signal name descriptions**

| Name | Description |
|---|---|
| 32k_clk | The 32 kHz output of the RTC oscillator. The 32 kHz clock must be enabled in the RTCOSCCTRL register. |
| clk_in | This is the internal clock that comes from the main CLK_IN pin function. That function must be connected to the pin by selecting it in the IOCON block. |
| frg_clk | The output of the Fractional Rate Generator. |
| fro_12m | The 12 MHz output of the currently selected on-chip FRO oscillator. |
| fro_hf | The currently selected FRO high speed output. This may be either 96 MHz or 48 MHz. |
| main_clk | The main clock used by the CPU and AHB bus, and potentially many others. |
| mclk_in | The MCLK input function, when it is connected to a pin by selecting it in the IOCON block. |
| pll_clk | The output of the PLL. |
| wdt_clk | The output of the watchdog oscillator, which has a selectable target frequency. It must also be enabled in the PDRINCFG0 register. |
| “none” | A tied-off source that should be selected to save power when the output of the related multiplexer is not used. |

### 7.13.3 Brownout detection

The LPC5411x includes a monitor for the voltage level on the $V_{DD}$ pin. If this voltage falls below a fixed level, the BOD sets a flag that can be polled or cause an interrupt. In addition, a separate threshold levels can be selected to cause chip reset and interrupt.

### 7.13.4 Safety

The LPC5411x includes a Windowed WatchDog Timer (WWDT), which can be enabled by software after reset. Once enabled, the WWDT remains locked and cannot be modified in any way until a reset occurs.

## 7.14 Code security (Code Read Protection - CRP)

This feature of the LPC5411x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry can be invoked by pulling a pin on the LPC5411x LOW on reset. This pin is called the ISP entry pin.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. CRP3 fully disables any access to the chip via SWD and ISP. It is up to the user’s application to provide (if needed) flash update mechanism using IAP calls or a call to reinvoke ISP command to enable a flash update via USART.

generates an RTC wake-up interrupt request, which can wake up the part. During deep power-down mode, the contents of the SRAM and registers are not retained. All functional pins are tri-stated in deep power-down mode.

Table 8 shows the peripheral configuration in reduced power modes.

**Table 8. Peripheral configuration in reduced power modes**

| Peripheral | Reduced power mode | | |
|---|---|---|---|
| | Sleep | Deep-sleep | Deep power-down |
| FRO | Software configured | Software configured | Off |
| Flash | Software configured | Standby | Off |
| BOD | Software configured | Software configured | Off |
| PLL | Software configured | Off | Off |
| Watchdog osc and WWDT | Software configured | Software configured | Off |
| Micro-tick Timer | Software configured | Software configured | Off |
| DMA | Active | Configurable some for operations, see Section 7.13.2 | Off |
| USART | Software configured | Off; but can create a wake-up interrupt in synchronous slave mode or 32 kHz clock mode | Off |
| SPI | Software configured | Off; but can create a wake-up interrupt in slave mode | Off |
| I2C | Software configured | Off; but can create a wake-up interrupt in slave mode | Off |
| USB | Software configured | Software configured | Off |
| DMIC | Software configured | Software configured | Off |
| Other digital peripherals | Software configured | Off | Off |
| RTC oscillator | Software configured | Software configured | Software configured |

Table 9 shows the wake-up sources for reduced power modes.

**Table 9. Wake-up sources for reduced power modes**

| Power mode | Wake-up source | Conditions |
|---|---|---|
| Sleep | Any interrupt | Enable interrupt in NVIC. |
| | HWWAKE | Certain Flexcomm Interface and DMIC subsystem activity. |

- No chip clocks are required in order to receive and compare an address as a Slave, so this event can wake up the device from deep-sleep mode.

### 7.19.8 I²S-bus interface

The I²S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I²S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer as well as other configurations. In the LPC5411x, the I²S function is included in Flexcomm Interface 6 and Flexcomm Interface 7. Each of these Flexcomm Interfaces implement four I²S channel pairs.

The I²S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a master or a slave. Other channel pairs, if present, always operate as slaves. All of the channel pairs within one Flexcomm Interface share one set of I²S signals, and are configured together for either transmit or receive operation, using the same mode, same data configuration and frame configuration. All such channel pairs can participate in a time division multiplexing (TDM) arrangement. For cases requiring an MCLK input and/or output, this is handled outside of the I²S block in the system level clocking scheme.

#### 7.19.8.1 Features

- A Flexcomm Interface may implement one or more I²S channel pairs, the first of which could be a master or a slave, and the rest of which would be slaves. All channel pairs are configured together for either transmit or receive and other shared attributes. The number of channel pairs is defined for each Flexcomm Interface, and may be from 0 to 4.
- Configurable data size for all channels within one Flexcomm Interface, from 4 bits to 32 bits. Each channel pair can also be configured independently to act as a single channel (mono as opposed to stereo operation).
- All channel pairs within one Flexcomm Interface share a single bit clock (SCK) and word select/frame trigger (WS), and data line (SDA).
- Data for all I²S traffic within one Flexcomm Interface uses the Flexcomm Interface FIFO. The FIFO depth is 8 entries.
- Left justified and right justified data modes.
- DMA support using FIFO level triggering.
- TDM (Time Division Multiplexing) with a several stereo slots and/or mono slots is supported. Each channel pair can act as any data slot. Multiple channel pairs can participate as different slots on one TDM data line.
- The bit clock and WS can be selectively inverted.
- Sampling frequencies supported depends on the specific device configuration and applications constraints (e.g. system clock frequency, PLL availability, etc.) but generally supports standard audio data rates. See the data rates section in I2S chapter (UM10914) to calculate clock and sample rates.

**Remark:** The Flexcomm Interface function clock frequency should not be above 48 MHz.

### 7.20.6 Micro-tick timer (UTICK)

The ultra-low power Micro-tick Timer, running from the Watchdog oscillator, can be used to wake up the device from low power modes.

#### 7.20.6.1 Features

- Ultra simple timer.
- Write once to start.
- Interrupt or software polling.
- Four capture registers that can be triggered by external pin transitions.

## 7.21 12-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12-bit and fast conversion rates of up to 5.0 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCTimer/PWM, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

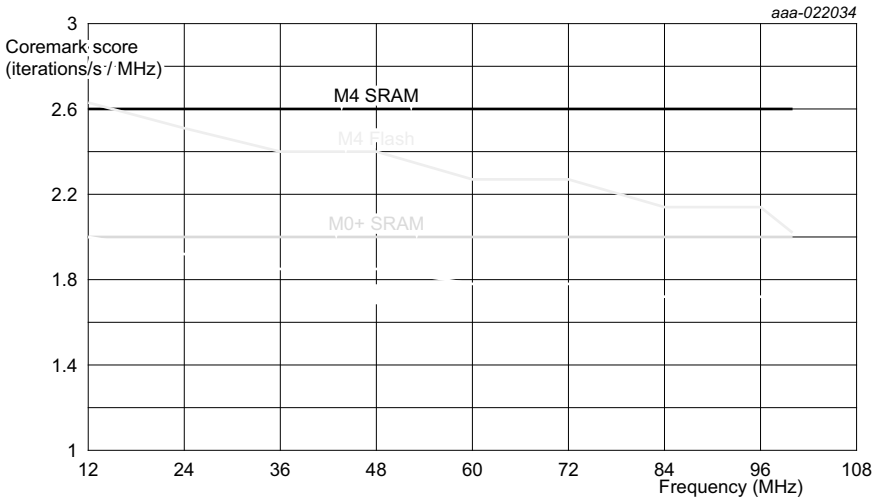
The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCTimer/PWM inputs for tight timing control between the ADC and the SCTimer/PWM.

### 7.21.1 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range $V_{REFN}$ to $V_{REFP}$ (not to exceed $V_{DDA}$ voltage level).
- 12-bit conversion rate of 5.0 MHz. Options for reduced resolution at higher conversion rates.
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.
- A temperature sensor is connected as an alternative input for ADC channel 0.

## 7.22 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a Complement To Absolute Temperature ($V_{CTAT}$) voltage. The output voltage varies inversely with device temperature with an absolute accuracy of better than ±3 °C over the full temperature range (-40 °C to +105 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

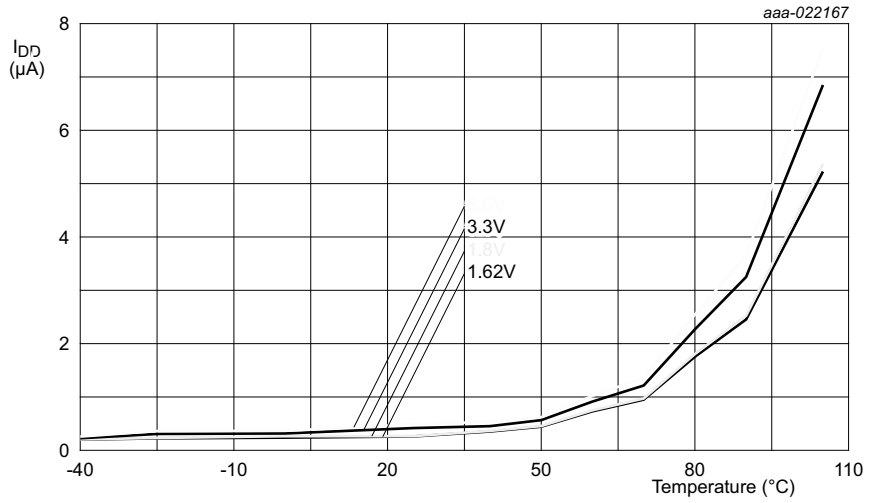



Conditions: $V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C; active mode; all peripherals disabled; BOD disabled; See the FLASHCFG register in the LPC5411x, UM10914 User Manual for system clock flash access time settings. Measured with Keil uVision 5.17. Optimization level 3, optimized for time ON.

12 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.

24 MHz, 36 MHz, 60 MHz, 72 MHz, 84 MHz, and 100 MHz: FRO enabled; PLL enabled.

**Fig 9. Typical CoreMark score**




Conditions: RTC disabled (RTC oscillator input grounded)

**Fig 12. Deep power-down mode: Typical supply current $I_{DD}$ versus temperature for different supply voltages $V_{DD}$**

**Table 18. Typical peripheral power consumption[1][2][3]**

*$V_{DD}$ = 3.3 V; $T_{amb}$ = 25 °C*

| Peripheral | $I_{DD}$ in uA |
|---|---|
| FRO (12 MHz, 48 MHz, 96 MHz) | 100.0 |
| WDT OSC | 2.0 |
| Flash | 200.0 |
| BOD | 2.0 |

[1] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[2] The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, and 96 MHz.

[3] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

**Table 19. Typical AHB/APB peripheral power consumption [3][4][5]**

*$T_{amb}$ = 25 °C, $V_{DD}$ = 3.3 V;*

| Peripheral | | $I_{DD}$ in uA/MHz | $I_{DD}$ in uA/MHz | $I_{DD}$ in uA/MHz |
|---|---|---|---|---|
| **AHB peripheral** | | **CPU: 12 MHz, sync APB bus: 12 MHz** | **CPU: 48 MHz, sync APB bus: 48 MHz** | **CPU: 96MHz, sync APB bus: 96 MHz** |
| USB | | 2.09 | 2.09 | 2.09 |
| Temperature sensor | | 0.02 | 0.01 | 0.01 |
| DMIC | | 0.17 | 0.17 | 0.17 |
| GPIO0 | [1] | 0.65 | 0.65 | 0.65 |
| GPIO1 | [1] | 0.56 | 0.56 | 0.56 |
| DMA | | 0.34 | 0.43 | 0.43 |
| CRC | | 0.50 | 0.54 | 0.54 |
| MAILBOX | | 0.12 | 0.12 | 0.12 |

**Table 20. Static characteristics: pin characteristics** *…continued*

*$T_{amb}$ = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ $V_{DD}$ ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Pin capacitance** | | | | | | | |
| $C_{io}$ | input/output capacitance | $I^2C$-bus pins | [8] | - | - | 6.0 | pF |
| | | pins with digital functions only | [6] | - | - | 2.0 | pF |
| | | Pins with digital and analog functions | [6] | - | - | 7.0 | pF |

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltage.

[2] Based on characterization. Not tested in production.

[3] With respect to ground.

[4] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[5] To $V_{SS}$.

[6] The values specified are simulated and absolute values, including package/bondwire capacitance.

[7] The weak pull-up resistor is connected to the $V_{DD}$ rail and pulls up the I/O pin to the $V_{DD}$ level.

[8] The value specified is a simulated value, excluding package/bondwire capacitance.

[9] Without 33 Ω ± 2 % series external resistor.

[10] The parameter values specified are simulated and absolute values.

[11] With 33 Ω ± 2 % series external resistor.

[12] With 15 KΩ ± 5 % resistor to $V_{SS}$.

[13] With 1.5 KΩ ± 5% resistor to 3.6 V external pull-up.

[14] Guaranteed by design, not tested in production.

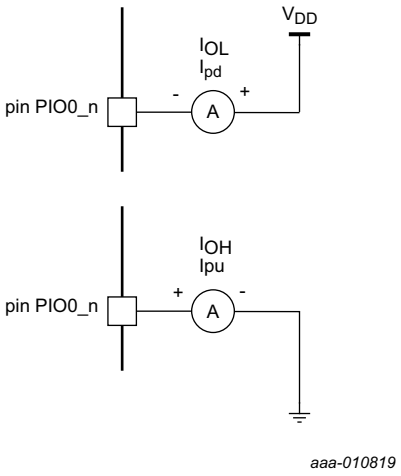



**Fig 13. Pin input/output current measurement**

# 11. Dynamic characteristics

## 11.1 Flash memory

**Table 21. Flash characteristics**

*$T_{amb}$ = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ $V_{DD}$ ≤ 3.6 V unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $N_{endu}$ | endurance | sector erase/program | [2] | 10000 | - | - | cycles |
| | | page erase/program; page in a sector | | 1000 | - | - | cycles |
| $t_{ret}$ | retention time | powered | | 10 | - | - | years |
| | | unpowered | | 10 | - | - | years |
| $t_{er}$ | erase time | page, sector, or multiple consecutive sectors | | - | 100 | - | ms |
| $t_{prog}$ | programming time | | [3] | - | 1 | - | ms |

[1] Typical ratings are not guaranteed.

[2] Number of erase/program cycles.

[3] Programming times are given for writing 256 bytes from RAM to the flash.

## 11.2 I/O pins

**Table 22. Dynamic characteristic: I/O pins[1]**

*$T_{amb}$ = −40 °C to +85 °C unless otherwise specified; 1.62 V ≤ $V_{DD}$ ≤ 3.6 V unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Standard I/O pins - normal drive strength** | | | | | | | |
| $t_r$ | rise time | pin configured as output; SLEW = 1 (fast mode); | [2][3] | | | | |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.0 | - | 2.5 | ns |
| | | 1.62 V ≤ $V_{DD}$ ≤ 1.98 V | | 1.6 | - | 3.8 | ns |
| $t_f$ | fall time | pin configured as output; SLEW = 1 (fast mode); | [2][3] | | | | |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 0.9 | - | 2.5 | ns |
| | | 1.62 V ≤$V_{DD}$ ≤ 1.98 V | | 1.7 | - | 4.1 | ns |
| $t_r$ | rise time | pin configured as output; SLEW = 0 (standard mode); | [2][3] | | | | |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.9 | - | 4.3 | ns |
| | | 1.62 V ≤ $V_{DD}$ ≤ 1.98 V | | 2.9 | - | 7.8 | ns |
| $t_f$ | fall time | pin configured as output; SLEW = 0 (standard mode); | [2][3] | | | | |
| | | 2.7 V ≤ $V_{DD}$ ≤ 3.6 V | | 1.9 | - | 4.0 | ns |
| | | 1.62 V ≤ $V_{DD}$ ≤ 1.98 V | | 2.7 | - | 6.7 | ns |
| $t_r$ | rise time | pin configured as input | [4] | 0.3 | - | 1.3 | ns |
| $t_f$ | fall time | pin configured as input | [4] | 0.2 | - | 1.2 | ns |

[1] Simulated data.

## 11.7 Watchdog oscillator

**Table 28. Dynamic characteristics: Watchdog oscillator**
*$T_{amb}$ = −40 °C to +105 °C; 1.62 V ≤ $V_{DD}$ ≤ 3.6 V*

| Symbol | Parameter | | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{osc(int)}$ | internal watchdog oscillator frequency | [2] | 6 | - | 1500 | kHz |
| $D_{clkout}$ | clkout duty cycle | | 48 | - | 52 | % |
| $J_{PP-CC}$ | peak-peak period jitter | [3][4] | - | 1 | 20 | ns |
| $t_{start}$ | start-up time | [4] | - | 4 | - | µs |

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{amb}$ = −40 °C to +105 °C) is ±40 %.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Guaranteed by design. Not tested in production samples.

## 11.8 I²C-bus

**Table 29. Dynamic characteristic: I²C-bus pins[1]**
*$T_{amb}$ = −40 °C to +105 °C; 1.62 V ≤ $V_{DD}$ ≤ 3.6 V[2]*

| Symbol | Parameter | | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | | Standard-mode | 0 | 100 | kHz |
| | | | Fast-mode | 0 | 400 | kHz |
| | | | Fast-mode Plus | 0 | 1 | MHz |
| $t_f$ | fall time | [4][5][6][7] | of both SDA and SCL signals Standard-mode | - | 300 | ns |
| | | | Fast-mode | 20 + 0.1 × $C_b$ | 300 | ns |
| | | | Fast-mode Plus | - | 120 | ns |
| $t_{LOW}$ | LOW period of the SCL clock | | Standard-mode | 4.7 | - | µs |
| | | | Fast-mode | 1.3 | - | µs |
| | | | Fast-mode Plus | 0.5 | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | Standard-mode | 4.0 | - | µs |
| | | | Fast-mode | 0.6 | - | µs |
| | | | Fast-mode Plus | 0.26 | - | µs |
| $t_{HD;DAT}$ | data hold time | [3][4][8] | Standard-mode | 0 | - | µs |
| | | | Fast-mode | 0 | - | µs |
| | | | Fast-mode Plus | 0 | - | µs |
| $t_{SU;DAT}$ | data set-up time | [9][10] | Standard-mode | 250 | - | ns |
| | | | Fast-mode | 100 | - | ns |
| | | | Fast-mode Plus | 50 | - | ns |

[1] Guaranteed by design. Not tested in production.

[2] Parameters are valid over operating temperature range unless otherwise specified. See the I²C-bus specification *UM10204* for details.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH}$(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] $C_b$ = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

**Table 30. Dynamic characteristics: I²S-bus interface pins [1][4]**

*$T_{amb}$ = −40 °C to 105 °C; $V_{DD}$ = 1.62 V to 3.6 V; $C_L$ = 30 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.*

| Symbol | Parameter | Conditions | | Min | Typ[3] | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Master; 1.62 V ≤ VDD ≤ 2.0 V** | | | | | | | |
| $t_{v(Q)}$ | data output valid time | on pin I2Sx_TX_SDA | [2] | | | | |
| | | CCLK = 1 MHz to 12 MHz | | 32.7 | - | 56.6 | ns |
| | | CCLK = 48 MHz to 60 MHz | | 29.9 | - | 48.9 | ns |
| | | CCLK = 96 MHz | | 29.0 | - | 47.2 | ns |
| | | on pin I2Sx_WS | | | | | |
| | | CCLK = 1 MHz to 12 MHz | | 35.1 | - | 61.1 | ns |
| | | CCLK = 48 MHz to 60 MHz | | 31.9 | - | 51.8 | ns |
| | | CCLK = 96 MHz | | 31.0 | - | 49.7 | ns |
| $t_{su(D)}$ | data input set-up time | on pin I2Sx_RX_SDA | [2] | | | | |
| | | CCLK = 1 MHz to 12 MHz | | 0.0 | - | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 0.0 | - | - | ns |
| | | CCLK = 96 MHz | | 0.0 | - | - | ns |
| $t_{h(D)}$ | data input hold time | on pin I2Sx_RX_SDA | [2] | | | | |
| | | CCLK = 1 MHz to 12 MHz | | 0.0 | - | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 0.0 | - | - | ns |
| | | CCLK = 96 MHz | | 0.0 | - | - | ns |
| **Slave; 1.62 V ≤ VDD ≤ 2.0 V** | | | | | | | |
| $t_{v(Q)}$ | data output valid time | on pin I2Sx_TX_SDA | [2] | | | | |
| | | CCLK = 1 MHz to 12 MHz | | 25.8 | - | 47.0 | ns |
| | | CCLK = 48 MHz to 60 MHz | | 23.0 | - | 38.9 | ns |
| | | CCLK = 96 MHz | | 22.2 | - | 37.1 | ns |
| $t_{su(D)}$ | data input set-up time | on pin I2Sx_RX_SDA | [2] | | | | |
| | | CCLK = 1 MHz to 12 MHz | | 0.0 | - | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 0.0 | - | - | ns |
| | | CCLK = 96 MHz | | 0.0 | - | - | ns |
| | | on pin I2Sx_RX_WS | | | | | |
| | | CCLK = 1 MHz to 12 MHz | | 0.0 | - | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 0.0 | - | - | ns |
| | | CCLK = 96 MHz | | 0.0 | - | - | ns |
| $t_{h(D)}$ | data input hold time | on pin I2Sx_RX_SDA | [2] | | | | |
| | | CCLK = 1 MHz to 12 MHz | | 1.0 | - | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 1.0 | - | - | ns |
| | | CCLK = 96 MHz | | 1.0 | - | - | ns |
| | | on pin I2Sx_RX_WS | | | | | |
| | | CCLK = 1 MHz to 12 MHz | | 2.0 | - | - | ns |
| | | CCLK = 48 MHz to 60 MHz | | 2.0 | - | - | ns |
| | | CCLK = 96 MHz | | 2.0 | - | - | ns |

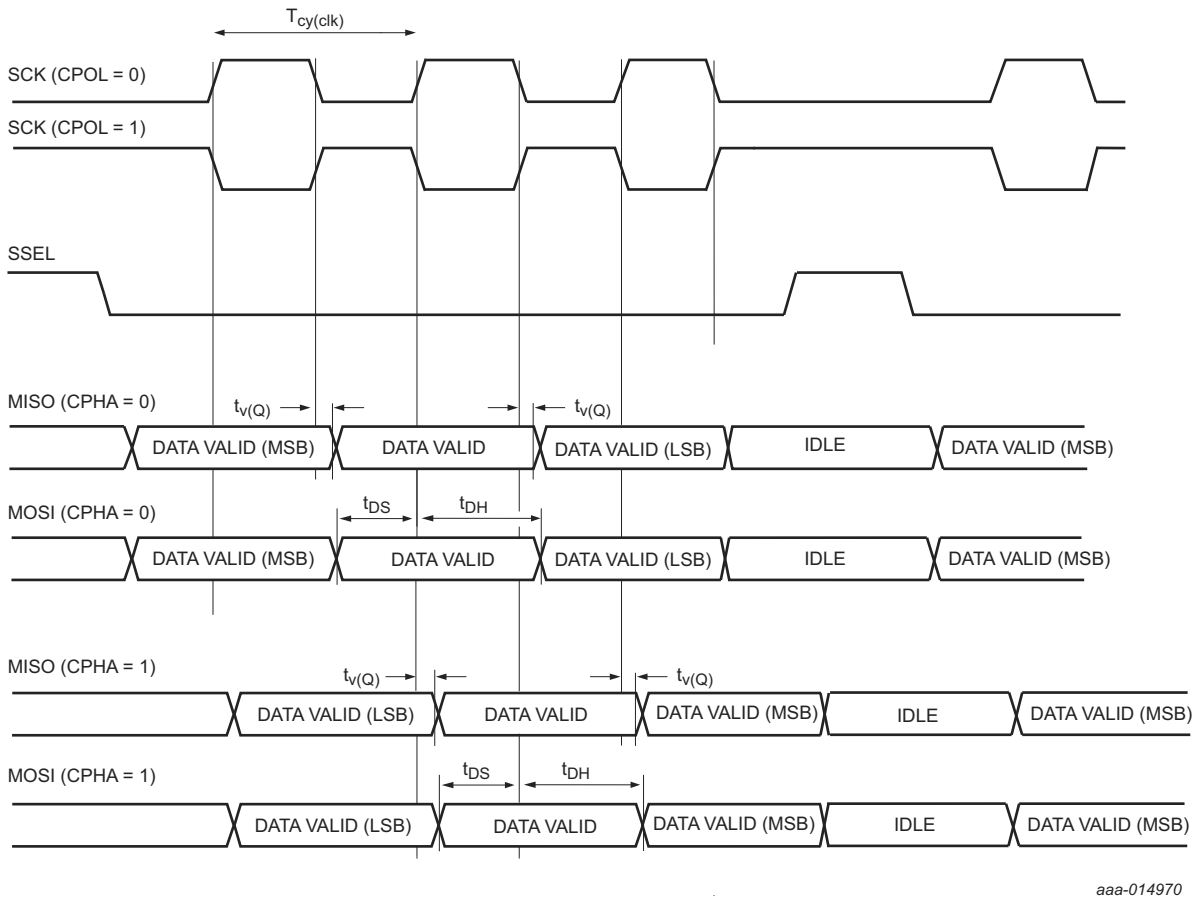
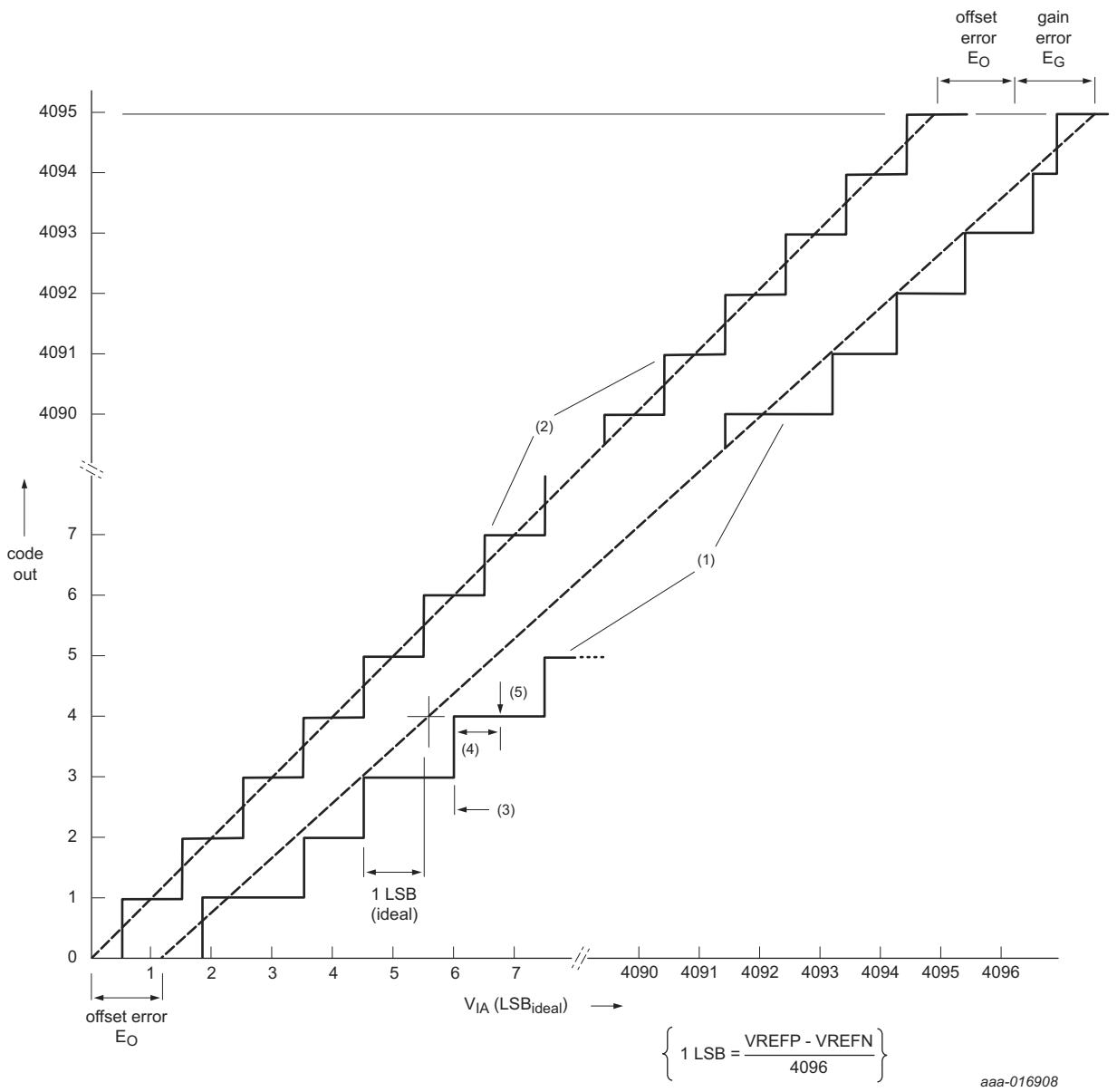



**Fig 23. SPI slave timing**

[8] The full-scale error voltage or gain error ($E_G$) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 27.

[9] $T_{amb}$ = 25 °C; maximum sampling frequency $f_s$ = 5.0 Msamples/s and analog input capacitance $C_{ia}$ = 5 pF.

[10] Input impedance $Z_i$ is inversely proportional to the sampling frequency and the total input capacity including $C_{ia}$ and $C_{io}$: $Z_i \propto 1 / (f_s \times C_i)$. See Table 20 for $C_{io}$. See Figure 28.




(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error ($E_D$).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

**Fig 27. 12-bit ADC characteristics**

**Table 38. ADC sampling times** *...continued*[1]

*$T_{amb}$ = -40 °C to 85 °C; 1.62 V ≤ $V_{DDA}$ ≤ 3.6 V; 1.62 V ≤ $V_{DD}$ ≤ 3.6 V*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 10 bit** | | | | | | | |
| $t_s$ | sampling time | $Z_o$ < 0.05 kΩ | [3] | 35 | - | - | ns |
| | | 0.05 kΩ ≤ $Z_o$ < 0.1 kΩ | | 38 | - | - | ns |
| | | 0.1 kΩ ≤ $Z_o$ < 0.2 kΩ | | 40 | - | - | ns |
| | | 0.2 kΩ ≤ $Z_o$ < 0.5 kΩ | | 46 | - | - | ns |
| | | 0.5 kΩ ≤ $Z_o$ < 1 kΩ | | 61 | - | - | ns |
| | | 1 kΩ ≤ $Z_o$ < 5 kΩ | | 86 | - | - | ns |
| **ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 8 bit** | | | | | | | |
| $t_s$ | sampling time | $Z_o$ < 0.05 kΩ | [3] | 27 | - | - | ns |
| | | 0.05 kΩ ≤ $Z_o$ < 0.1 kΩ | | 29 | - | - | ns |
| | | 0.1 kΩ ≤ $Z_o$ < 0.2 kΩ | | 32 | - | - | ns |
| | | 0.2 kΩ ≤ $Z_o$ < 0.5 kΩ | | 36 | - | - | ns |
| | | 0.5 kΩ ≤ $Z_o$ < 1 kΩ | | 48 | - | - | ns |
| | | 1 kΩ ≤ $Z_o$ < 5 kΩ | | 69 | - | - | ns |
| **ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 6 bit** | | | | | | | |
| $t_s$ | sampling time | $Z_o$ < 0.05 kΩ | [3] | 20 | - | - | ns |
| | | 0.05 kΩ ≤ $Z_o$ < 0.1 kΩ | | 22 | - | - | ns |
| | | 0.1 kΩ ≤ $Z_o$ < 0.2 kΩ | | 23 | - | - | ns |
| | | 0.2 kΩ ≤ $Z_o$ < 0.5 kΩ | | 26 | - | - | ns |
| | | 0.5 kΩ ≤ $Z_o$ < 1 kΩ | | 36 | - | - | ns |
| | | 1 kΩ ≤ $Z_o$ < 5 kΩ | | 51 | - | - | ns |

[1] Characterized through simulation. Not tested in production.

[2] The ADC default sampling time is 2.5 ADC clock cycles. To match a given analog source output impedance, the sampling time can be extended by adding up to seven ADC clock cycles for a maximum sampling time of 9.5 ADC clock cycles. See the TSAMP bits in the ADC CTRL register.

[3] $Z_o$ = analog source output impedance.

### 12.2.1 ADC input impedance

Figure 28 shows the ADC input impedance. In this figure:

- ADCx represents slow ADC input channels 6 to 11.
- ADCy represents fast ADC input channels 0 to 5.
- $R_1$ and $R_{sw}$ are the switch-on resistance on the ADC input channel.
- If fast channels (ADC inputs 0 to 5) are selected, the ADC input signal goes through $R_{sw}$ to the sampling capacitor ($C_{ia}$).
- If slow channels (ADC inputs 6 to 11) are selected, the ADC input signal goes through $R_1$ + $R_{sw}$ to the sampling capacitor ($C_{ia}$).
- Typical values, $R_1$ = 487 Ω, $R_{sw}$ = 278 Ω
- See Table 20 for $C_{io}$.
- See Table 37 for $C_{ia}$.

### 13.5.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

## 13.6 Suggested USB interface solutions

The USB device can be connected to the USB as self-powered device (see Figure 34) or bus-powered device (see Figure 35).

On the LPC5411x, the USB_VBUS pin is 5 V tolerant only when $V_{DD}$ is applied and at operating voltage level. Therefore, if the USB_VBUS function is connected to the USB connector and the device is self-powered, the USB_VBUS pin must be protected for situations when $V_{DD}$ = 0 V.

If $V_{DD}$ is always at operating level while VBUS = 5 V, the USB_VBUS pin can be connected directly to the VBUS pin on the USB connector.

For systems where $V_{DD}$ can be 0 V and VBUS is directly applied to the VBUS pin, precautions must be taken to reduce the voltage to below 3.6 V, which is the maximum allowable voltage on the USB_VBUS pin in this case.

One method is to use a voltage divider to connect the USB_VBUS pin to the VBUS on the USB connector. The voltage divider ratio should be such that the USB_VBUS pin is greater than 0.7 $V_{DD}$ to indicate a logic HIGH while below the 3.6 V allowable maximum voltage.

For the following operating conditions

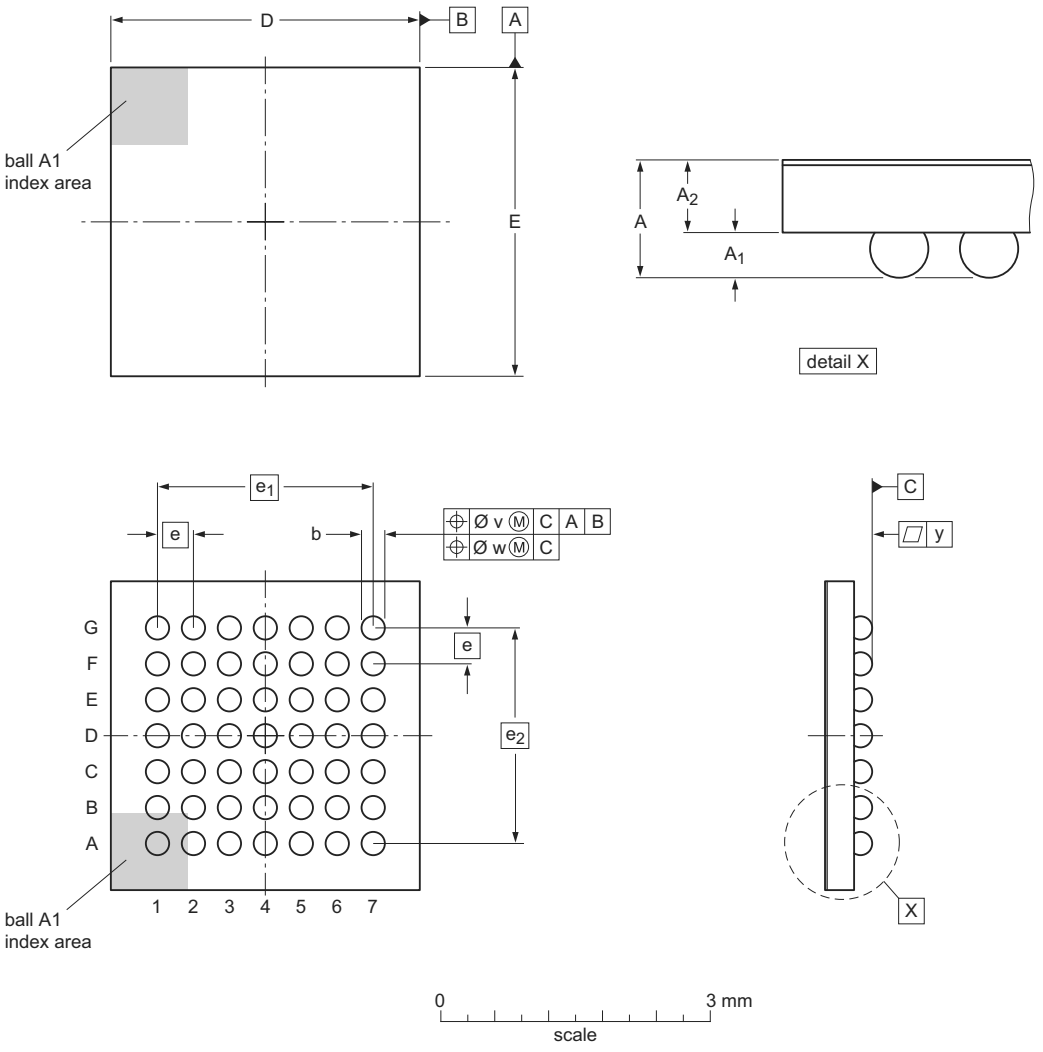
$VBUS_{max}$ = 5.25 V

$V_{DD}$ = 3.6 V,

the voltage divider should provide a reduction of 3.6 V/5.25 V or ~0.686 V.

# 14. Package outline

**WLCSP49: wafer level chip-scale package; 49 bumps; 3.44 x 3.44 x 0.525 mm (Backside coating included)** **SOT1444-5**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_1$ | $A_2$ | b | D | E | e | $e_1$ | $e_2$ | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.565 | 0.23 | 0.350 | 0.29 | 3.47 | 3.47 | 0.4 | 2.4 | 2.4 | 0.05 | 0.015 | 0.03 |
| | nom | 0.525 | 0.20 | 0.325 | 0.26 | 3.44 | 3.44 | | | | | | |
| | min | 0.485 | 0.17 | 0.300 | 0.23 | 3.41 | 3.41 | | | | | | |

Note
Backside coating 25 µm

*sot1444-5_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1444-5 | | - - - | | | | ~~15-01-30~~ 16-01-20 |

**Fig 36. WLCSP49 Package outline**

**Table 43. Revision history** *...continued*

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC5411x v.1.4 | 20160711 | Product data sheet | - | LPC5411x v.1.3 |
| Modifications: | • Updated Table 16 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”. Added Max values to $I_{DD}$ supply current in deep-sleep mode and deep power-down mode.<br>• Updated Table 17 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”. Added Max values for deep-sleep mode and deep power-down mode.<br>• Updated Table 30 “Dynamic characteristics: I2S-bus interface pins [1][4]”.<br>• Updated Table 31 “SPI dynamic characteristics[1]”.<br>• Updated Table 32 “USART dynamic characteristics[1]”.<br>• Updated Table 5 “Termination of unused pins”. Added USB_DP and USB_DM.<br>• Updated USART features: Maximum bit rates of 6.25 Mbit/s in asynchronous mode and Maximum data rate of 20 Mbit/s in synchronous master mode and 16 Mbit/s in synchronous slave mode.See Section 7.17.4.<br>• Added a remark to the features of Section 7.17.5 “SPI serial I/O controller”.<br>• Updated SPIO features. Added maximum and minimum data rates for SPI functions in master mode and slave mode. See Section 7.17.5.<br>• Updated Figure 8 “LPC5411x clock generation”.<br>• Added a table note to Table 16 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”: [3] Guaranteed by characterization, not tested in production. VDD = 2.0 V.<br>• PLL section renamed to System PLL. See Section 11.4 “System PLL”.<br>• Added Section 13.1 “Start-up behavior”.<br>• Updated Figure 31 “Standard I/O and RESET pin configuration”.<br>• Added Section 13.6 “Suggested USB interface solutions”.<br>• Added Table 39 “Temperature sensor static and dynamic characteristics”.<br>• Added Figure 29 “LLS fit of the temperature sensor output voltage”.<br>• Updated Table 30 “Dynamic characteristics: I2S-bus interface pins [1][4]”: common to input and output, $t_{WH}$ and $t_{WL}$ typical values.<br>• Added a remark to the features of Section 7.17.8 “I2S-bus interface”.<br>• Updated Table 19 “Typical AHB/APB peripheral power consumption [3][4][5]”:<br>– USB, GPIO0, MAILBOX, SCTimer/PWM, PINT, RTC for: CPU: 12 MHz, sync APB bus: 12 MHz.<br>– GPIO0 and GINT for: CPU: 96MHz, sync APB bus: 96 MHz.<br>– GINT for: CPU: 48 MHz, sync APB bus: 48 MHz.<br>• Removed the section: Power-up ramp conditions.<br>• Updated Table 25 “Dynamic characteristics of the PLL[1]”:<br>– $f_{ref}$ changed to $F_{in}$; reference frequency to input frequency.<br>– removed $f_{refjitter}$.<br>• Updated Table 30 “Dynamic characteristics: I2S-bus interface pins [1][4]”<br>– removed rise time ($t_r$) and fall time ($t_f$). | | | |