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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0+
Core Size	32-Bit Dual-Core
Speed	100MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54113j256bd64ql

- The Micro-Tick Timer running from the watchdog oscillator can be used to wake-up the device from any reduced power modes.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.

- Single power supply 1.62 V to 3.6 V.
- JTAG boundary scan supported.
- 128 bit unique device serial number for identification.
- Operating temperature range −40 °C to +105 °C.
- Available as WLCSP49 and LQFP64 packages.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54113J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.436 x 3.436 x 0.525 mm	-
LPC54114J256UK49	WLCSP49	wafer level chip-size package; 49 (7 x 7) bumps; 3.436 x 3.436 x 0.525 mm	-
LPC54113J128BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54113J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC54114J256BD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

3.1 Ordering options

Table 2. Ordering options

Type number	Flash in KB	SRAM in KB					Cortex-M4 with FPU	Cortex-M0+	USB FS	GPIO
		SRAMX	SRAM0	SRAM1	SRAM2	Total				
LPC54113J256UK49	256	32	64	64	32	192	1	0	1	37
LPC54114J256UK49	256	32	64	64	32	192	1	1	1	37
LPC54113J128BD64	128	32	64	-	-	96	1	0	1	48
LPC54113J256BD64	256	32	64	64	32	192	1	0	1	48
LPC54114J256BD64	256	32	64	64	32	192	1	1	1	48

4. Marking

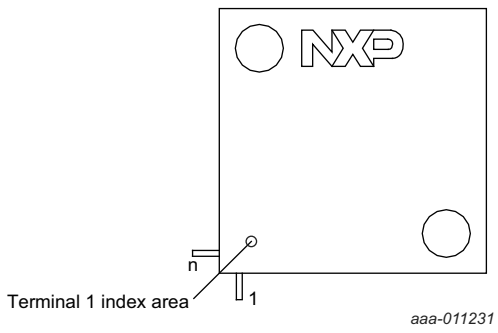


Fig 1. LQFP64 package marking

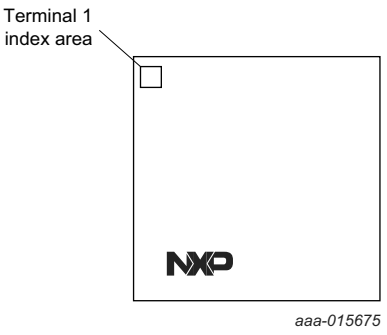


Fig 2. WLCSP49 package marking

The LPC5411x LQFP64 package has the following top-side marking:

- First line: LPC5411xJyyy
  - x: 4 = dual core (M4, M0+)
  - x: 3 = single core (M4)
  - yyy: flash size
- Second line: BD64
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = Boot code version and device revision.

The LPC5411x WLCSP49 package has the following top-side marking:

- First line: LPC5411x
  - x: 4 = dual core (M4, M0+)
  - x: 3 = single core (M4)
- Second line: JxxxUK49
  - xxx: flash size
- Third line: xxxxxxxx
- Fourth line: xxxyyww
  - yyww: Date code with yy = year and ww = week.
- Fifth line: xxxxx
- Sixth line: NXP x[R]x
  - xR = Boot code version and device revision.

Table 3. Device revision table

	Revision description
'0A'	Initial device revision with boot code version 18.0.

Table 4. Pin description *…continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
VREFN	-	21		-	-	ADC negative reference voltage.
V_{DDA}	A4	23		-	-	Analog supply voltage.
V_{DD}	C4, F4	8, 24, 34, 56		-	-	Single 1.62 V to 3.6 V power supply powers internal digital functions and I/Os.
V_{SS}	D4, E4	9, 25, 55		-	-	Ground.
V_{SSA}	A3	20		-	-	Analog ground.

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 31. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

7.6 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- 40 vectored interrupt slots.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table using Vector Table Offset Register (VTOR).
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.7 Nested Vectored Interrupt Controller (NVIC) for Cortex-M0+

The NVIC is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.7.1 Features

- Controls system exceptions and peripheral interrupts.
- 32 vectored interrupt slots.
- Four programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table using VTOR.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.7.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.12 Memory mapping

The LPC5411x incorporates several distinct memory regions. The APB peripheral area is 64 KB in size and is divided to allow for up to 32 peripherals. Each peripheral is allocated 4 KB of space simplifying the address decoding.

Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset.

generates an RTC wake-up interrupt request, which can wake up the part. During deep power-down mode, the contents of the SRAM and registers are not retained. All functional pins are tri-stated in deep power-down mode.

Table 8 shows the peripheral configuration in reduced power modes.

Table 8. Peripheral configuration in reduced power modes

Peripheral	Reduced power mode		
	Sleep	Deep-sleep	Deep power-down
FRO	Software configured	Software configured	Off
Flash	Software configured	Standby	Off
BOD	Software configured	Software configured	Off
PLL	Software configured	Off	Off
Watchdog osc and WWDT	Software configured	Software configured	Off
Micro-tick Timer	Software configured	Software configured	Off
DMA	Active	Configurable some for operations, see Section 7.13.2	Off
USART	Software configured	Off; but can create a wake-up interrupt in synchronous slave mode or 32 kHz clock mode	Off
SPI	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
I2C	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
USB	Software configured	Software configured	Off
DMIC	Software configured	Software configured	Off
Other digital peripherals	Software configured	Off	Off
RTC oscillator	Software configured	Software configured	Software configured

Table 9 shows the wake-up sources for reduced power modes.

Table 9. Wake-up sources for reduced power modes

Power mode	Wake-up source	Conditions
Sleep	Any interrupt	Enable interrupt in NVIC.
	HWWAKE	Certain Flexcomm Interface and DMIC subsystem activity.

7.16 General Purpose I/O (GPIO)

The LPC5411x provides two GPIO ports with a total of 48 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

See Table 4 for the default state on reset.

7.16.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set, clear, and toggle registers allow a single instruction set, clear or toggle of any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request.
- One GPIO group interrupt can be triggered by a combination of any pin or pins.

7.17 Pin interrupt/pattern engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can be used in conjunction with software to create complex state machines based on pin inputs. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the I/O+ bus for fast single-cycle access.

7.17.1 Features

- Pin interrupts:
  - Up to eight pins can be selected from all GPIO pins on ports 0 and 1 as edge-sensitive or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Pin interrupts can wake up the device from sleep mode and deep-sleep mode.
- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

7.18 AHB peripherals

7.18.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.18.1.1 Features

- 20 channels, 19 of which are connected to peripheral DMA requests. These come from the Flexcomm Interfaces (USART, SPI, I^2C, and I2S) and digital microphone interfaces.
- DMA operations can be triggered by on-chip or off-chip events.
- Priority is user selectable for each channel (up to eight priority levels).
- Continuous priority arbitration.
- Address cache with four entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

- No chip clocks are required in order to receive and compare an address as a Slave, so this event can wake up the device from deep-sleep mode.

7.19.8 I²S-bus interface

The I²S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I²S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer as well as other configurations. In the LPC5411x, the I²S function is included in Flexcomm Interface 6 and Flexcomm Interface 7. Each of these Flexcomm Interfaces implement four I²S channel pairs.

The I²S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a master or a slave. Other channel pairs, if present, always operate as slaves. All of the channel pairs within one Flexcomm Interface share one set of I²S signals, and are configured together for either transmit or receive operation, using the same mode, same data configuration and frame configuration. All such channel pairs can participate in a time division multiplexing (TDM) arrangement. For cases requiring an MCLK input and/or output, this is handled outside of the I²S block in the system level clocking scheme.

7.19.8.1 Features

- A Flexcomm Interface may implement one or more I²S channel pairs, the first of which could be a master or a slave, and the rest of which would be slaves. All channel pairs are configured together for either transmit or receive and other shared attributes. The number of channel pairs is defined for each Flexcomm Interface, and may be from 0 to 4.
- Configurable data size for all channels within one Flexcomm Interface, from 4 bits to 32 bits. Each channel pair can also be configured independently to act as a single channel (mono as opposed to stereo operation).
- All channel pairs within one Flexcomm Interface share a single bit clock (SCK) and word select/frame trigger (WS), and data line (SDA).
- Data for all I²S traffic within one Flexcomm Interface uses the Flexcomm Interface FIFO. The FIFO depth is 8 entries.
- Left justified and right justified data modes.
- DMA support using FIFO level triggering.
- TDM (Time Division Multiplexing) with a several stereo slots and/or mono slots is supported. Each channel pair can act as any data slot. Multiple channel pairs can participate as different slots on one TDM data line.
- The bit clock and WS can be selectively inverted.
- Sampling frequencies supported depends on the specific device configuration and applications constraints (e.g. system clock frequency, PLL availability, etc.) but generally supports standard audio data rates. See the data rates section in I2S chapter (UM10914) to calculate clock and sample rates.

Remark: The Flexcomm Interface function clock frequency should not be above 48 MHz.

- PWM features:
  - Counters can be used in conjunction with match registers to toggle outputs and create time-proportioned PWM signals.
  - Up to eight single-edge or four dual-edge PWM outputs with independent duty cycle and common PWM cycle length.
- Event creation features:
  - The following conditions define an event: a counter match condition, an input (or output) condition such as an rising or falling edge or level, a combination of match and/or input/output condition.
  - Selected events can limit, halt, start, or stop a counter or change its direction.
  - Events trigger state changes, output toggles, interrupts, and DMA transactions.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- State control features:
  - A state is defined by events that can happen in the state while the counter is running.
  - A state changes into another state as a result of an event.
  - Each event can be assigned to one or more states.
  - State variable allows sequencing across multiple counter cycles.

7.20.3 Windowed WatchDog Timer (WWDT)

The purpose of the Watchdog Timer is to reset or interrupt the microcontroller within a programmable time if it enters an erroneous state. When enabled, a watchdog reset is generated if the user program fails to feed (reload) the Watchdog within a predetermined amount of time.

7.20.3.1 Features

- Internally resets chip if not reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Programmable 24-bit timer with internal fixed pre-scaler.
- Selectable time period from 1,024 watchdog clocks ($T_{WDCLK} \times 256 \times 4$) to over 67 million watchdog clocks ($T_{WDCLK} \times 2^{24} \times 4$) in increments of four watchdog clocks.
- “Safe” watchdog operation. Once enabled, requires a hardware reset or a Watchdog reset to be disabled.
- Incorrect feed sequence causes immediate watchdog event if enabled.
- The watchdog reload value can optionally be protected such that it can only be changed after the “warning interrupt” time is reached.
- Flag to indicate Watchdog reset.

- The Watchdog clock (WDCLK) source is a selectable frequency in the range of 6 kHz to 1.5 MHz. The accuracy of this clock is limited to +/- 40% over temperature, voltage, and silicon processing variations.
- The Watchdog timer can be configured to run in deep-sleep mode.
- Debug mode.

7.20.4 RTC timer

The RTC block has two timers: main RTC timer, and high-resolution/wake-up timer. The main RTC timer is a 32-bit timer that uses a 1 Hz clock and is intended to run continuously as a real-time clock. When the timer value reaches a match value, an interrupt is raised. The alarm interrupt can also wake up the part from any low power mode, if enabled.

The high-resolution or wake-up timer is a 16-bit timer that uses a 1 kHz clock and operates as a one-shot down timer. When the timer is loaded, it starts counting down to 0 at which point an interrupt is raised. The interrupt can be used to wake-up the part from any low power modes. This timer is intended to be used for timed wake-up from deep-sleep or deep power-down modes. The high-resolution wake-up timer can be disabled to conserve power if not used.

The RTC timer uses the 32.768 kHz clock input to create a 1 Hz or 1 kHz clock.

7.20.4.1 Features

- The RTC oscillator has the following clock outputs:
  - 32.768 kHz clock, selectable for system clock and CLKOUT pin.
  - 1 Hz clock for RTC timing.
  - 1 kHz clock for high-resolution RTC timing.
- 32-bit, 1 Hz RTC counter and associated match register for alarm generation.
- Separate 16-bit high-resolution/wake-up timer clocked at 1 kHz for 1 ms resolution with a more that one minute maximum time-out period.
- RTC alarm and high-resolution/wake-up timer time-out each generate independent interrupt requests. Either time-out can wake up the part from any of the low power modes, including deep power-down.

7.20.5 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.20.5.1 Features

- 24-bit interrupt timer.
- Four channels independently counting down from individually set values.
- Repeat interrupt, one-shot interrupt, and one-shot bus stall modes.

[8] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

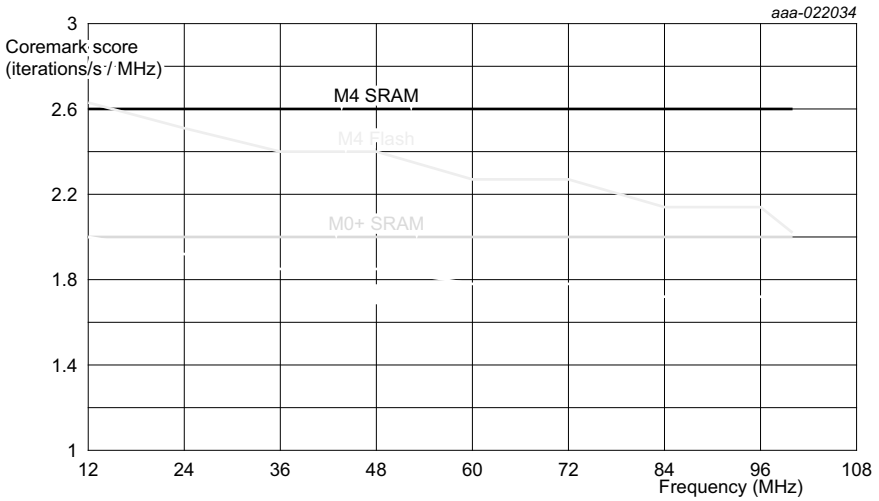
$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 11. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
LQFP64 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	58 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	81 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		18 ± 15 %	°C/W
WLCSP49 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	41 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		0.3 ± 15 %	°C/W



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; See the FLASHCFG register in the LPC5411x, UM10914 User Manual for system clock flash access time settings. Measured with Keil uVision 5.17. Optimization level 3, optimized for time ON.

12 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.

24 MHz, 36 MHz, 60 MHz, 72 MHz, 84 MHz, and 100 MHz: FRO enabled; PLL enabled.

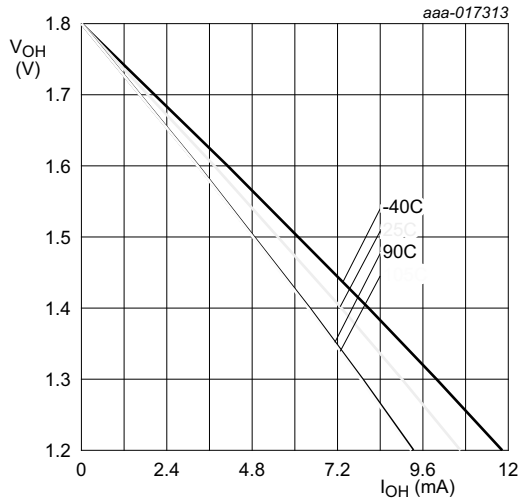
Fig 9. Typical CoreMark score

10.4 Pin characteristics

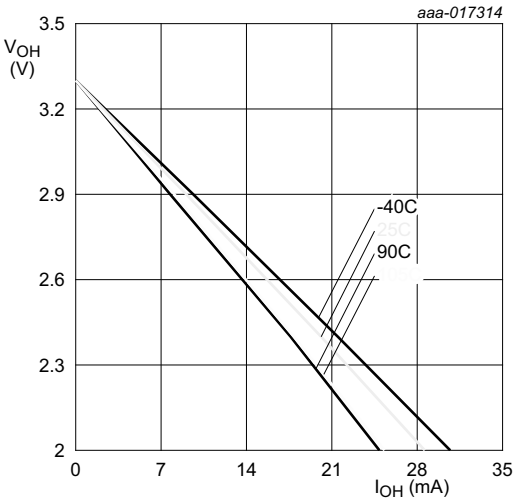
Table 20. Static characteristics: pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
RESET pin							
V_{IH}	HIGH-level input voltage			0.8 × V_{DD}	-	5.0	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage		[1][14]	0.05 × V_{DD}	-	-	V
Standard I/O pins							
Input characteristics							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled.		-	3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; V_{DD} = 3.6 V; for RESETN pin.			3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	3.0	180	nA
V_I	input voltage	pin configured to provide a digital function;	[3]				
		V_{DD} > 1.8 V		0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_{IH}	HIGH-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		1.5	-	5.0	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		2.0	-	5.0	V
V_{IL}	LOW-level input voltage	1.62 V ≤ V_{DD} < 2.7 V		−0.5	-	+0.4	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		[14]	0.1 × V_{DD}	-	-	V
Output characteristics							
V_O	output voltage	output active		0	-	V_{DD}	V
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/pull-down resistors disabled		-	3	180	nA
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA; 1.62 V ≤ V_{DD} < 2.7 V		V_{DD} − 0.4	-	-	V
		I_{OH} = −6 mA; 2.7 V ≤ V_{DD} ≤ 3.6 V		V_{DD} − 0.4			
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 1.62 V ≤ V_{DD} < 2.7 V		-	-	0.4	V
		I_{OL} = 6 mA; 2.7 V ≤ V_{DD} ≤3.6 V		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 1.62 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OH} = V_{DD} − 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 1.62 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OL} = 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	1.62 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	35	mA
	drive HIGH; connected to ground;	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	87	mA

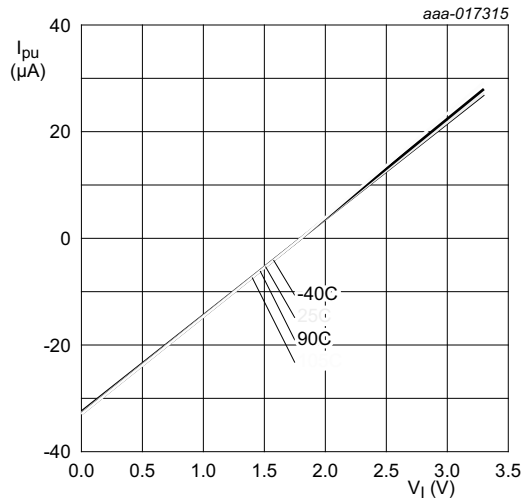


Conditions: V_{DD} = 1.8 V; on standard port pins.

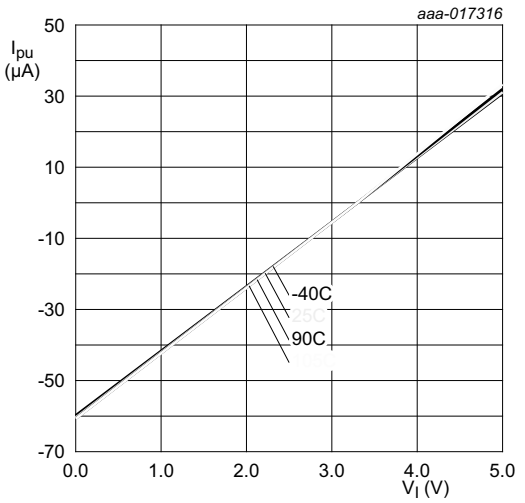


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 16. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 1.8 V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 17. Typical pull-up current I_{PU} versus input voltage V_I

Table 25. Dynamic characteristics of the PLL[1]

T_{amb} = −40 °C to +105 °C. V_{DD} = 1.62 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency	-		32.768 kHz	-	25 MHz	-
Clock output							
f_o	output frequency	for PLL clkout output	[2]	1.2	-	150	MHz
d_o	output duty cycle	for PLL clkout output		46	-	54	%
f_{CCO}	CCO frequency	-		-	-	150	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion	-	[3]	1	2	4	ns
Dynamic parameters at f_{out} = f_{CCO} = 100 MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	f_{ref} = 10 MHz	[4][5]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[4][5]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[4] Actual jitter dependent on amplitude and spectrum of substrate noise.

[5] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.5 FRO

The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.

Table 26. Dynamic characteristic: FRO

T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Min[2]	Typ[1]	Max[2]	Unit
$f_{osc(FRO)}$	FRO clock frequency	11.88	12	12.12	MHz
$f_{osc(FRO)}$	FRO clock frequency	47.52	48	48.48	MHz
$f_{osc(FRO)}$	FRO clock frequency	95.04	96	96.96	MHz

[1] Tested in production.The values listed are at room temperature (25 °C).

[2] Data based on characterization results, not tested in production.

11.6 RTC oscillator

See Section 13.5 for connecting the RTC oscillator to an external clock source.

Table 27. Dynamic characteristic: RTC oscillator

T_{amb} = −40 °C to +105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V[1]

Symbol	Parameter	Min	Typ	Max	Unit
f_i	input frequency	-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

Table 32. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.62 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW set to standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
USART slave (in synchronous mode) 2.7 V ≤ V_{DD} ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK = 1 MHz to 12 MHz	2	-	-	ns
		CCLK = 48 MHz to 60 MHz	1	-	-	ns
		CCLK = 96 MHz	1	-	-	ns
$t_{h(D)}$	data input hold time	CCLK = 1 MHz to 12 MHz	2	-	-	ns
		CCLK = 48 MHz to 60 MHz	1	-	-	ns
		CCLK = 96 MHz	1	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK = 1 MHz to 12 MHz	19	-	42	ns
		CCLK = 48 MHz to 60 MHz	14	-	31	ns
		CCLK = 96 MHz	13	-	28	ns

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed.

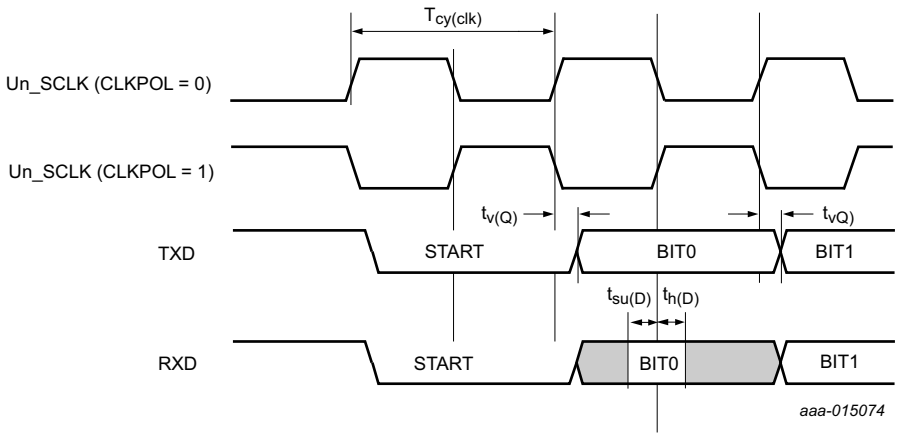


Fig 24. USART timing

11.12 SCTimer/PWM output timing

Table 33. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.62 V ≤ V_{DD} ≤ 3.6 V C_L = 30 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at 10 % and 90 % of the signal level; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	-	-	2.7	ns

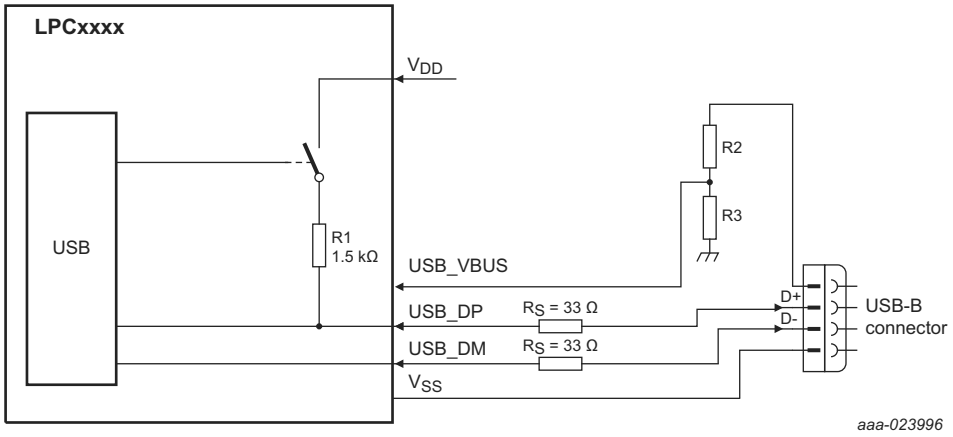
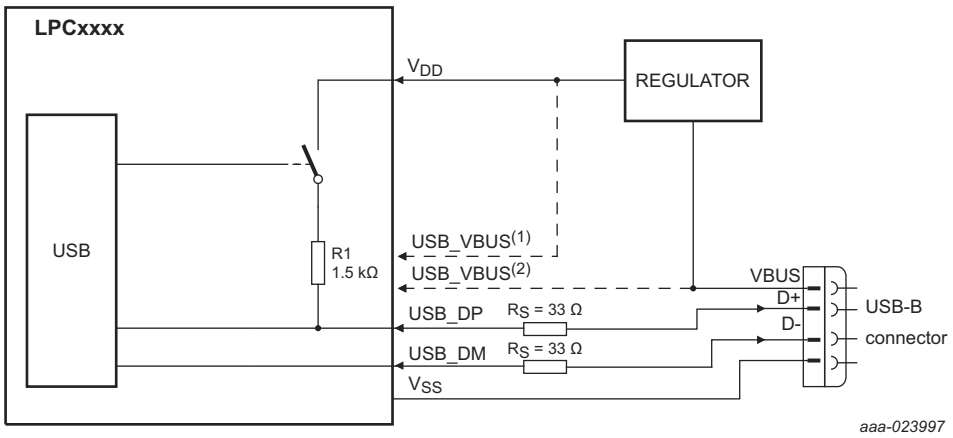


Fig 34. USB interface on a self-powered device where USB_VBUS = 5 V

The internal pull-up (1.5 kΩ) can be enabled by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required.



Two options exist for connecting VBUS to the USB_VBUS pin:

(1) Connect the regulator output to USB_VBUS. In this case, the USB_VBUS signal is HIGH whenever the part is powered.

(2) Connect the VBUS signal directly from the connector to the USB_VBUS pin. In this case, 5 V are applied to the USB_VBUS pin while the regulator is ramping up to supply V_{DD}. Since the USB_VBUS pin is only 5 V tolerant when V_{DD} is at operating level, this connection can degrade the performance of the part over its lifetime. Simulation shows that lifetime is reduced to 15 years at T_{amb} = 45 °C and 8 years at T_{amb} = 55 °C assuming that USB_VBUS = 5 V is applied continuously while V_{DD} = 0 V.

Fig 35. USB interface on a bus-powered device

Table 43. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Updated Section 2 “Features and benefits”: deleted text: Real-Time Clock (RTC) running from the 32.768 kHz clock from the list item: The Micro-Tick Timer running from the watchdog oscillator can be used to wake-up the device from any reduced power modes. See • Removed code executing in flash and SRAM from deep-sleep mode in Table 23 “Dynamic characteristic: Typical wake-up times from low power modes”. • Updated Table 13 “CoreMark score”: In ARM Cortex-M4 in active mode; ARM Cortex-M0+ in sleep mode, changed CCLK = 96 MHz; 5 system clock flash access time to CCLK = 96 MHz; 6 system clock flash access time. In ARM Cortex-M0+ in active mode; ARM Cortex-M4 in sleep mode, changed CCLK = 96 MHz; 5 system clock flash access time to CCLK = 96 MHz; 6 system clock flash access time. • Added text in Section 2 “Features and benefits” and Section 7.11 “On-chip ROM”: ROM based USB drivers (HID, CDC, MSC, DFU). • Replaced list item in ROM API support in Section 2 “Features and benefits” and Section 7.11 “On-chip ROM”: Legacy, Single, and Dual image boot. • Changed text in clock generation in Section 2 “Features and benefits”, Section 7.18.3.1 “Features”, and Section 7.21.1.2 “Watchdog oscillator (WDTOSC)”: was, Watchdog oscillator (WDTOSC) with a frequency range of 200 kHz to 1.5 MHz, now, Watchdog oscillator (WDTOSC) with a frequency range of 6kHz to 1.5 MHz. • Updated Table 28 “Dynamic characteristics: Watchdog oscillator”. The min value of internal watchdog oscillator frequency is 6 kHz. • Updated Section 7.13.2 “Deep-sleep mode”. • Updated Table 7 “Peripheral configuration in reduced power modes” and added Table 8 “Wake-up sources for reduced power modes”. • Updated Figure 32 “Power, clock, and debug connections”. • Updated Figure 34 “USB interface on a self-powered device where USB_VBUS = 5 V” and Figure 35 “USB interface on a bus-powered device”.			
LPC5411x v.1.5	20160718	Product data sheet	-	LPC5411x v.1.4
Modifications:	• Updated Table 16 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”: IDD typical values at deep-sleep mode, flash is powered down.			