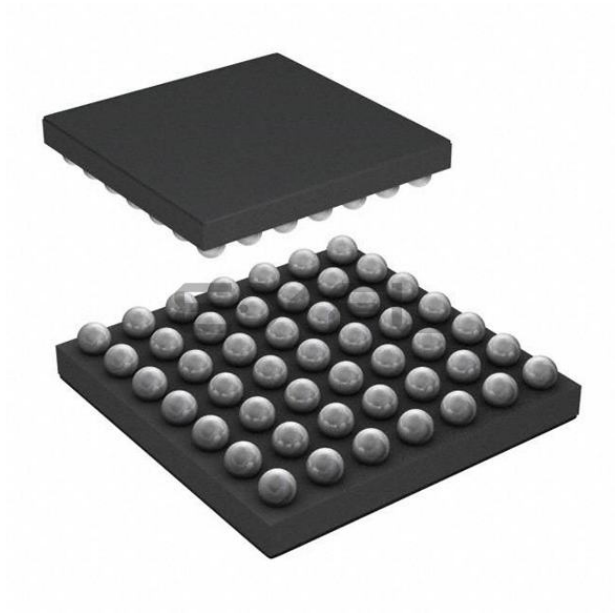

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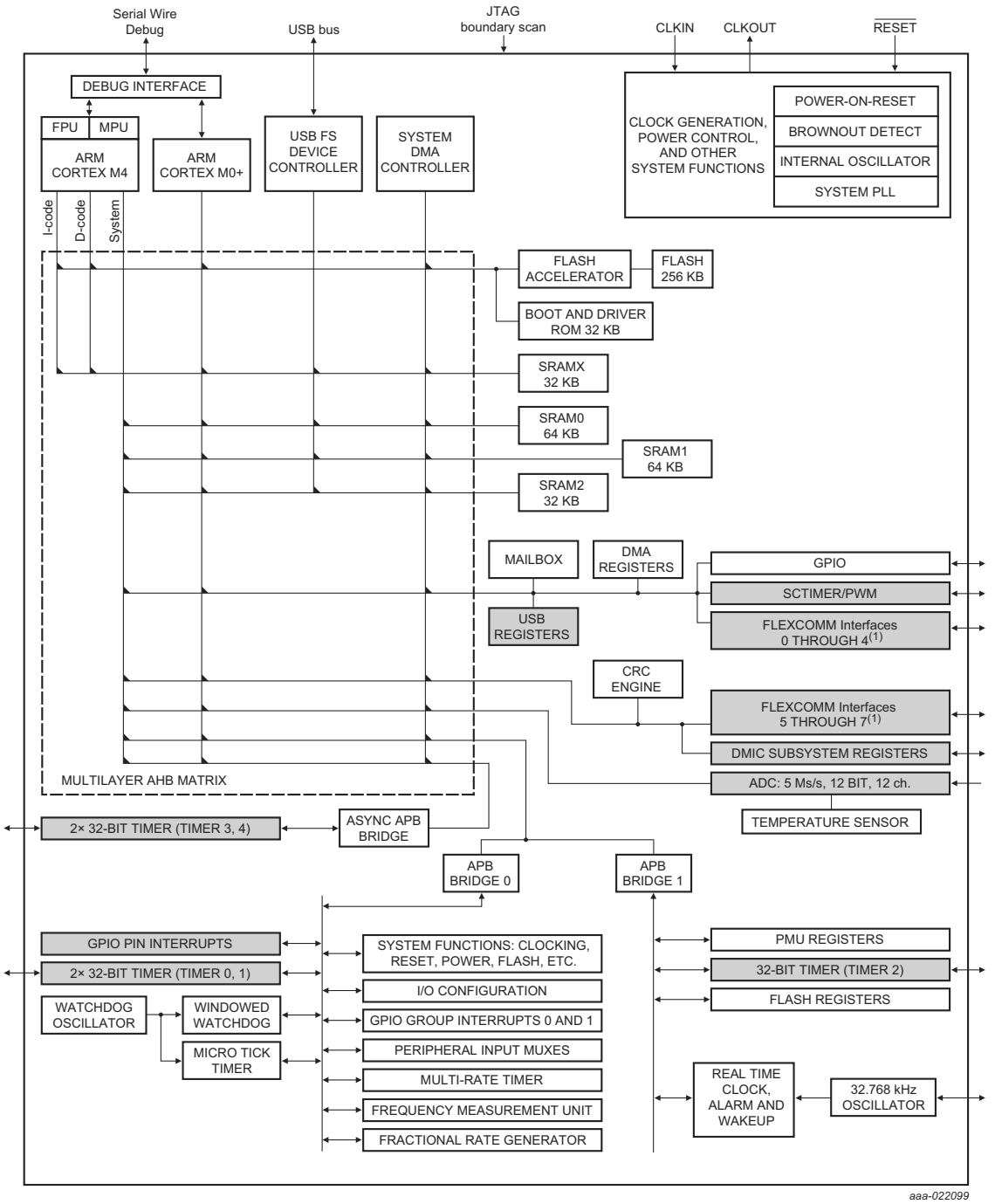
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4/M0+
Core Size	32-Bit Dual-Core
Speed	100MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	39
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	49-UFBGA, WLCSP
Supplier Device Package	49-WLCSP (3.44x3.44)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54114j256uk49z

5. Block diagram



Each Flexcomm Interface includes USART, SPI, and I^2C functions. Flexcomm Interfaces 6 and 7 each also provide an I2S function. Grey-shaded blocks indicate peripherals that provide DMA requests or are otherwise able to trigger DMA transfers

Fig 3. LPC5411x Block diagram

6. Pinning information

6.1 Pinning

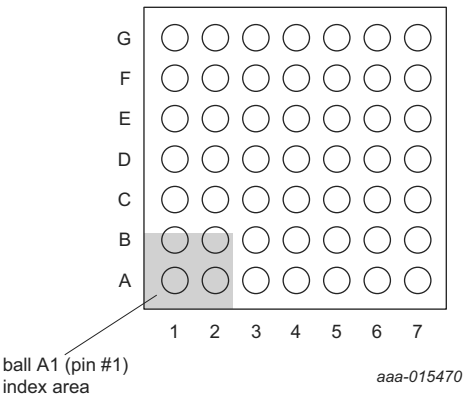


Fig 4. WLCSP49 Pin configuration

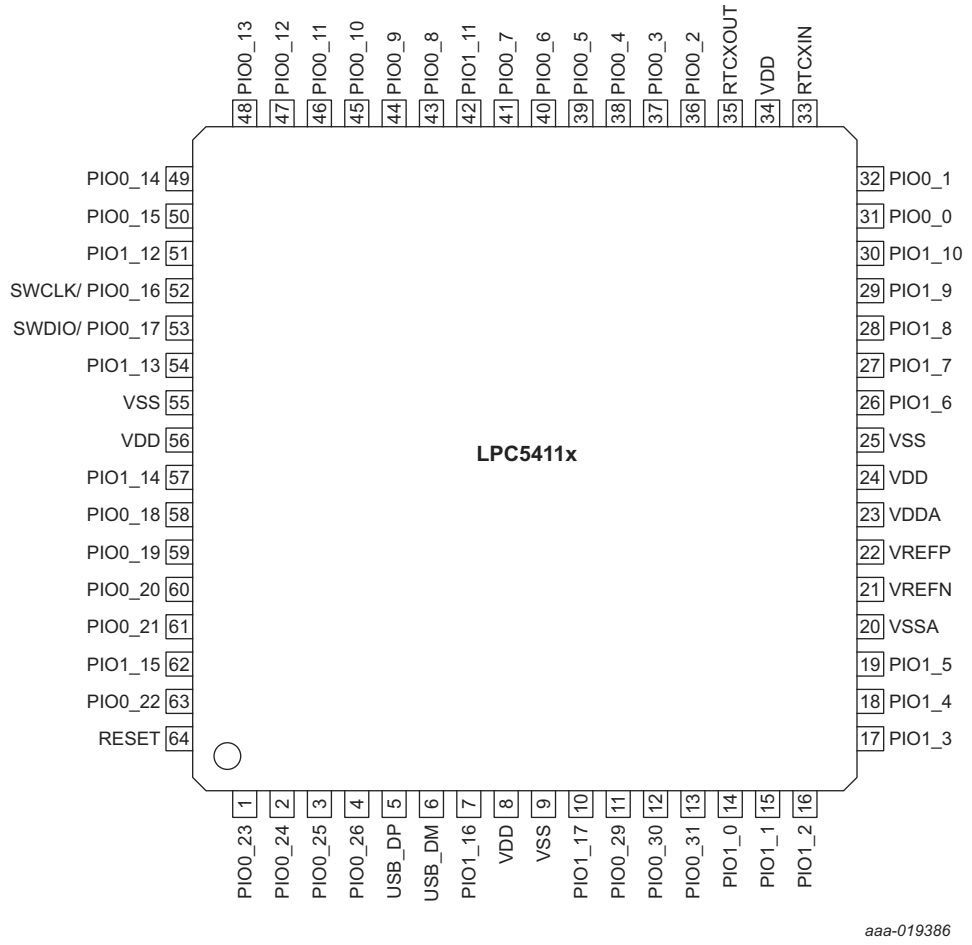


Fig 5. LQFP64 Pin configuration

6.2 Pin description

On the LPC5411x, digital pins are grouped into two ports. Each digital pin may support up to four different digital functions and one analog function, including General Purpose I/O (GPIO).

Table 4. Pin description

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_0	A6	31	[2]	PU	I/O	**PIO0_0 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm Interface 0 USART RXD function.
					I/O	**FC0_RXD_SDA_MOSI —** Flexcomm Interface 0: USART RXD, I2C SDA, SPI MOSI.
					I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm Interface 3: USART CTS, I2C SDA, SPI SSEL0.
					I	**CTimer0_CAP0 —** 32-bit CTimer0 capture input 0.
						R — Reserved.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
PIO0_1	B6	32	[2]	PU	I/O	**PIO0_1 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm Interface 0 USART TXD function.
					I/O	**FC0_TXD_SCL_MISO —** Flexcomm Interface 0: USART TXD, I2C SCL, SPI MISO.
					I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm Interface 3: USART RTS, I2C SCL, SPI SSEL1.
					I	**CTimer0_CAP1 —** 32-bit CTimer0 capture input 1.
						R — Reserved.
					O	**SCT0_OUT1 —** SCT0 output 1. PWM output 1.
PIO0_2	-	36	[2]	PU	I/O	**PIO0_2 —** General-purpose digital input/output pin.
					I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm Interface 0: USART CTS, I2C SDA, SPI SSEL0.
					I/O	**FC3_SSEL3 —** Flexcomm Interface 3: SPI SSEL3.
					I	**CTimer2_CAP1 —** 32-bit CTimer2 capture input 1.
PIO0_3	-	37	[2]	PU	I/O	**PIO0_3 —** General-purpose digital input/output pin.
					I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm Interface 0: USART RTS, I2C SCL, SPI SSEL1.
					I/O	**FC2_SSEL2 —** Flexcomm Interface 2: SPI SSEL2.
					O	**CTimer1_MAT3 —** 32-bit CTimer1 match output 3.
PIO0_4	C7	38	[2]	PU	I/O	**PIO0_4 —** General-purpose digital input/output pin. **Remark:** The state of this pin at Reset in conjunction with PIO0_31 and PIO1_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM10914 for more details.
					I/O	**FC0_SCK —** Flexcomm Interface 0: USART or SPI clock.
					I/O	**FC3_SSEL2 —** Flexcomm Interface 3: SPI SSEL2.
					I	**CTimer0_CAP2 —** 32-bit CTimer0 capture input 2.

Table 4. Pin description *…continued*

Symbol	49-pin	64-pin		Reset state [1]	Type	Description
PIO0_29/ ADC0_0	D3	11	[4]	PU	I/O; AI	**PIO0_29/ADC0_0 —** General-purpose digital input/output pin. ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I/O	**FC1_RXD_SDA_MOSI —** Flexcomm Interface 1: USART RXD, I2C SDA, SPI MOSI.
					O	**SCT0_OUT2 —** SCT0 output 2. PWM output 2.
					O	**CTimer0_MAT3 —** 32-bit CTimer0 match output 3.
						R — Reserved.
					I	**CTimer0_CAP1 —** 32-bit CTimer0 capture input 1.
						R — Reserved.
					O	**CTimer0_MAT1 —** 32-bit CTimer0 match output 1.
PIO0_30/ ADC0_1	C1	12	[4]	PU	I/O; AI	**PIO0_30/ADC0_1 —** General-purpose digital input/output pin. ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I/O	**FC1_TXD_SCL_MISO —** Flexcomm Interface 1: USART TXD, I2C SCL, SPI MISO.
					O	**SCT0_OUT3 —** SCT0 output 3. PWM output 3.
					O	**CTimer0_MAT2 —** 32-bit CTimer0 match output 2.
						R — Reserved.
					I	**CTimer0_CAP2 —** 32-bit CTimer0 capture input 2.
PIO0_31/ ADC0_2	C2	13	[4]	PU	I/O; AI	**PIO0_31/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin. **Remark:** This pin is also used to invoke ISP mode after device reset. Secondary selection of boot source for ISP mode also uses PIO0_4 and PIO1_6. See the Boot Process chapter in UM10914 for more details.
					O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
					I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm Interface 2: USART CTS, I2C SDA, SPI SSEL0.
					I	**CTimer2_CAP2 —** 32-bit CTimer2 capture input 2.
						R — Reserved.
					I	**CTimer0_CAP3 —** 32-bit CTimer0 capture input 3.
					O	**CTimer0_MAT3 —** 32-bit CTimer0 match output 3.
PIO1_0/ ADC0_3	C3	14	[4]	PU	I/O; AI	**PIO1_0/ADC0_3 —** General-purpose digital input/output pin. ADC input channel 3 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
					I	**PDM0_DATA —** Data for PDM interface 0, digital microphone input.
					I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm Interface 2: USART RTS, I2C SCL, SPI SSEL1.
					O	**CTimer3_MAT1 —** 32-bit CTimer3 match output 1.
						R — Reserved.
					I	**CTimer0_CAP0 —** 32-bit CTimer0 capture input 0.

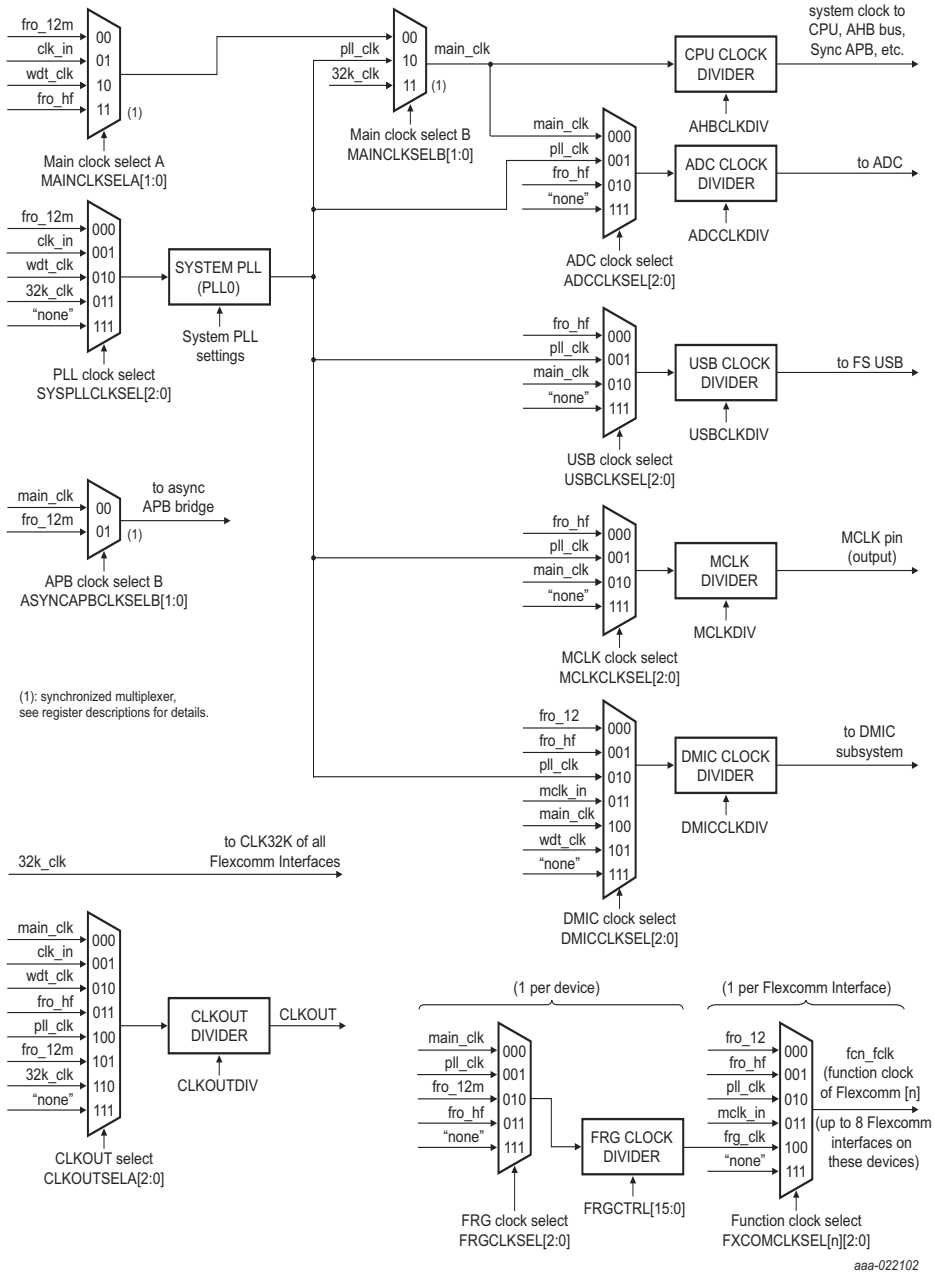


Fig 8. LPC5411x clock generation

Table 9 describes signals on the clocking diagram.

Table 7. Clocking diagram signal name descriptions

Name	Description
32k_clk	The 32 kHz output of the RTC oscillator. The 32 kHz clock must be enabled in the RTCOSCCTRL register.
clk_in	This is the internal clock that comes from the main CLK_IN pin function. That function must be connected to the pin by selecting it in the IOCON block.
frg_clk	The output of the Fractional Rate Generator.
fro_12m	The 12 MHz output of the currently selected on-chip FRO oscillator.
fro_hf	The currently selected FRO high speed output. This may be either 96 MHz or 48 MHz.
main_clk	The main clock used by the CPU and AHB bus, and potentially many others.
mclk_in	The MCLK input function, when it is connected to a pin by selecting it in the IOCON block.
pll_clk	The output of the PLL.
wdt_clk	The output of the watchdog oscillator, which has a selectable target frequency. It must also be enabled in the PDRINCFG0 register.
“none”	A tied-off source that should be selected to save power when the output of the related multiplexer is not used.

7.13.3 Brownout detection

The LPC5411x includes a monitor for the voltage level on the V_{DD} pin. If this voltage falls below a fixed level, the BOD sets a flag that can be polled or cause an interrupt. In addition, a separate threshold levels can be selected to cause chip reset and interrupt.

7.13.4 Safety

The LPC5411x includes a Windowed WatchDog Timer (WWDT), which can be enabled by software after reset. Once enabled, the WWDT remains locked and cannot be modified in any way until a reset occurs.

7.14 Code security (Code Read Protection - CRP)

This feature of the LPC5411x allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

In addition, ISP entry can be invoked by pulling a pin on the LPC5411x LOW on reset. This pin is called the ISP entry pin.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. CRP3 fully disables any access to the chip via SWD and ISP. It is up to the user’s application to provide (if needed) flash update mechanism using IAP calls or a call to reinvoke ISP command to enable a flash update via USART.

Table 9. Wake-up sources for reduced power modes

Power mode	Wake-up source	Conditions
Deep-sleep	Pin interrupts	Enable pin interrupts in NVIC and STARTER0 and/or STARTER1 registers.
	BOD interrupt	• Enable interrupt in NVIC and STARTER0 registers. • Enable interrupt in BODCTRL register. • Configure the BOD to keep running in this mode with the power API.
	BOD reset	Enable reset in BODCTRL register.
	Watchdog interrupt	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the watchdog interrupt in NVIC and STARTER0 registers. • Enable the watchdog in the WWDT MOD register and feed. • Enable interrupt in WWDT MOD register. • Configure the WDTOSC to keep running in this mode with the power API.
	Watchdog reset	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the watchdog and watchdog reset in the WWDT MOD register and feed.
	Reset pin	Always available.
	RTC 1 Hz alarm timer	• Enable the RTC 1 Hz oscillator in the RTCOSCCTRL register. • Enable the RTC bus clock in the AHBCLKCTRL0 register. • Start RTC alarm timer by writing a time-out value to the RTC COUNT register. • Enable the RTCALARM interrupt in the STARTER0 register.
	RTC 1 kHz timer time-out and alarm	• Enable the RTC 1 Hz oscillator and the RTC 1 kHz oscillator in the RTC CTRL register. • Start RTC 1 kHz timer by writing a value to the WAKE register of the RTC. • Enable the RTC wake-up interrupt in the STARTER0 register.
	Micro-tick timer (intended for ultra-low power wake-up from deep-sleep mode	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the Micro-tick timer clock by writing to the AHBCLKCTRL1 register. • Start the Micro-tick timer by writing UTICK CTRL register. • Enable the Micro-tick timer interrupt in the STARTER0 register.
	I^2C interrupt	Interrupt from I^2C in slave mode.
	SPI interrupt	Interrupt from SPI in slave mode.
	USART interrupt	Interrupt from USART in slave or 32 kHz mode.
	USB need clock interrupt	Interrupt from USB when activity is detected that requires a clock.
	DMA interrupt	See the LPC5411x User Manual for details of DMA-related interrupts.
	HWWAKE	Certain Flexcomm Interface and DMIC subsystem activity.
Deep power-down	RTC 1 Hz alarm timer	• Enable the RTC 1 Hz oscillator in the RTC CTRL register. • Start RTC alarm timer by writing a time-out value to the RTC COUNT register.
	RTC 1 kHz timer time-out and alarm	• Enable the RTC 1 Hz oscillator and the RTC 1 kHz oscillator in the RTCOSCCTRL register. • Enable the RTC bus clock in the AHBCLKCTRL0 register. • Start RTC 1 kHz timer by writing a value to the WAKE register of the RTC.
	Reset pin	Always available.

7.17.1 Features

- Pin interrupts:
  - Up to eight pins can be selected from all GPIO pins on ports 0 and 1 as edge-sensitive or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Pin interrupts can wake up the device from sleep mode and deep-sleep mode.
- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

7.18 AHB peripherals

7.18.1 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.18.1.1 Features

- 20 channels, 19 of which are connected to peripheral DMA requests. These come from the Flexcomm Interfaces (USART, SPI, I^2C, and I2S) and digital microphone interfaces.
- DMA operations can be triggered by on-chip or off-chip events.
- Priority is user selectable for each channel (up to eight priority levels).
- Continuous priority arbitration.
- Address cache with four entries.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

Every action that the SCTimer/PWM block can perform occurs in direct response to one of these user-defined events without any software overhead. Any event can be enabled to:

- Start, stop, or halt the counter.
- Limit the counter which means to clear the counter in unidirectional mode or change its direction in bi-directional mode.
- Set, clear, or toggle any SCTimer/PWM output.
- Force a capture of the count value into any capture registers.
- Generate an interrupt of DMA request.

7.20.2.1 Features

- The SCTimer/PWM Supports:
  - Eight inputs.
  - Eight outputs.
  - Ten match/capture registers.
  - Ten events.
  - Ten states.
- Counter/timer features:
  - Each SCTimer/PWM is configurable as two 16-bit counters or one 32-bit counter.
  - Counters clocked by system clock or selected input.
  - Configurable number of match and capture registers. Up to five match and capture registers total.
  - Ten events.
  - Ten states.
  - Upon match and/or an input or output transition create the following events: interrupt; stop, limit, halt the timer or change counting direction; toggle outputs; change the state.
  - Counter value can be loaded into capture register triggered by a match or input/output toggle.

10.3 Power consumption

Power measurements in active, sleep, and deep-sleep modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.
- All peripherals disabled.

Table 14. Static characteristics: Power consumption in active mode

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
ARM Cortex-M0+ in active mode; ARM Cortex-M4 in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAMX; flash powered down: CCLK = 12 MHz	[2][3][4][6][7]	-	1.1	-	mA
		CCLK = 48 MHz	[2][3][4][6][7]	-	3.0	-	mA
		CCLK = 96 MHz	[2][3][4][6]	-	7.1	-	mA
I_{DD}	supply current	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[2][3][4][5][7]	-	1.3	-	mA
		CCLK = 48 MHz; 3 system clock flash access time.	[2][3][4][5][7]	-	3.6	-	mA
		CCLK = 96 MHz; 7 system clock flash access time.	[2][3][4][5]	-	8.0	-	mA
ARM Cortex-M4 in active mode; ARM Cortex-M0+ in sleep mode							
I_{DD}	supply current	CoreMark code executed from SRAMX; flash powered down: CCLK = 12 MHz	[2][3][4][6][7]	-	1.3	-	mA
		CCLK = 48 MHz	[2][3][4][6][7]	-	3.9	-	mA
		CCLK = 96 MHz	[2][3][4][6]	-	9.3	-	mA
I_{DD}	supply current	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[2][3][4][5][7]	-	1.5	-	mA
		CCLK = 48 MHz; 3 system clock flash access time.	[2][3][4][5][7]	-	4.6	-	mA
		CCLK = 96 MHz; 7 system clock flash access time.	[2][3][4][5]	-	9.9	-	mA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), 3.3V.

[2] Clock source FRO. PLL disabled.

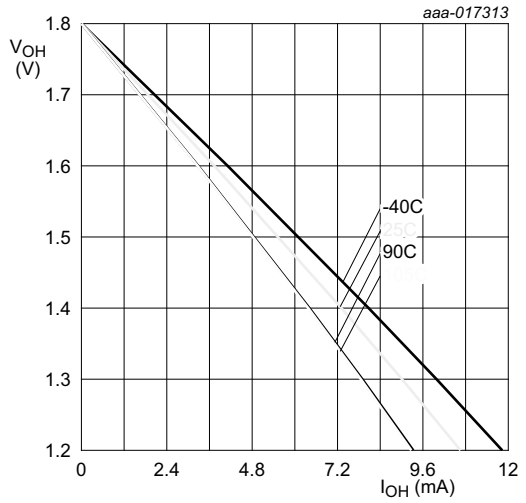
[3] Characterized through bench measurements using typical samples.

[4] Compiler settings: Keil µVision 5.17., optimization level 0, optimized for time off.

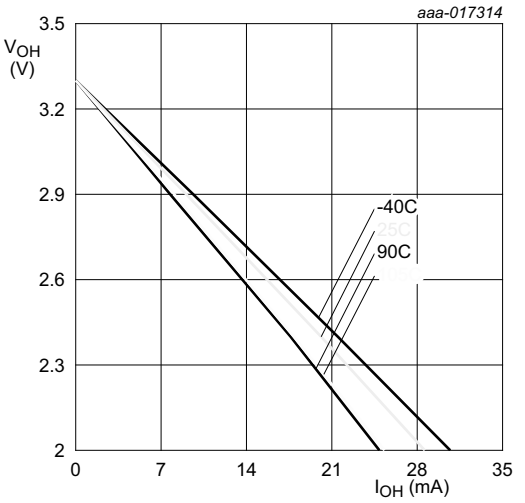
[5] Prefetch disabled in FLASHCFG register. SRAM0 powered. SRAM1, SRAM2, and SRAMX powered down. All peripheral clocks disabled.

[6] Flash is powered down; SRAM0 and SRAMX are powered; SRAM1 and SRAM2 are powered down. All peripheral clocks disabled.

[7] Characterized using low power regulation mode.

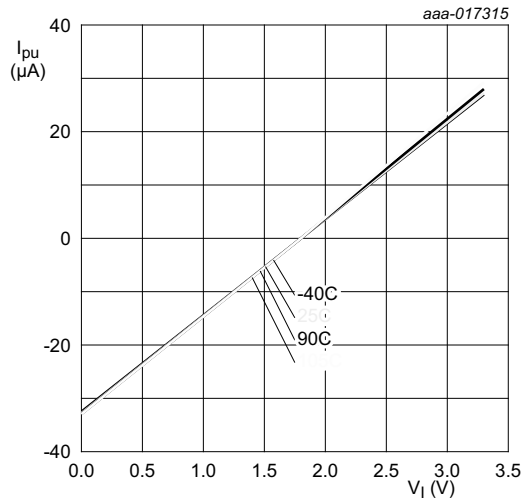


Conditions: V_{DD} = 1.8 V; on standard port pins.

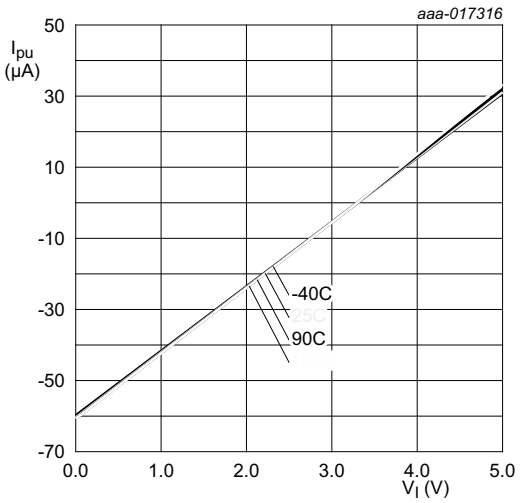


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 16. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 1.8 V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 17. Typical pull-up current I_{PU} versus input voltage V_I

11. Dynamic characteristics

11.1 Flash memory

Table 21. Flash characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
N_{endu}	endurance	sector erase/program	[2]	10000	-	-	cycles
		page erase/program; page in a sector		1000	-	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	page, sector, or multiple consecutive sectors		-	100	-	ms
t_{prog}	programming time		[3]	-	1	-	ms

[1] Typical ratings are not guaranteed.

[2] Number of erase/program cycles.

[3] Programming times are given for writing 256 bytes from RAM to the flash.

11.2 I/O pins

Table 22. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +85 °C unless otherwise specified; 1.62 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1 (fast mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.0	-	2.5	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		1.6	-	3.8	ns
t_f	fall time	pin configured as output; SLEW = 1 (fast mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		0.9	-	2.5	ns
		1.62 V ≤V_{DD} ≤ 1.98 V		1.7	-	4.1	ns
t_r	rise time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.3	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		2.9	-	7.8	ns
t_f	fall time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.0	ns
		1.62 V ≤ V_{DD} ≤ 1.98 V		2.7	-	6.7	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data.

[2] Clock Divider register (DIV) = 0x0.

[3] Typical ratings are not guaranteed.

[4] The Flexcomm Interface function clock frequency should not be above 48 MHz. See the data rates section in the I²S chapter (UM10912) to calculate clock and sample rates.

[5] Based on simulation. Not tested in production.

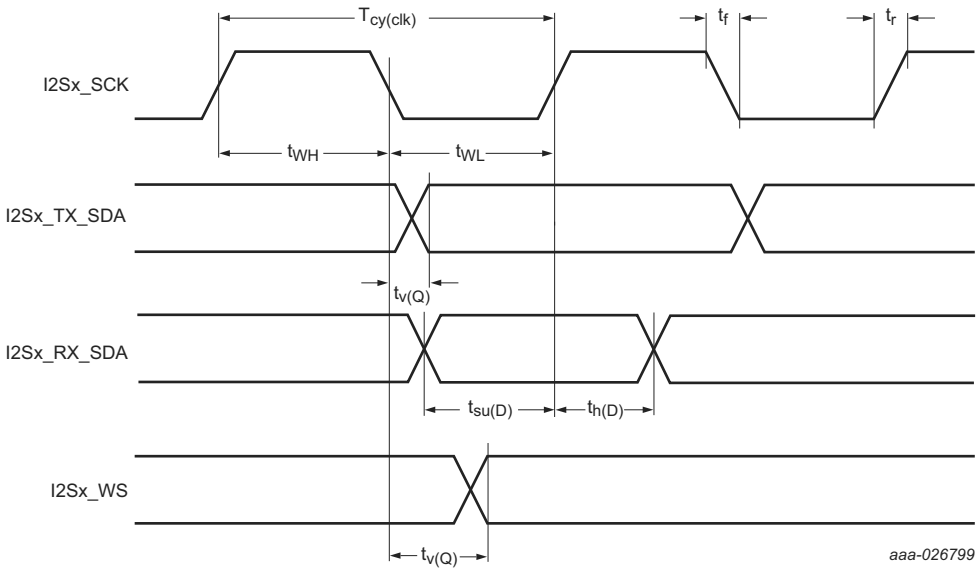


Fig 20. I²S-bus timing (master)

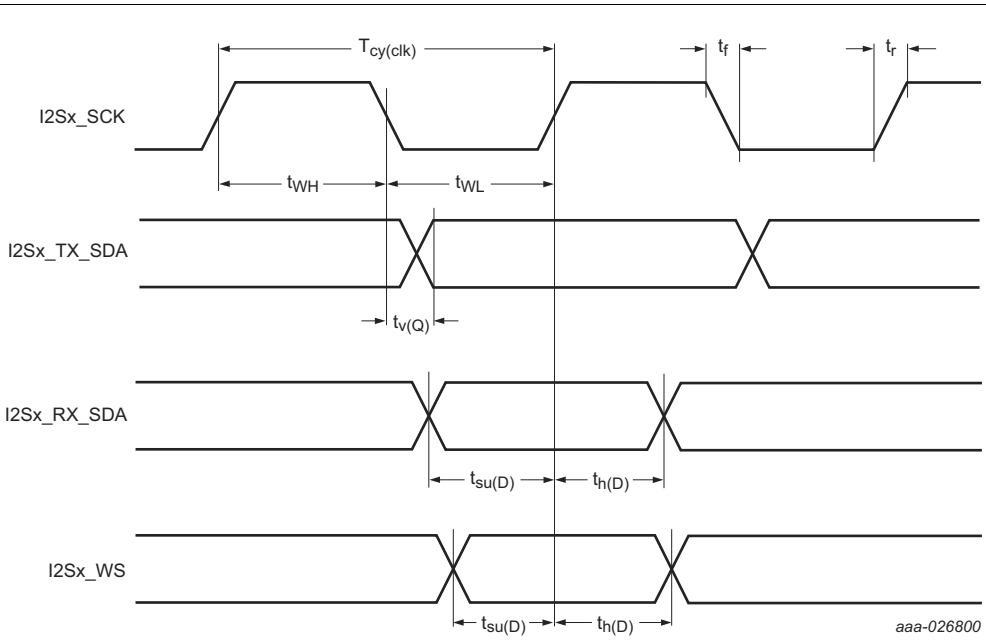
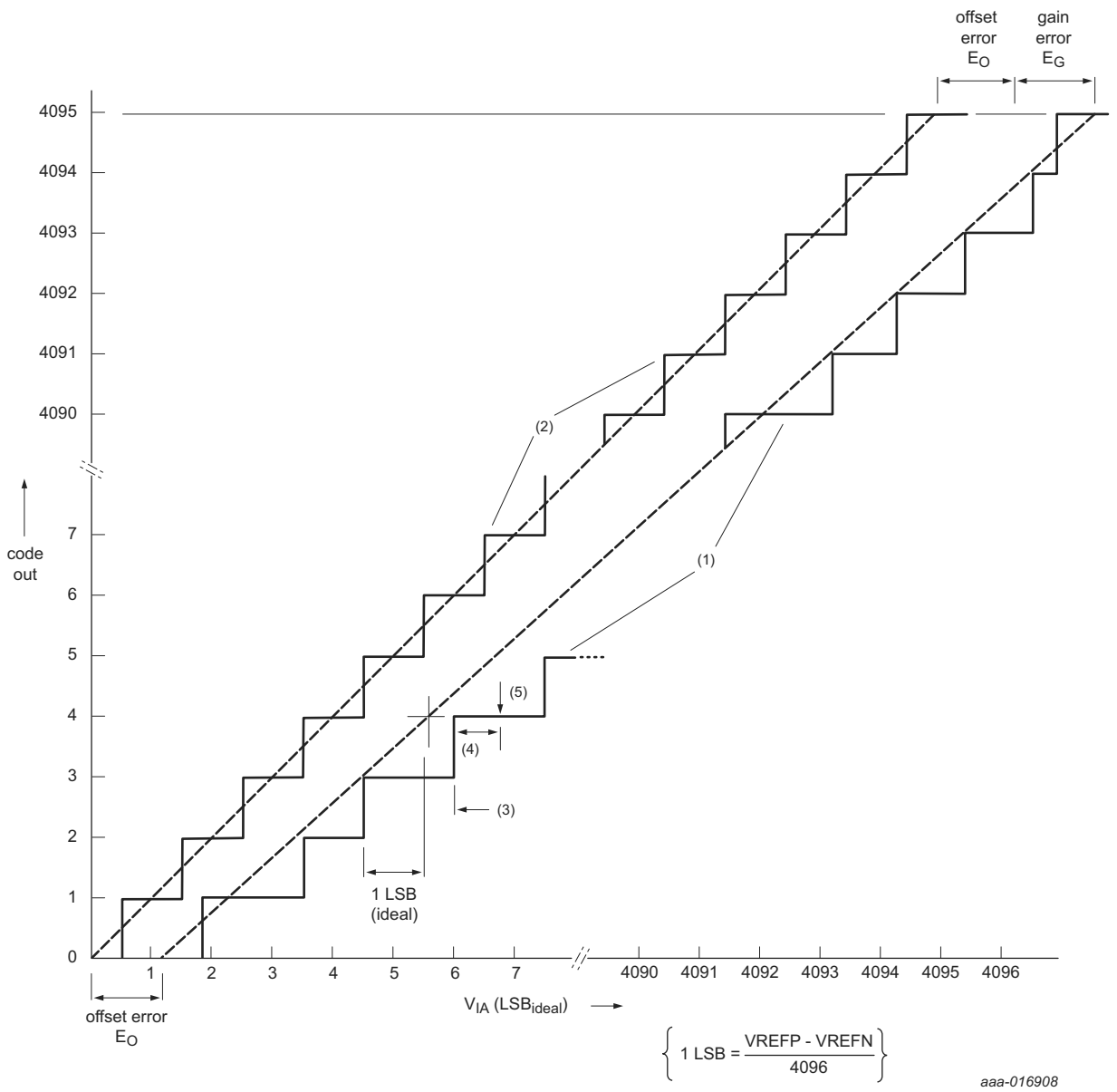


Fig 21. I²S-bus timing (slave)

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 27.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 5.0 Msamples/s and analog input capacitance C_{ia} = 5 pF.

[10] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 20 for C_{io}. See Figure 28.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 27. 12-bit ADC characteristics

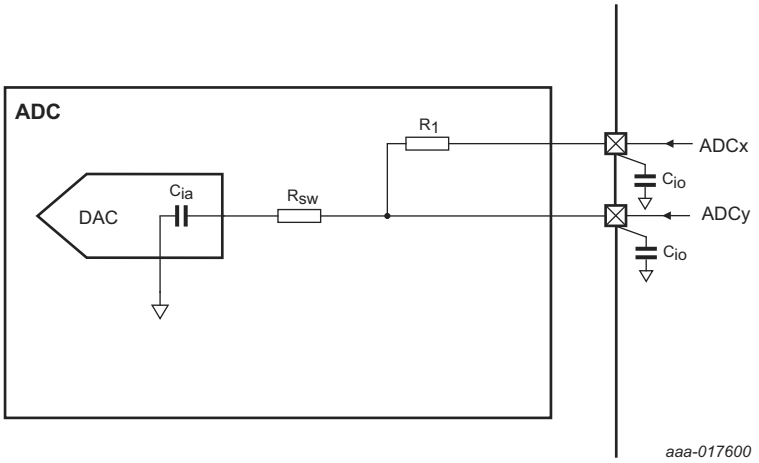


Fig 28. ADC input impedance

12.3 Temperature sensor

Table 39. Temperature sensor static and dynamic characteristics
$V_{DD} = V_{DDA} = 1.62$ V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C	[1]	-	-	3	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C		-	-	3	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	10	15	µs

[1] Absolute temperature accuracy.

[2] Based on simulation.

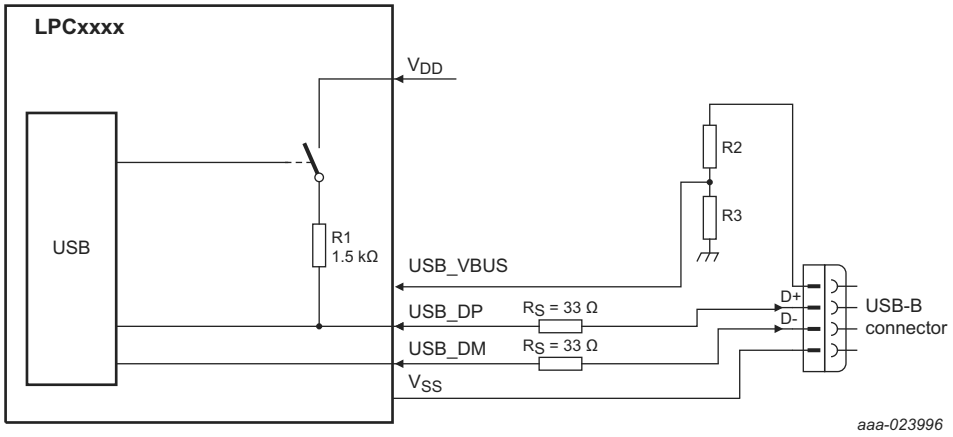
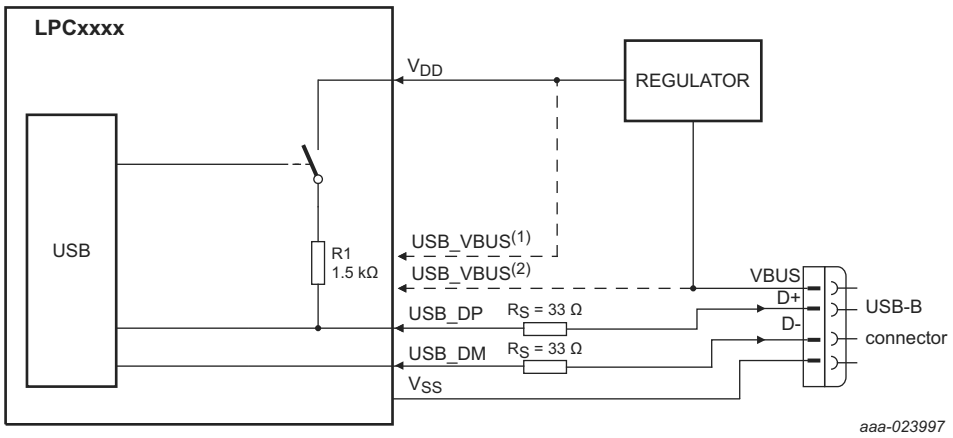


Fig 34. USB interface on a self-powered device where USB_VBUS = 5 V

The internal pull-up (1.5 kΩ) can be enabled by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required.



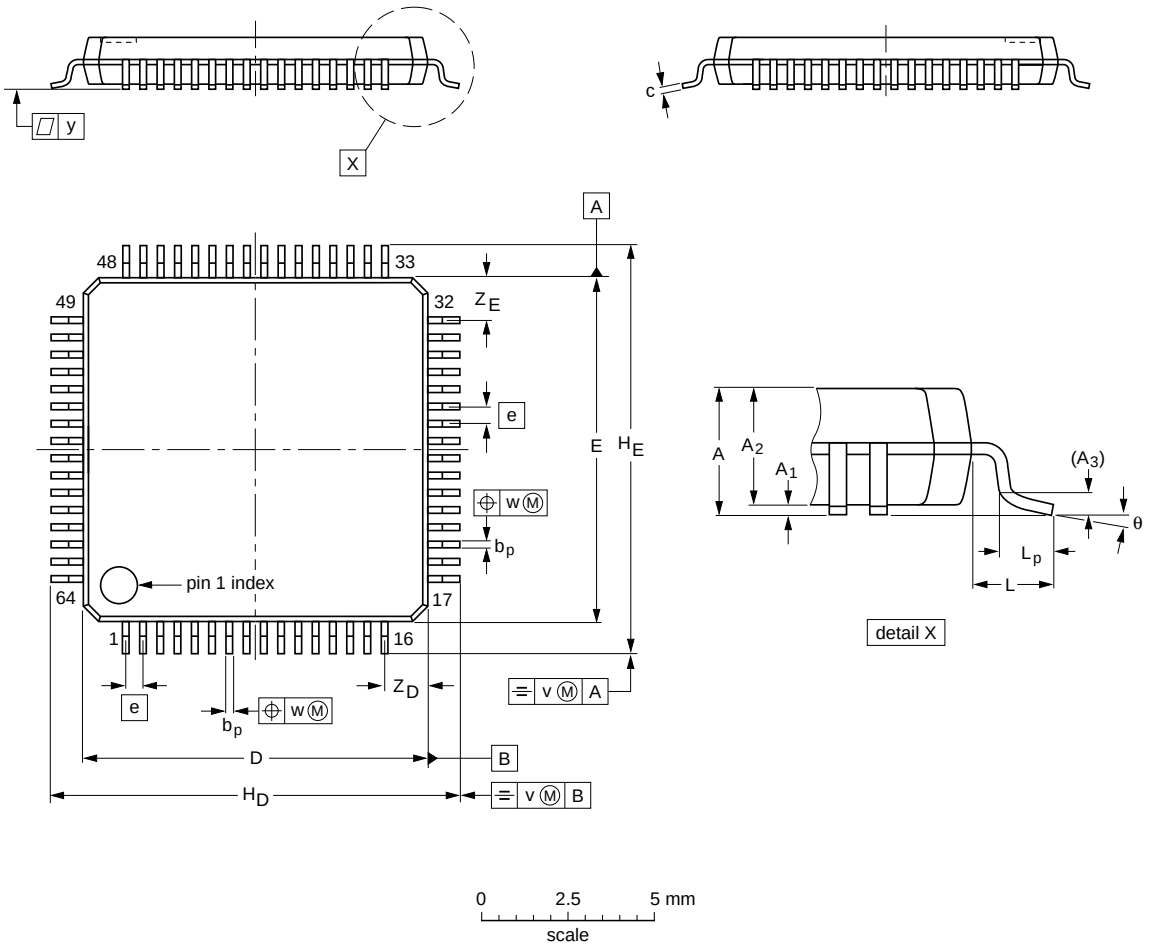
Two options exist for connecting VBUS to the USB_VBUS pin:

(1) Connect the regulator output to USB_VBUS. In this case, the USB_VBUS signal is HIGH whenever the part is powered.

(2) Connect the VBUS signal directly from the connector to the USB_VBUS pin. In this case, 5 V are applied to the USB_VBUS pin while the regulator is ramping up to supply V_{DD}. Since the USB_VBUS pin is only 5 V tolerant when V_{DD} is at operating level, this connection can degrade the performance of the part over its lifetime. Simulation shows that lifetime is reduced to 15 years at T_{amb} = 45 °C and 8 years at T_{amb} = 55 °C assuming that USB_VBUS = 5 V is applied continuously while V_{DD} = 0 V.

Fig 35. USB interface on a bus-powered device

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 37. LQFP64 Package outline

18. Revision history

Table 43. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC5411x v.2.1	20180509	Product data sheet	-	LPC5411x v.2.0
Modifications:	• Updated Section 2 “Features and benefits”: text for serial interfaces: USB 2.0 full-speed device controller with on-chip PHY and dedicated DMA controller supporting crystal-less operation in device mode using software library. See Technical note TN00031 for more details.			
LPC5411x v.2.0	20180420	Product data sheet	-	LPC5411x v.1.9
Modifications:	• Fixed Figure 38 “WLCSP49 Soldering footprint”. • Added Figure 39 “LQFP64 Soldering footprint”.			
LPC5411x v.1.9	20180126	Product data sheet	-	LPC5411x v.1.8
Modifications:	• Updated a feature in Section 7.19.5 “SPI serial I/O controller”: Maximum data rate of 48 Mbit/s in master mode and 15 Mbit/s in slave mode for SPI functions. Was 71 Mbit/s in master mode. • Updated Section 11.10 “SPI interfaces”: the maximum supported bit rate for SPI master mode is 48 Mbit/s. Was 71 Mbit/s in master mode.			
LPC5411x v.1.8	20171102	Product data sheet	-	LPC5411x v.1.7
Modifications:	• Updated broken cross references throughout the document.			
LPC5411x v.1.7	20170417	Product data sheet	-	LPC5411x v.1.6
Modifications:	• Updated Table 30 “Dynamic characteristics: I2S-bus interface pins [1][4]” • Updated Table 16 “Static characteristics: Power consumption in deep-sleep and deep power-down modes” and Table 17 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”: Conditions for I_{DD} supply current.			
LPC5411x v.1.6	20161222	Product data sheet	-	LPC5411x v.1.5

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For sales office addresses, please send an email to: salesaddresses@nxp.com

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