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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UFQFN Exposed Pad
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl03z16vfg4r

Ordering Information[1]

Part Number	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MKL03Z8VFG4(R)	8	2	14
MKL03Z16VFG4(R)	16	2	14
MKL03Z32VFG4(R)	32	2	14
MKL03Z32CAF4R	32	2	18
MKL03Z32CBF4R	32	2	18
MKL03Z8VFK4(R)	8	2	22
MKL03Z16VFK4(R)	16	2	22
MKL03Z32VFK4(R)	32	2	22

1. To confirm current availability of ordererable part numbers, go to http://www.nxp.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL03PB[1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL03P24M48SF0RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KL03P24M48SF0[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KL03Z_*x*N86K[2]
Package drawing	Package dimensions are provided in package drawings.	QFN 16-pin: 98ASA00525D[1] QFN 24-pin: 98ASA00602D[1] WLCSP 20-pin: 98ASA00676D[1] WLCSP 20-pin (ultra thin): 98ASA00964D[1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.
2. To find the associated resource, go to http://www.nxp.com and perform a search using this term with the “x” replaced by the revision of the device you are using.

Figure 1 shows the functional modules in the chip.

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1.4 Voltage and current operating ratings

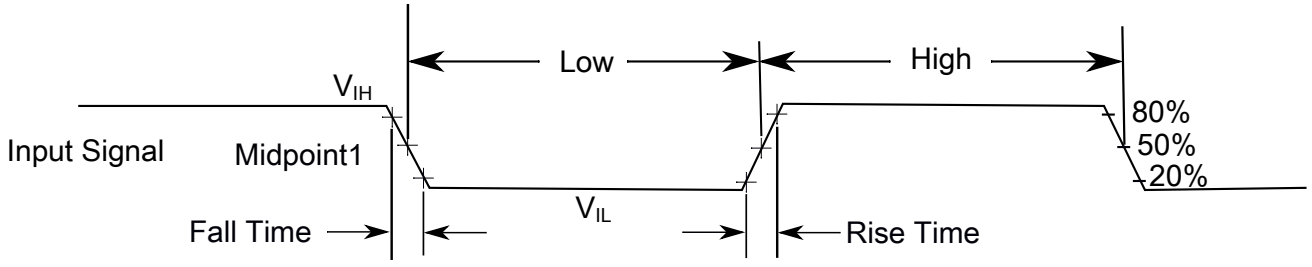
Table 5. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	IO pin input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- C_L=30 pF loads

2.2.2 LVD and POR operating requirements

Table 7. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	—
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	—

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 8. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad (except $\overline{\text{RESET}}$)				1, 2
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –2.5 mA	V_{DD} – 0.5	—	V	
V_{OH}	Output high voltage — High drive pad (except $\overline{\text{RESET}}$)				1, 2
		V_{DD} – 0.5	—	V	
		V_{DD} – 0.5	—	V	

Table continues on the next page...

Table 8. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = –20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = –10 mA				
I_{OHT}	Output high current total for all ports	—	100	mA	—
V_{OL}	Output low voltage — Normal drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	 — —	 0.5 0.5	 V V	1
V_{OL}	Output low voltage — High drive pad • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	 — —	 0.5 0.5	 V V	1
I_{OLT}	Output low current total for all ports	—	100	mA	—
I_{IN}	Input leakage current (per pin) for full temperature range	—	1	µA	3
I_{IN}	Input leakage current (per pin) at 25 °C	—	0.025	µA	3
I_{IN}	Input leakage current (total all pins) for full temperature range	—	41	µA	3
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	—
R_{PU}	Internal pullup resistors	20	50	kΩ	4

1. I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
3. Measured at V_{DD} = 3.6 V
4. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

VLLSx→RUN recovery uses LIRC clock mode at the default CPU and system frequency of 8 MHz, and a bus and flash clock frequency of 4 MHz.

Table 9. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Note
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	1
	• VLLS0 → RUN	—	152	166	µs	—
	• VLLS1 → RUN	—	152	166	µs	—
	• VLLS3 → RUN	—	93	104	µs	—
	• VLPS → RUN	—	7.5	8	µs	—
	• STOP → RUN	—	7.5	8	µs	—

1. Normal boot (FTFA_FOPT[LPBOOT]=11).

2.2.5 Power consumption operating behaviors

Table 10. KL03 QFN packages power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	2
I_{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.49	5.71	mA	
	• at 105 °C	—	5.62	5.84		
I_{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.16	5.37	mA	
	• at 105 °C	—	5.27	5.48		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	6.03	6.27	mA	
	• at 105 °C	—	6.16	6.41		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V					3

Table continues on the next page...

Table 10. KL03 QFN packages power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V					—
	• at 25 °C and below	—	265	373	nA	
	• at 50 °C	—	467	512.9		
	• at 85 °C	—	1920	2256		
	• at 105 °C	—	4540	5395		
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V					4
	• at 25 °C and below	—	77	350	nA	
	• at 50 °C	—	255	465.70		
	• at 85 °C	—	1640	1994		
	• at 105 °C	—	4080	4956		

1. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).
2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
4. No brownout

Table 11. KL03 WLCSP package power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	2
I_{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.49	5.71	mA	
	• at 85 °C	—	5.59	5.81		
I_{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	5.16	5.37	mA	
	• at 85 °C	—	5.24	5.45		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					3
	• at 25 °C	—	6.03	6.27	mA	
	• at 85 °C	—	6.13	6.38		

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 3.71 3.78	 3.86 3.93	 mA	3
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 2.47 2.55	 2.57 2.65	 mA	3
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 6.43 6.53	 6.69 6.79	 mA	3
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 5.71 5.79	 5.94 6.02	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 3.3 3.37	 3.43 3.50	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 2.28 2.35	 2.37 2.44	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	 — —	 6.1 6.19	 6.34 6.44	 mA	—
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V	 — —	 3.14 3.24	 3.23 3.33	 mA	—

Table continues on the next page...

Table 11. KL03 WLCSP package power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 25 °C • at 85 °C					
I_{DD_RUN}	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V_{DD} = 3.0 V • at 25 °C • at 85 °C	— —	3.54 3.64	3.63 3.73	mA	—
I_{DD_VLPRCO}	Very-low-power run While(1) loop in flash in compute operation mode— 2 MHz LIRC mode, 2 MHz core/0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	500	750	µA	—
I_{DD_VLPRCO}	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	188	217	µA	—
I_{DD_VLPRCO}	Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	82	123	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	503	754	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V_{DD} = 3.0 V • at 25 °C	—	60	90	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	516	774	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	209	350	µA	—
I_{DD_VLPR}	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	229	370	µA	—
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all					—

Table continues on the next page...

2.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for "EMC design"

2.2.8 Capacitance attributes

Table 14. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 15. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
f_{SYS}	System and core clock	—	48	MHz
f_{BUS}	Bus clock	—	24	MHz
f_{FLASH}	Flash clock	—	24	MHz
f_{LPTMR}	LPTMR clock	—	24	MHz
VLPR and VLPS modes[1]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	1	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{LPTMR}	LPTMR clock[2]	—	24	MHz
f_{ERCLK}	External reference clock	—	16	MHz
f_{ERCLK}	External reference clock	—	32.768	kHz
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
f_{TPM}	TPM asynchronous clock	—	8	MHz
f_{UART0}	UART0 asynchronous clock	—	8	MHz

3.1.1 SWD electricals

Table 20. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	 0	 25	 MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	 20	 —	 ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

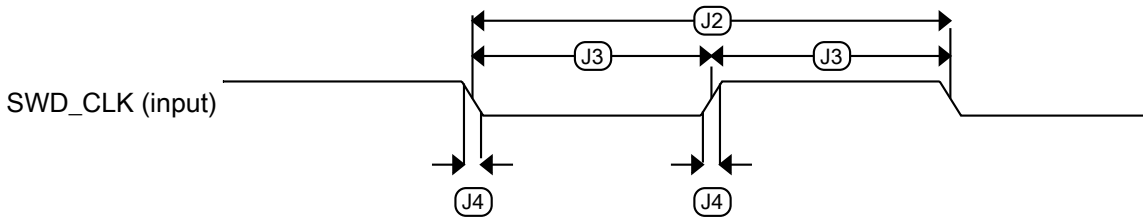


Figure 6. Serial wire clock input timing

Table 21. HIRC48M specification (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$\Delta f_{irc48m\_ol\_hv}$	total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over temperature	—	± 0.5	±1.0	$\%f_{irc48m}$	—
J_{cyc_irc48m}	Period Jitter (RMS)	—	35	150	ps	—
$t_{irc48mst}$	Startup time	—	2	3	µs	1

1. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by setting MCG_MC[HIRCEN] = 1. See reference manual for details.

Table 22. LIRC8M/2M specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.08	—	1.47	V	—
T	Temperature range	-40	—	125	°C	—
I_{DD_2M}	Supply current in 2 MHz mode	—	14	17	µA	—
I_{DD_8M}	Supply current in 8 MHz mode	—	30	35	µA	—
f_{IRC_2M}	Output frequency	—	2	—	MHz	—
f_{IRC_8M}	Output frequency	—	8	—	MHz	—
$f_{IRC\_T\_2M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	V_{DD}≥1.89 V
$f_{IRC\_T\_8M}$	Output frequency range (trimmed)	—	—	±3	$\%f_{IRC}$	V_{DD}≥1.89 V
T_{su_2M}	Startup time	—	—	12.5	µs	—
T_{su_8M}	Startup time	—	—	12.5	µs	—

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 23. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	—
I_{DDOSC}	Supply current — low-power mode • 32 kHz	—	500	—	nA	1
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode	—	—	—	MΩ	2, 4
R_S	Series resistor — low-frequency, low-power mode	—	—	—	kΩ	—

Table continues on the next page...

Table 30. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
DNL	Differential non-linearity	• 12-bit modes	—	±0.9	–1.1 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.4	–0.3 to 0.5		
INL	Integral non-linearity	• 12-bit modes	—	±1.5	–2.7 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.5	–0.7 to +0.5		
E_{FS}	Full-scale error	• 12-bit modes	—	5	—	LSB[4]	V_{ADIN} = V_{DDA}[5]
		• <12-bit modes	—	2	3		
E_Q	Quantization error	• 12-bit modes	—	—	±0.5	LSB[4]	
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	6
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	6

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = (V_{REFH} - V_{REFL})/2^N
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. ADC conversion clock < 3 MHz

Table 31. 12-bit ADC characteristics (V_{REFH} = V_{REFO}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = $1/f_{ADACK}$
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	

Table continues on the next page...

Table 34. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	1
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	1
V_{step}	Voltage reference trim step	—	0.5	—	mV	1
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range: 0 to 70°C)	—	—	50	mV	1
Ac	Aging coefficient	—	—	400	uV/yr	—
I_{bg}	Bandgap only current	—	—	80	µA	1
I_{lp}	Low-power buffer current	—	—	360	uA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	µV	1, 2
T_{stup}	Buffer startup time	—	—	100	µs	—
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 35. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	—

Table 36. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	—

3.7 Timers

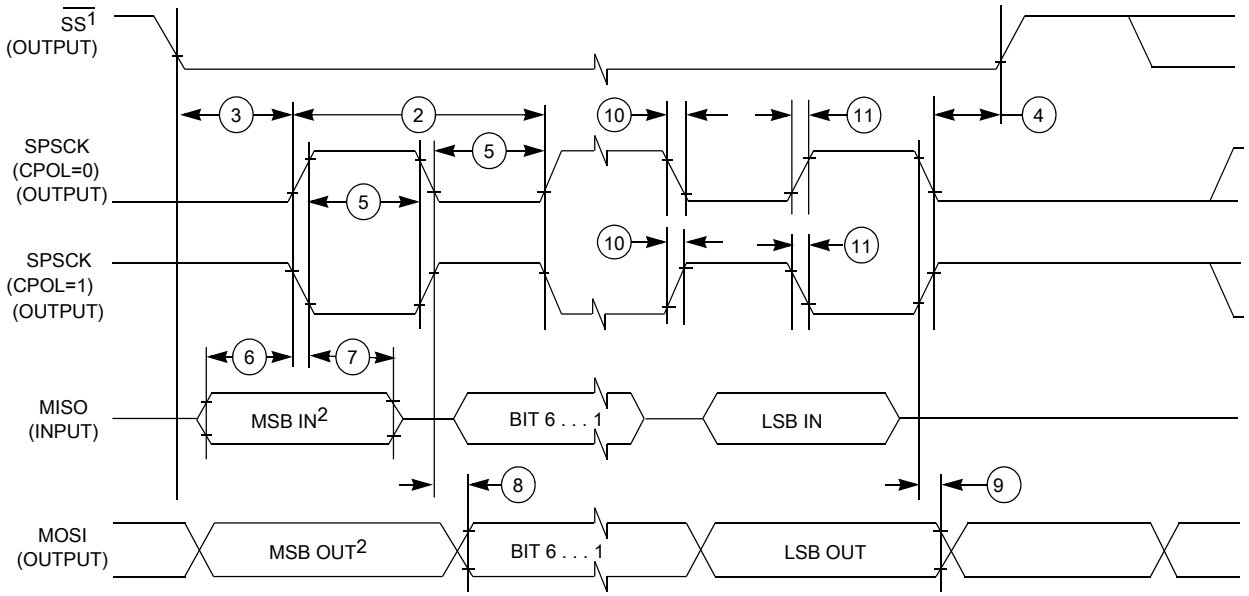
See General switching specifications.

3.8 Communication interfaces

Table 38. SPI master mode timing on slew rate enabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI master mode timing (CPHA = 0)

Table 40. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} – 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} – 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

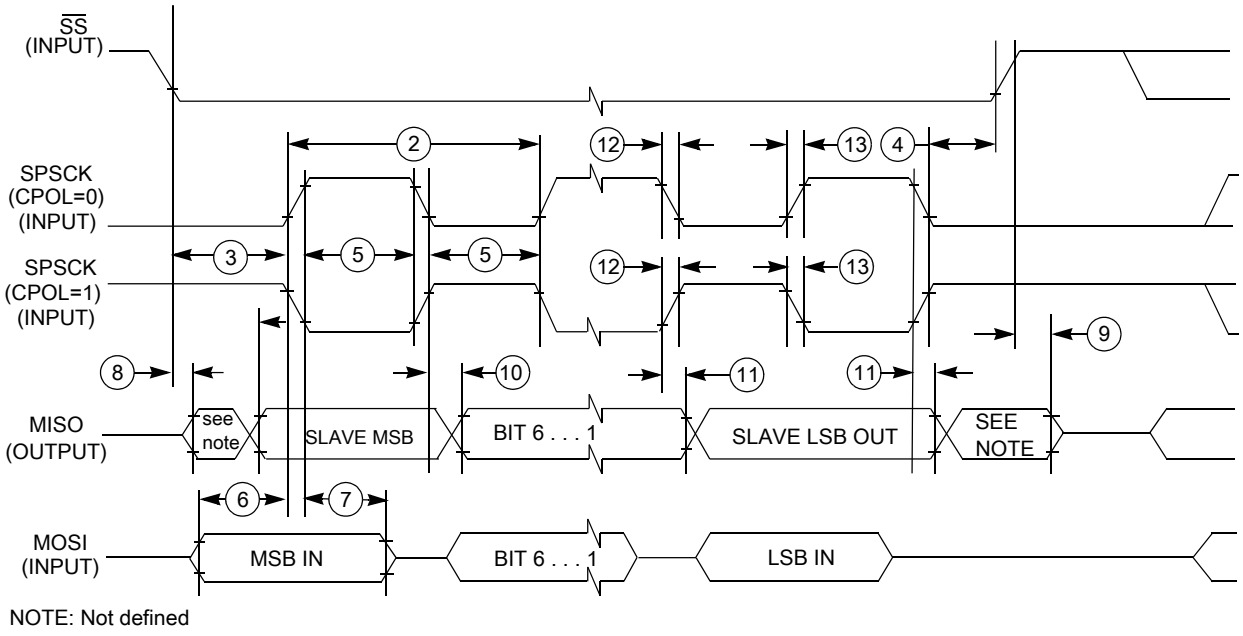


Figure 14. SPI slave mode timing (CPHA = 0)

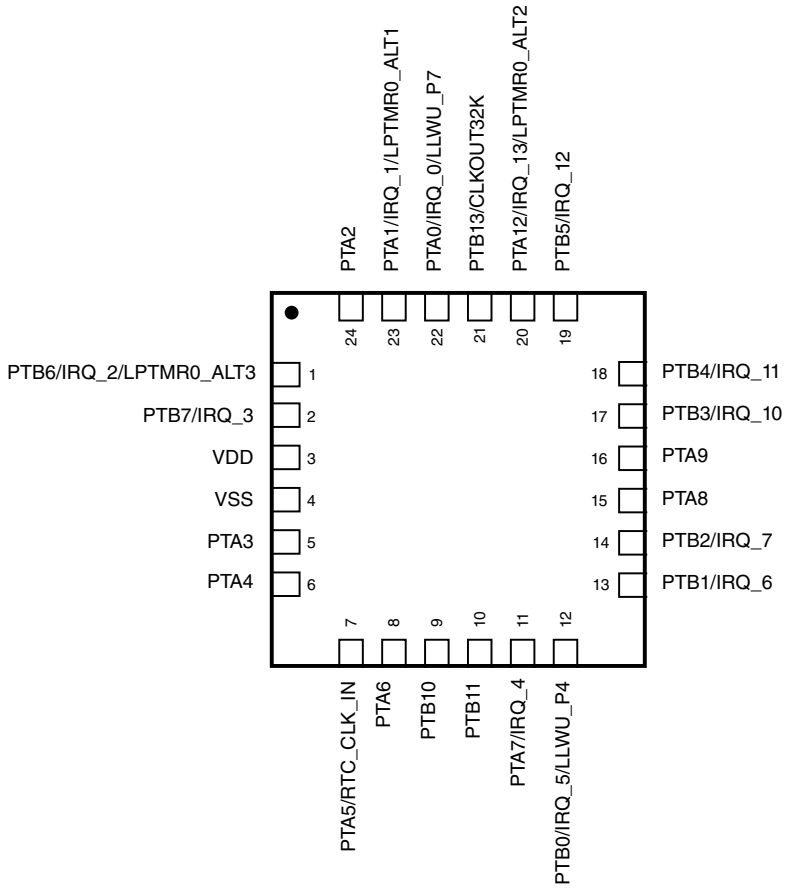


Figure 17. KL03 24-pin QFN pinout diagram

	1	2	3	4	5
A	PTB3	PTB5	PTB13	PTA0	PTA2
B	PTB2	PTB4	PTA12	PTA1	VDD
C	PTB0	PTA9	PTA4	PTA3	VSS
D	PTB1	PTA8	PTA5	PTA7	PTA6

Figure 18. KL03 20-pin WLCSP pinout diagram

7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 43. Part number fields description

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow(full reels for WLCSP) • P = Prequalification • K = Fully qualified, general market flow, 100 pieces reels (WLCSP only)
KL##	Kinetis family	• KL03
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	• 8 = 8 KB • 16 = 16 KB • 32 = 32 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• FG = 16 QFN (3 mm x 3 mm) • AF = 20 WLCSP (2 mm x 1.61 mm x 0.56 mm) • BF = 20 WLCSP (2 mm x 1.61 mm x 0.32 mm) • FK = 24 QFN (4 mm x 4 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKL03Z32VFK4

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions: