Renesas Electronics America Inc - UPD70F3826GB(R)-GAH-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, CSI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3826gb-r-gah-ax

APPLICATIONS

○ Applications that require Ethernet controller

Home audio, printers, and scanners.

ORDERING INFORMATION

- V850ES/JE3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3826GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	64 KB
μPD70F3827GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	128 KB
μPD70F3828GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB
μPD70F3829GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB
μPD70F3826K8-6B4-AX	64-pin plastic WQFN (9 × 9)	64 KB
μPD70F3827K8-6B4-AX	64-pin plastic WQFN (9 × 9)	128 KB
μPD70F3828K8-6B4-AX	64-pin plastic WQFN (9 × 9)	256 KB
μPD70F3829K8-6B4-AX	64-pin plastic WQFN (9 × 9)	256 KB

- V850ES/JF3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3830GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	64 KB
μPD70F3831GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	128 KB
μPD70F3832GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	256 KB
μPD70F3833GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	256 KB

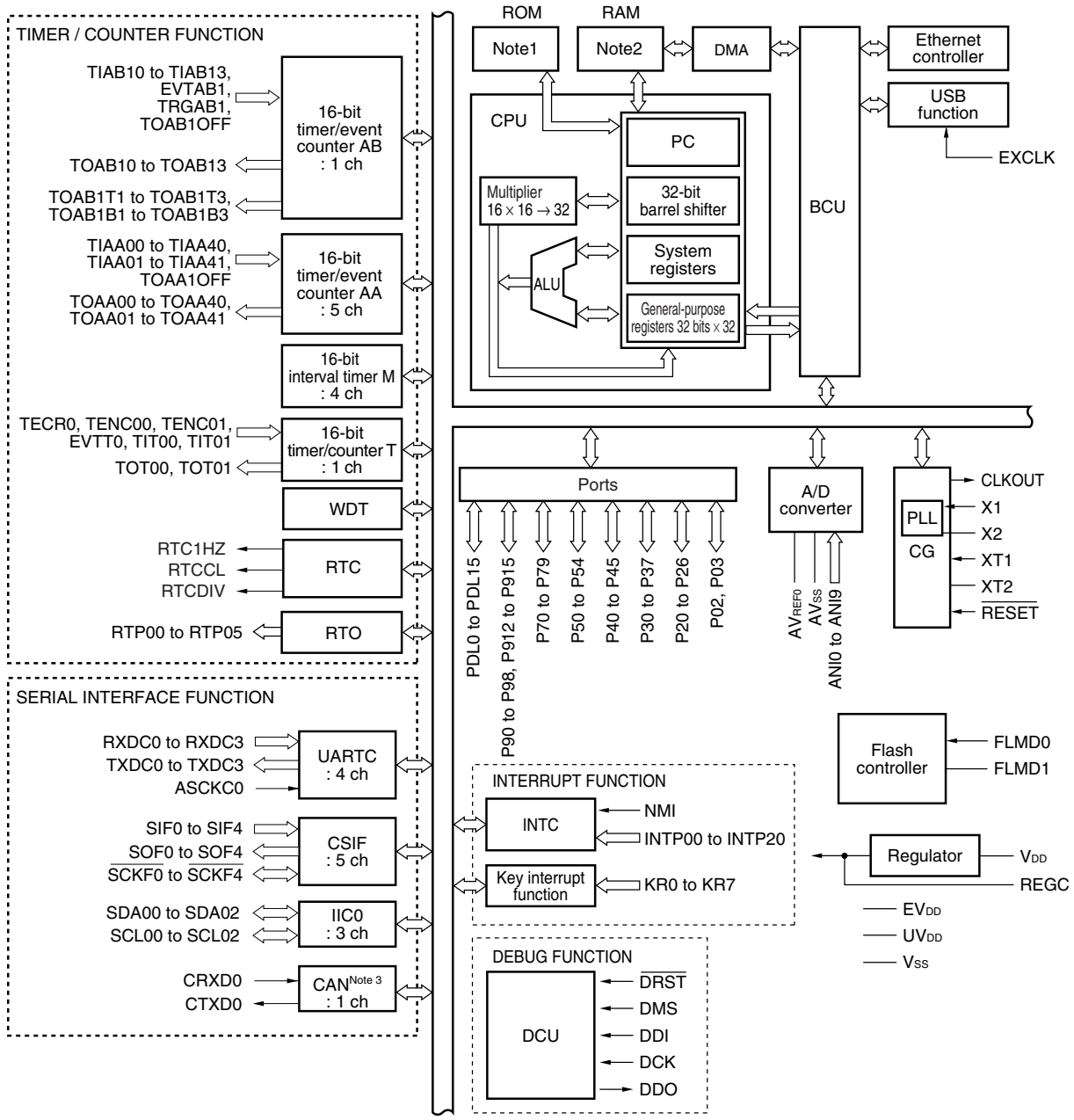
- V850ES/JG3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3834GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	64 KB
μPD70F3835GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	128 KB
μPD70F3836GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB
μPD70F3837GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB
μPD70F3837F1-CAH-AX[Note]	113-pin plastic FBGA (8 × 8)	256 KB

Note Under planning

Remark The V850ES/Jx3-E microcontrollers are lead-free products.

- **V850ES/JG3-E**



Notes 1. μPD70F3834: 64 KB
μPD70F3835: 128 KB
μPD70F3836, 70F3837: 256 KB

2. μPD70F3834: 32 KB (Including 16 KB of data RAM)
μPD70F3835: 48 KB (Including 16 KB of data RAM)
μPD70F3836, 70F3837: 64 KB (Including 16 KB of data RAM)

3. μPD70F3837 only.

(2/2)

Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
P70	I/O	Port 7 10-bit I/O port Input/output can be specified in 1-bit units.	ANI0	64	80	100
P71			ANI1	63	79	99
P72			ANI2	62	78	98
P73			ANI3	61	77	97
P74			ANI4	60	76	96
P75			ANI5	59	75	95
P76			ANI6	58	74	94
P77			ANI7	57	73	93
P78			ANI8	56	72	92
P79			ANI9	55	71	91
P90	I/O	Port 9 13-bit I/O port(V850ES/JG3-E) 11-bit I/O port(V850ES/JF3-E) Input/output can be specified in 1-bit units.	TOAB1T1/TOAB11/TIAB11/KR0/INTP12	–	57	72
P91			TOAB1B1/TIAB10/KR1/TOAB10	–	58	73
P92			TOAB1T2/TOAB12/TIAB12/KR2/INTP13	–	59	74
P93			TOAB1B2/TRGAB1/KR3/INTP14	–	60	75
P94			TOAB1T3/TOAB13/TIAB13/KR4/INTP15	–	61	76
P95			TOAB1B3/EVTB1/KR5/INTP16	–	62	77
P96			TECR0/TIT00/KR6/TOT00	–	31	40
P97			TENC00/TIT01/KR7/TOT01	–	32	41
P98			TENC01/INTP17	–	33	42
P912			TOAB1OFF/INTP18	–	63	78
P913			SIF31/INTP19	–	–	30
			INTP19	–	25	–
P914			SOF3/INTP20	–	–	31
P915			$\overline{\text{SCKF3}}$	–	–	32
PDL0	I/O	Port DL 11-bit I/O port(V850ES/JG3-E) 1-bit I/O port(V850ES/JF3-E, V850ES/JE3-E) Input/output can be specified in 1-bit units.	–	–	–	58
PDL1			–	–	–	59
PDL2			–	–	–	60
PDL3			–	–	–	66
PDL4			–	–	–	67
PDL5			FLMD1	49	64	79
PDL6			–	–	–	83
PDL7			–	–	–	84
PDL8			–	–	–	33
PDL9			–	–	–	34
PDL10			–	–	–	43

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Table 1-1. Types of Pin I/O Circuits (2/3)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JE3-E	JF3-E	JG3-E
P90	TOAB1T1/TOAB11/TIAB11/KR0 /INTP12	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	–	57	72
P91	TOAB1B1/TIAB10/KR1/TOAB10			–	58	73
P92	TOAB1T2/TOAB12/TIAB12/KR2 /INTP13			–	59	74
P93	TOAB1B2/TRGAB1/KR3/INTP14			–	60	75
P94	TOAB1T3/TOAB13/TIAB13/KR4 /INTP15			–	61	76
P95	TOAB1B3/EVTB1/KR5/INTP16			–	62	77
P96	TECR0/TIT00/KR6/TOT00			–	31	40
P97	TENC00/TIT01/KR7/TOT01			–	32	41
P98	TENC01/INTP17			–	33	42
P912	TOAB1OFF/INTP18			–	63	78
P913	SIF3/INTP19			–	–	30
	INTP19			–	25	–
P914	SOF3/INTP20			–	–	31
P915	$\overline{SCKF3}$			–	–	32
PDL0 to PDL4	–	5	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	–	–	58 to 67
PDL5	FLMD1	5		49	64	79
PDL6 to PDL10	–	5		–	–	83,84, 33,34, 43
AV_{REF0}	–	–	Directly connect to V_{DD} and always supply power.	1	1	1
AV_{SS}	–	–	Directly connect to V_{SS}.	2	2	2
EV_{DD}	–	–	Directly connect to V_{DD} and always supply power.	24, 44	29, 52	38, 65
FLMD0	–	–	Connect to V_{SS} in other than flash mode.	42	50	63
P1COL	–	5	Independently connect to EV_{DD} or V_{SS} via a resistor.	46	54	69
P1CRS	–	5		45	53	68
P1MDIO	–	5		47	55	70
P1RXCLK	–	5		48	56	71
P1RXD0	–	5		39	47	57
P1RXD1	–	5		33	41	51
P1RXD2	–	5		34	42	52
P1RXD3	–	5		35	43	53
P1RXDV	–	5		36	44	54
P1RXER	–	5		37	45	55
P1TXCLK	–	5		38	46	56
P1MDC	–	5	Leave open.	32	40	50
P1TXD0	–	5		26	34	44
P1TXD1	–	5		27	35	45
P1TXD2	–	5		28	36	46
P1TXD3	–	5		29	37	47
P1TXEN	–	5		31	39	49
P1TXER	–	5		30	38	48

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Table 1-1. Types of Pin I/O Circuits (3/3)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JE3-E	JF3-E	JG3-E
REGC	–	–	Connect to regulator output stabilization (4.7 μF (preliminary value)) capacitor.	6, 41	6, 49	9, 62
$\overline{\text{RESET}}$	–	2	–	10	10	13
UDMF	–	–	Leave open.	21	26	35
UDPF	–	–	Leave open.	22	27	36
UV_{DD}	–	–	Directly connect to V_{DD} and always supply power.	23	28	37
V_{DD}	–	–	–	5	5	8
V_{SS}	–	–	–	7	7	10
X1	–	–	–	8	8	11
X2	–	–	–	9	9	12
XT1	–	16-C	Connect to V_{SS} via a resistor.	8	11	14
XT2	–	16-C	Leave open.	9	12	15

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

8. 16-BIT TIMER/EVENT COUNTER T (TMT)

The number of TAB of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	1 channel (TMT0[Note])	1 channel (TMT0)	1 channel (TMT0)
Number of timer output	-	2	2

Note Interval timer function only.

The TMT function has the following features.

- 16 bit timer/counter (TMT)
- Clock selection: 8 ways
- Capture/trigger input pins (TIT00, TIT01) : 2
- External event count input pin[Note 1] : 1
- Encoder input pin (TENC00, TENC01) : 2
- Encoder clear input pin (TECR0) : 1
- External trigger input pin[Note 1]: 1
- Timer/counter: 1
- Capture/compare registers: 2
- Capture/compare match interrupt request signals: 2
- Timer output pins (TOT00, TOT01) : 2

The TMT function has the following features[Note 2].

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Triangular wave PWM output
- Encoder count function

Notes1. The external trigger input pin and the external event count input pin also function as the encoder input pin (TENC00)

2. The TMT0 function of V850ES/JE3-E is only Interval timer.

10. MOTOR CONTROL FUNCTION

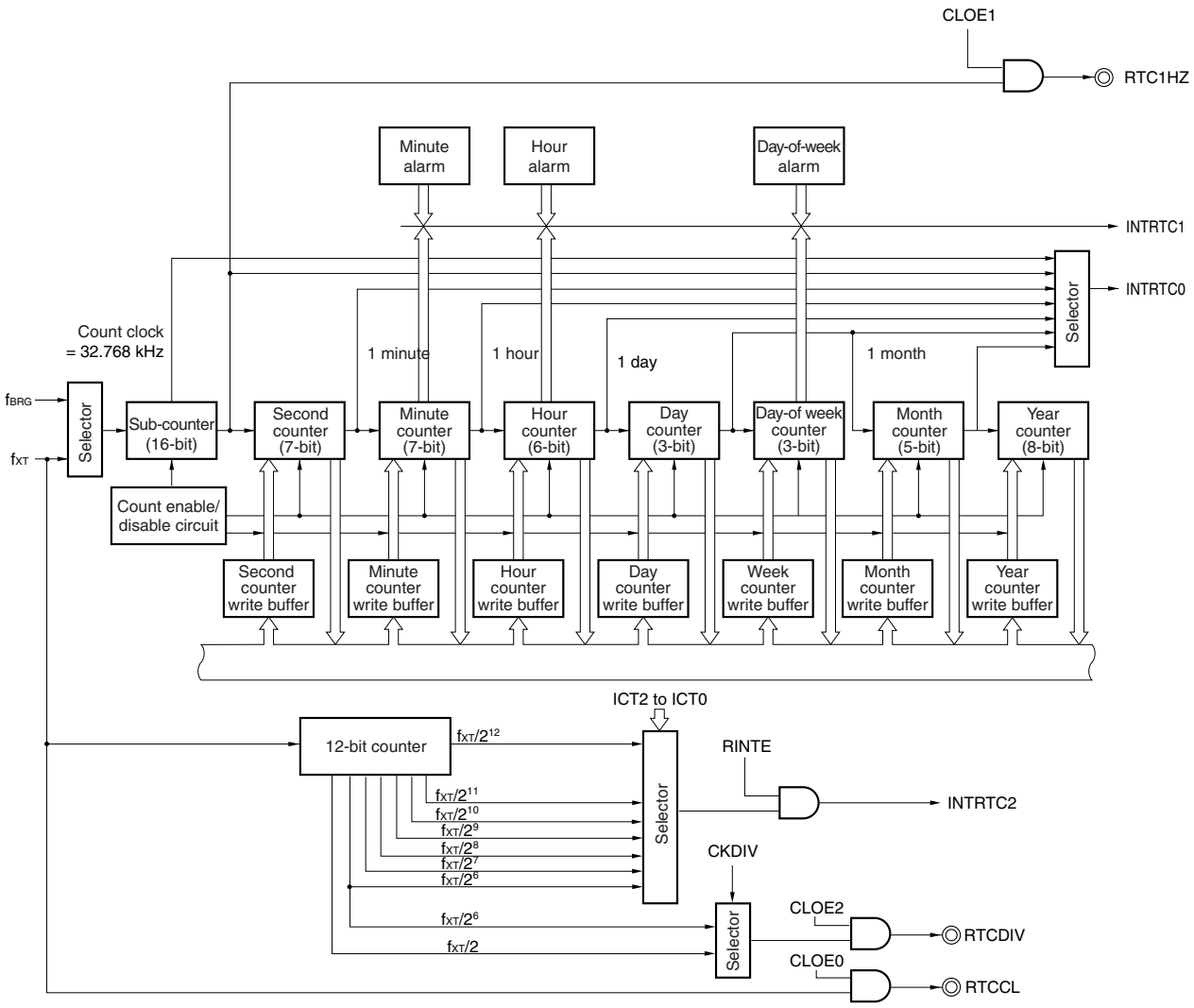
In the V850ES/JF3-E and V850ES/JG3-E, one channel of motor control function is provided.

Timer AB1 (TAB) and the TAB option (TABOP) can be used as an inverter function that controls a motor.

It performs a tuning operation with timer AA4 (TAA4) and A/D conversion of the A/D converter can be started when the value of TAB matches the value of TAA4. The following operations can be performed as motor control functions.

- 6-phase PWM output function with 16-bit resolution (with dead-timer, for upper and lower arms)
- Timer tuning operation function (tunable with TAA4)
- Cycle setting function (cycle can be changed during operation of crest or valley interrupt)
- Compare register rewriting: Anytime rewrite, batch rewrite, or intermittent rewrite
  (selectable during TAB operation)
- Interrupt and transfer culling functions
- Dead-time setting function
- A/D trigger timing function of the A/D converter (four types of timing can be generated)
- 0% output and 100% output available
- 0% output and 100% output selectable by crest interrupt and valley interrupt
- Forced output stop function
  - At valid edge detection by external pin input (INTP06/TOAA1OFF, INTP18/TOAB1OFF)
  - When stoppage of the main clock oscillation is detected by clock monitor function

The following figure shows the configuration of real-time timer.



Remark f_{BRG}: Real-time counter count clock frequency
f_{XT}: Subclock frequency
INTRTC0: Real-time counter fixed-cycle signal
INTRTC1: Real-time counter alarm match signal
INTRTC2: Real-time counter interval signal

15. ASYNCHRONOUS SERIAL INTERFACE C (UARTC)

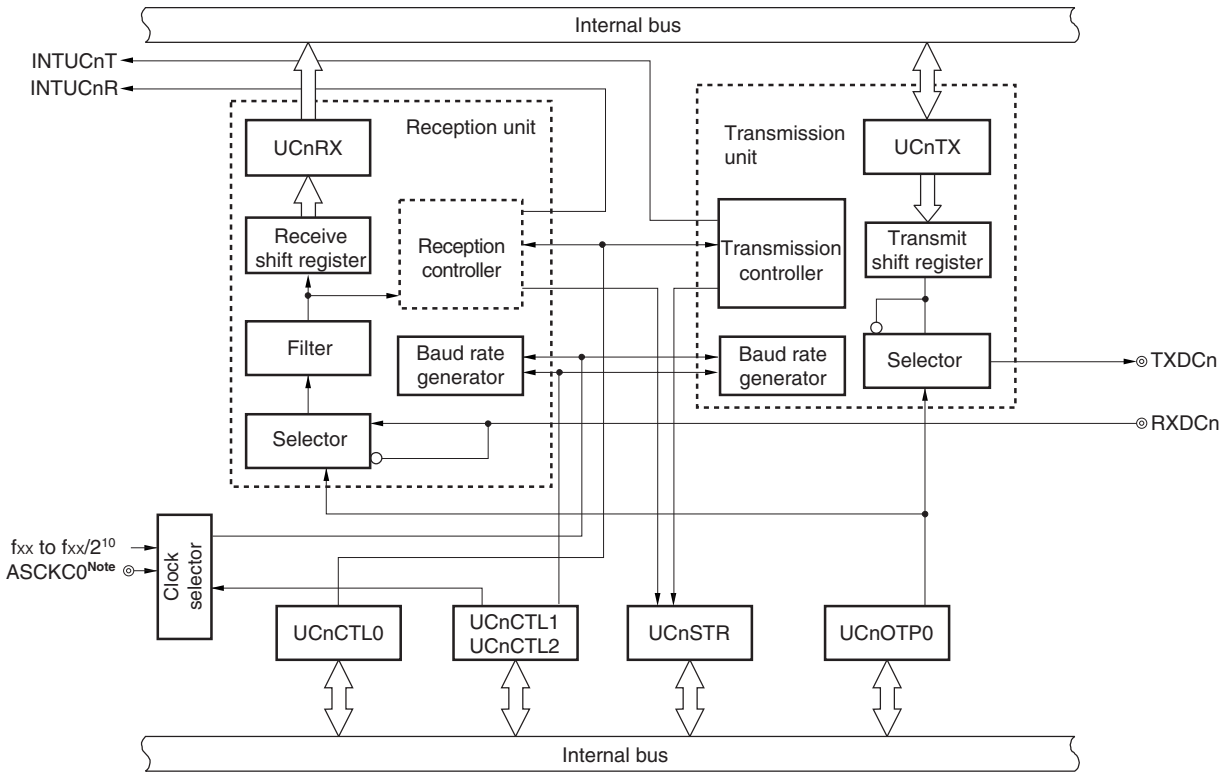
The number of UARTC of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	3 channels (UARTC0, UARTC2 and UARTC3)	4 channels (UARTC0 to UARTC3)	4 channels (UARTC0 to UARTC3)

The UARTC has the following features.

- Transfer rate: 300 bps to 3.125 Mbps (using internal system clock of 24 MHz and dedicated baud rate generator)
- Full-duplex communication: On-chip UARTCn receive data register (UCnRX)
  On-chip UARTCn transmit data register (UCnTX)
- 2-pin configuration: TXDCn: Transmit data output pin
  RXDCn: Receive data input pin
- Reception error detect function
  - Parity error
  - Framing error
  - Overrun error
  - LIN communication data consistency error detect function
  - SBF reception success detect function
- Interrupt sources: 2 types
  - Reception completion interrupt (INTUCnR): This interrupt occurs upon transfer of receive data from the receive shift register to receive data register after serial transfer completion, in the reception enabled status.
  - Transmission enable interrupt (INTUCnT): This interrupt occurs upon transfer of transmit data from the transmit data register to the transmit shift register in the transmission enabled status.
- Character length: 7, 8, 9 bits
- Parity function: Odd, even, 0, none
- Transmission stop bit: 1, 2 bits
- On-chip dedicated baud rate generator
- MSB-/LSB-first transfer selectable
- Transmit/receive data inverted input/output possible
- SBF (Sync Break Field) transmission/reception in the LIN (Local Interconnect Network) communication format possible
  - 13 to 20 bits are selectable for SBF transmission
  - Recognition of 11 bits or more possible for SBF reception in LIN format
  - SBF reception flag provided

The following figure shows the configuration of UARTC.



Note UARTC0 only

Remark fxx : Main clock frequency

16. CLOCKED SERIAL INTERFACE F (CSIF)

The number of CSIF of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	2 channels (CSIF0 and CSIF2)	3 channels (CSIF0 to CSIF2)	5 channels (CSIF0 to CSIF4)

- Transfer rate: 8 Mbps max. (f_{XX} = 50 MHz, using internal clock)
- Master mode and slave mode selectable
- 8-bit to 16-bit transfer, 3-wire serial interface
- Interrupt request signals (INTCFnT, INTCFnR)
- Serial clock and data phase switchable
- Transfer data length selectable in 1-bit units between 8 and 16 bits
- Transfer data MSB-first/LSB-first switchable
- 3-wire SOFn: Serial data output
  SIFn: Serial data input
  $\overline{\text{SCKFn}}$: Serial clock I/O

  Transmission mode, reception mode, and transmission/reception mode specifiable

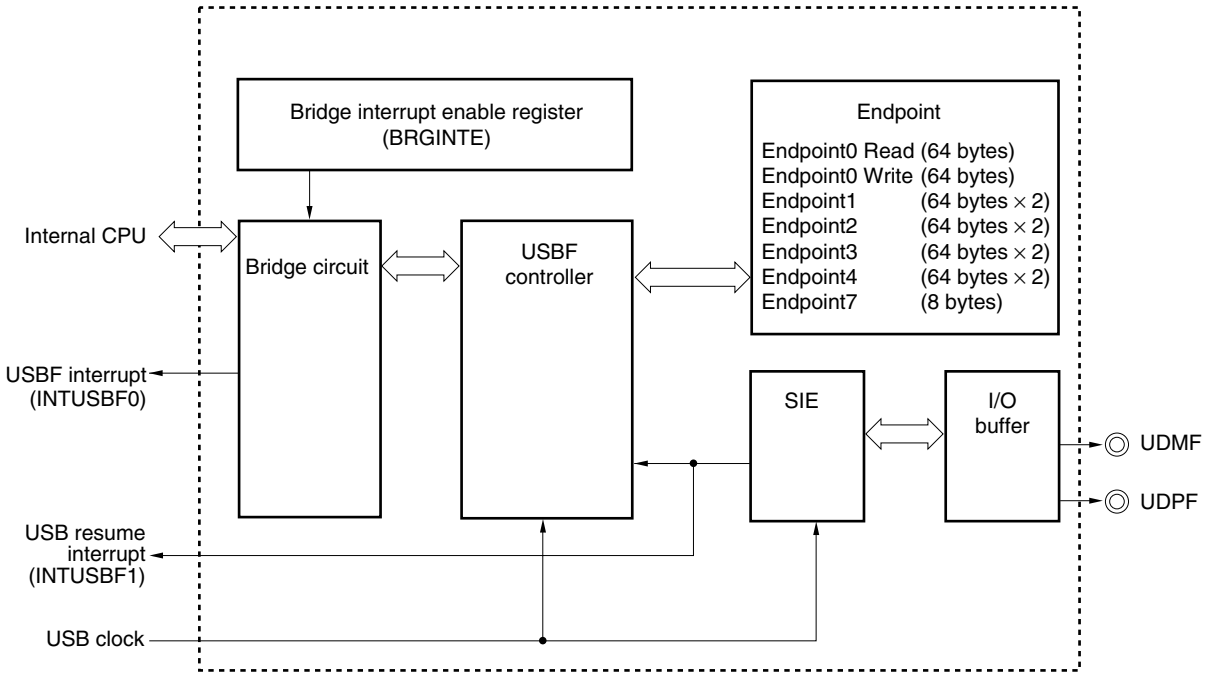
19. USB FUNCTION CONTROLLER (USBF)

In the V850ES/Jx3-E, one channel of USBF is provided.

- Conforms to the Universal Serial Bus (USB) Specification.
- USB 2.0-compatible full-speed transfer (12 Mbps) supported
- Endpoint for transfer incorporated

Endpoint Name	FIFO Size (Bytes)	Transfer Type	Remark
Endpoint0 Read	64	Control transfer	–
Endpoint0 Write	64	Control transfer	–
Endpoint1	64 × 2	Bulk 1 transfer (IN)	2-buffer configuration
Endpoint2	64 × 2	Bulk 1 transfer (OUT)	2-buffer configuration
Endpoint3	64 × 2	Bulk 2 transfer (IN)	2-buffer configuration
Endpoint4	64 × 2	Bulk 2 transfer (OUT)	2-buffer configuration
Endpoint7	8	Interrupt transfer (IN)	–

The following figure shows the configuration of USB function controller.



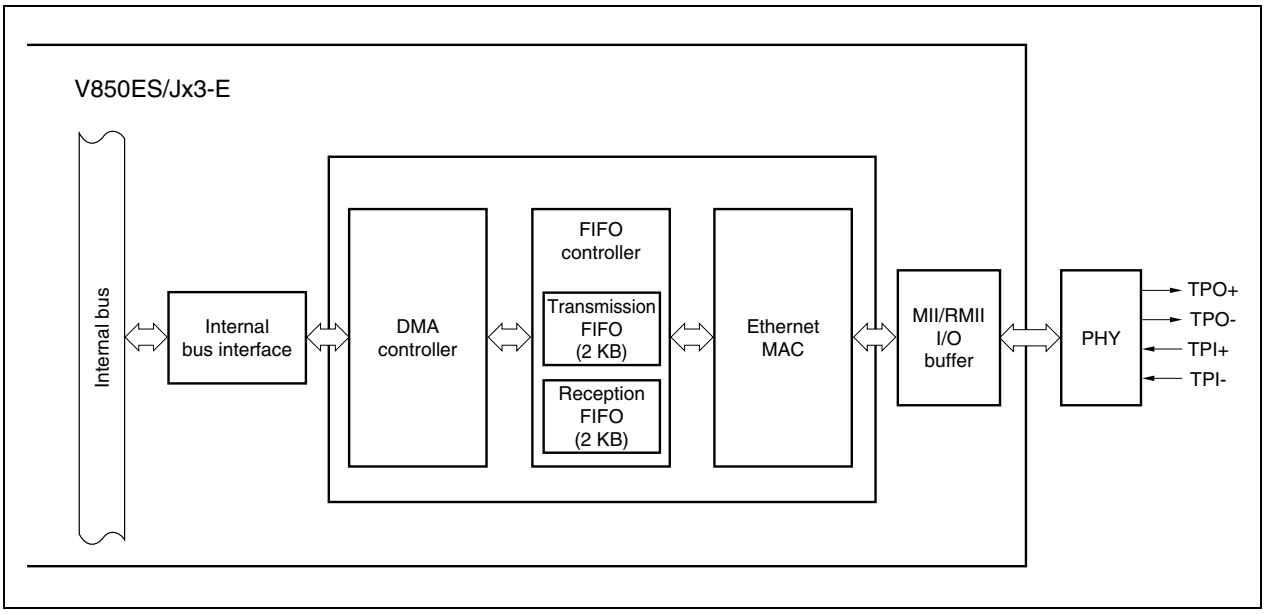
Remark Area enclosed with dashed line: Functions included in USB function controller

20. ETHERNET CONTROLLER

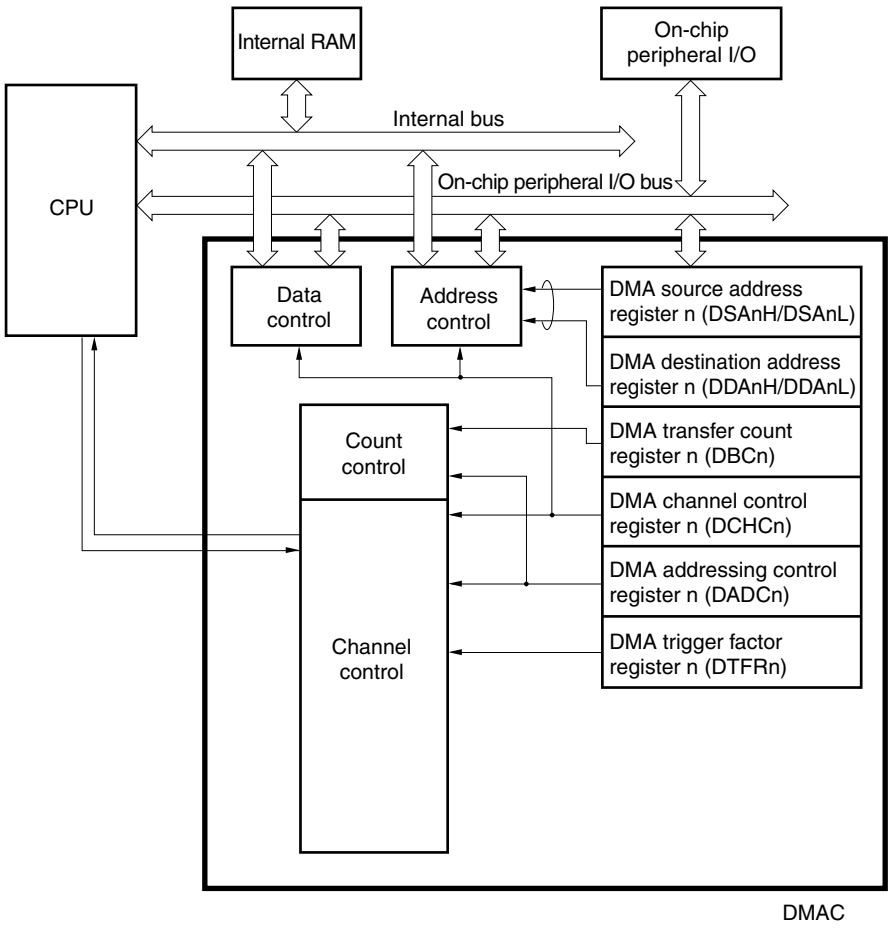
In the V850ES/Jx3-E, one channel of Ethernet controller is provided.

- 10 Mbps/100 Mbps MAC function conforming to the IEEE802.3 standard
  - Full-duplex and half-duplex communications and a flow control function are supported
  - On-chip packet filtering function based on address type
  - On-chip VLAN detection function
- Ethernet-dedicated DMA controller
  - Reception status DMA transfer possible
  - Reading (in pointer-chain format), analysis, and writing back of buffer descriptors possible
  - Interrupt control functions for packet transfers
- FIFO controller
  - Transmission/reception FIFO size: Transmission FIFO (2 KB), reception FIFO (2 KB)
  - On-chip FIFO status register
  - Interrupts occur in accordance with the transmission/reception status and FIFO status.
- MII is supported as the interface with physical-layer devices (PHY)
- On-chip reception checksum calculation function conforming to RFC1071

The following figure shows the configuration of USB function controller.



The following figure shows the configuration of DMA controller.



Remark n = 0 to 3

22. INTERRUPT/EXCEPTION PROCESSING FUNCTION

The features of interrupt/exception processing function is shown below.

○ Interrupts

		Internal			External		
		Non maskable	Maskable	Total	Non maskable	Maskable	Total
V850ES/JE3-E	μPD70F3826	1	53	54	1	6	7
	μPD70F3827	1	53	54	1	6	7
	μPD70F3828	1	53	54	1	6	7
	μPD70F3829	1	57	58	1	6	7
V850ES/JF3-E	μPD70F3830	1	56	57	1	18	19
	μPD70F3831	1	56	57	1	18	19
	μPD70F3832	1	56	57	1	18	19
	μPD70F3833	1	60	61	1	18	19
V850ES/JG3-E	μPD70F3834	1	60	61	1	21	22
	μPD70F3835	1	60	61	1	21	22
	μPD70F3836	1	60	61	1	21	22
	μPD70F3837	1	64	65	1	21	22

- 8 levels of programmable priorities
- Masks interrupt requests according to priority
- Masks can be specified for each maskable interrupt request.
- Noise elimination, edge detection, and valid edge specification for external interrupt request signals.

○ Exceptions

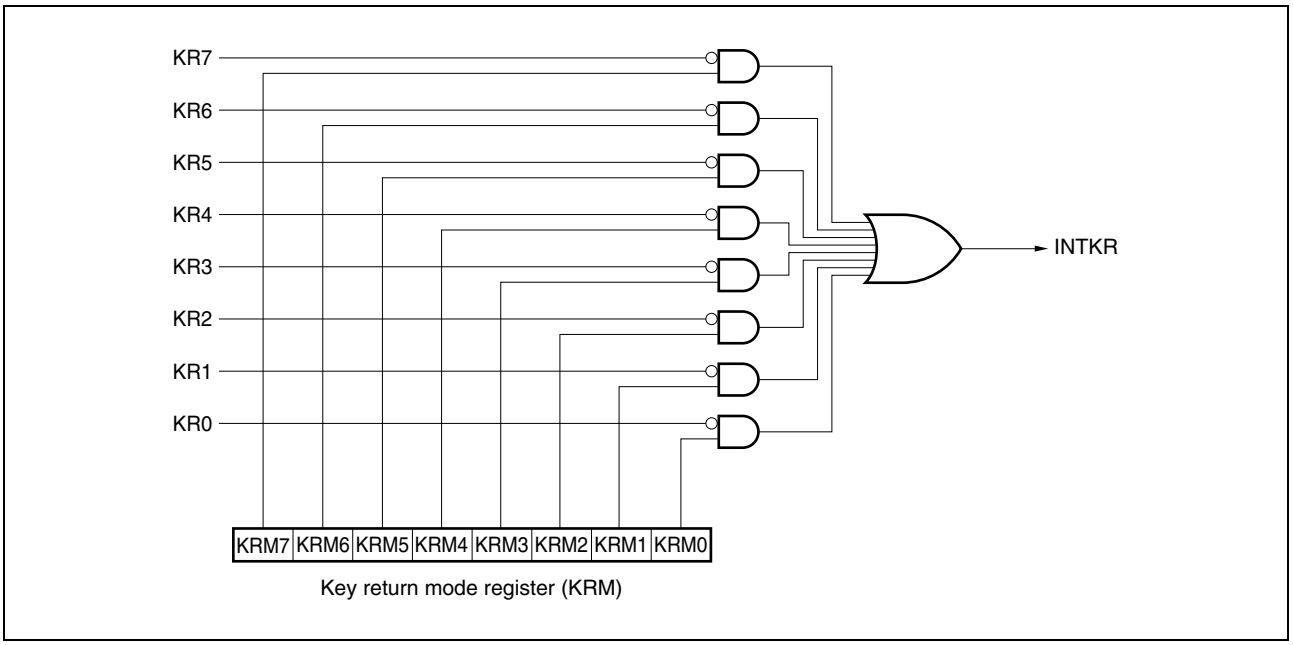
- Software exceptions: 32 sources
- Exception trap: 2 sources (illegal opcode exception, debug trap)

Interrupt/exception sources are listed in Table 22-1.

23. KEY INTERRUPT FUNCTION (V850ES/JF3-E, V850ES/JG3-E)

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins (KR0 to KR7).

The following figure shows the configuration of key interrupt.



26. CLOCK MONITOR, LOW-VOLTAGE DETECTOR

(1) Clock monitor

The clock monitor samples the main clock by using the internal oscillation clock (f_R) and generates a reset request signal when oscillation of the main clock is stopped.

(2) Low-voltage detector

The low-voltage detector (LVI) has the following functions.

- Compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}) and generates an interrupt request signal or internal reset signal when $V_{DD} < V_{LVI}$.
- An interrupt request signal or internal reset signal can be selected.
- Can operate in STOP mode.
- Operation can be stopped by software.

29. FLASH MEMORY

Flash memory versions offer the following advantages for development environments and mass production applications.

- For altering software after the V850ES/Jx3-E is soldered onto the target system.
- For data adjustment when starting mass production.
- For differentiating software according to the specification in small scale production of various models.
- For facilitating inventory management.
- For updating software after shipment.

The flash memory in the V850ES/Jx3-E has the following features.

- 4-byte/1-clock access (when instruction is fetched)
- Memory size: 64/128/256 KB
- Rewrite voltage: Erase/write with a single power supply
- Rewriting method
  - Rewriting by communication with dedicated flash programmer via serial interface (on-board/off-board programming)
  - Rewriting flash memory by user program (self programming)
- Flash memory write prohibit function supported (security function)
- Safe rewriting of entire flash memory area by self programming using boot swap function
- Interrupts can be acknowledged during self programming.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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