Renesas Electronics America Inc - UPD70F3827GB(R)-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, CSI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	26
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3827gb-r-gah-ax

Function list (V850ES/JF3-E)

Generic Name		V850ES/JF3-E			
Product Name		μPD70F3830	μPD70F3831	μPD70F3832	μPD70F3833
Internal memory	Flash memory	64 KB	128 KB	256 KB	256 KB
	Internal RAM	16 KB	32 KB	48 KB	48 KB
	Data RAM	16 KB	16 KB	16 KB	16 KB
Memory space		64 MB			
General-purpose register		32 bits × 32 registers			
Clocks	Main clock oscillation	PLL mode : f_X = 3 to 6.25 MHz, f_{XX} = 24 to 50 MHz (multiplication by 8) Clock through mode : f_X = 3 to 6.25 MHz (internal : f_{XX} = 3 to 6.25 MHz)			
	Subclock oscillation	f_{XT} = 32.768 kHz			
	Internal oscillation	f_R = 220 kHz (TYP.)			
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{XX}))			
I/O ports		I/O: 42 (5 V tolerant : 28)			
Timer	16-bit TAA	5 channels			
	16-bit TAB	1 channel			
	16-bit TMM	4 channels			
	16-bit TMT	1 channel			
	Motor control	1 channel			
	Watch timer	1 channel (RTC)			
	WDT	1 channel			
Real-time output function		6 bits × 1 channel			
10-bit A/D converter		10 channels			
Serial interface	CSIF/UARTC	1 channel			
	CSIF/UARTC/I²C	2 channels			
	CSIF	–			
	UARTC/I²C	1 channel			–
	UARTC/I²C/CAN	–			1 channel
USB function		1 channel			
Ethernet controller		1 channel			
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)			
Interrupt source	External Note 1, 2	19(19)	19(19)	19(19)	19(19)
	Internal	57	57	57	61
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes			
Reset factor		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)			
On-chip debugging		MINICUBE, MINICUBE2 supported			
Operating supply voltage		2.85 to 3.6 V			
Operating ambient temperature		–40 to +85°C			
Package		80-pin plastic LQFP (fine pitch) (12 × 12 mm)			

Notes 1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.

2. Include NMI.

Function list (V850ES/JG3-E)

Generic Name		V850ES/JG3-E			
Product Name		μPD70F3834	μPD70F3835	μPD70F3836	μPD70F3837
Internal memory	Flash memory	64 KB	128 KB	256 KB	256 KB
	Internal RAM	16 KB	32 KB	48 KB	48 KB
	Data RAM	16 KB	16 KB	16 KB	16 KB
Memory space		64 MB			
General-purpose register		32 bits × 32 registers			
Clocks	Main clock oscillation	PLL mode : f_X = 3 to 6.25 MHz, f_{XX} = 24 to 50 MHz (multiplication by 8) Clock through mode : f_X = 3 to 6.25 MHz (internal : f_{XX} = 3 to 6.25 MHz)			
	Subclock oscillation	f_{XT} = 32.768 kHz			
	Internal oscillation	f_R = 220 kHz (TYP.)			
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{XX}))			
I/O ports		I/O: 62 (5 V tolerant : 35)			
Timer	16-bit TAA	5 channels			
	16-bit TAB	1 channel			
	16-bit TMM	4 channels			
	16-bit TMT	1 channel			
	Motor control	1 channel			
	Watch timer	1 channel (RTC)			
	WDT	1 channel			
Real-time output function		6 bits × 1 channel			
10-bit A/D converter		10 channels			
Serial interface	CSIF/UARTC	1 channel			
	CSIF/UARTC/I²C	2 channels			
	CSIF	2 channels			
	UARTC/I²C	1 channel			–
	UARTC/I²C/CAN	–			1 channel
USB function		1 channel			
Ethernet controller		1 channel			
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)			
Interrupt source	External Note 1, 2	22(22)	22(22)	22(22)	22(22)
	Internal	61	61	61	65
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes			
Reset factor		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)			
On-chip debugging		MINICUBE, MINICUBE2 supported			
Operating supply voltage		2.85 to 3.6 V			
Operating ambient temperature		–40 to +85°C			
Package		100-pin plastic LQFP (fine pitch) (14 × 14 mm), 113-pin plastic FBGA Note3			

Notes 1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.

2. Include NMI.

3. Under planning.

APPLICATIONS

○ Applications that require Ethernet controller

Home audio, printers, and scanners.

ORDERING INFORMATION

- V850ES/JE3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3826GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	64 KB
μPD70F3827GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	128 KB
μPD70F3828GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB
μPD70F3829GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB
μPD70F3826K8-6B4-AX	64-pin plastic WQFN (9 × 9)	64 KB
μPD70F3827K8-6B4-AX	64-pin plastic WQFN (9 × 9)	128 KB
μPD70F3828K8-6B4-AX	64-pin plastic WQFN (9 × 9)	256 KB
μPD70F3829K8-6B4-AX	64-pin plastic WQFN (9 × 9)	256 KB

- V850ES/JF3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3830GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	64 KB
μPD70F3831GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	128 KB
μPD70F3832GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	256 KB
μPD70F3833GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	256 KB

- V850ES/JG3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3834GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	64 KB
μPD70F3835GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	128 KB
μPD70F3836GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB
μPD70F3837GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB
μPD70F3837F1-CAH-AX[Note]	113-pin plastic FBGA (8 × 8)	256 KB

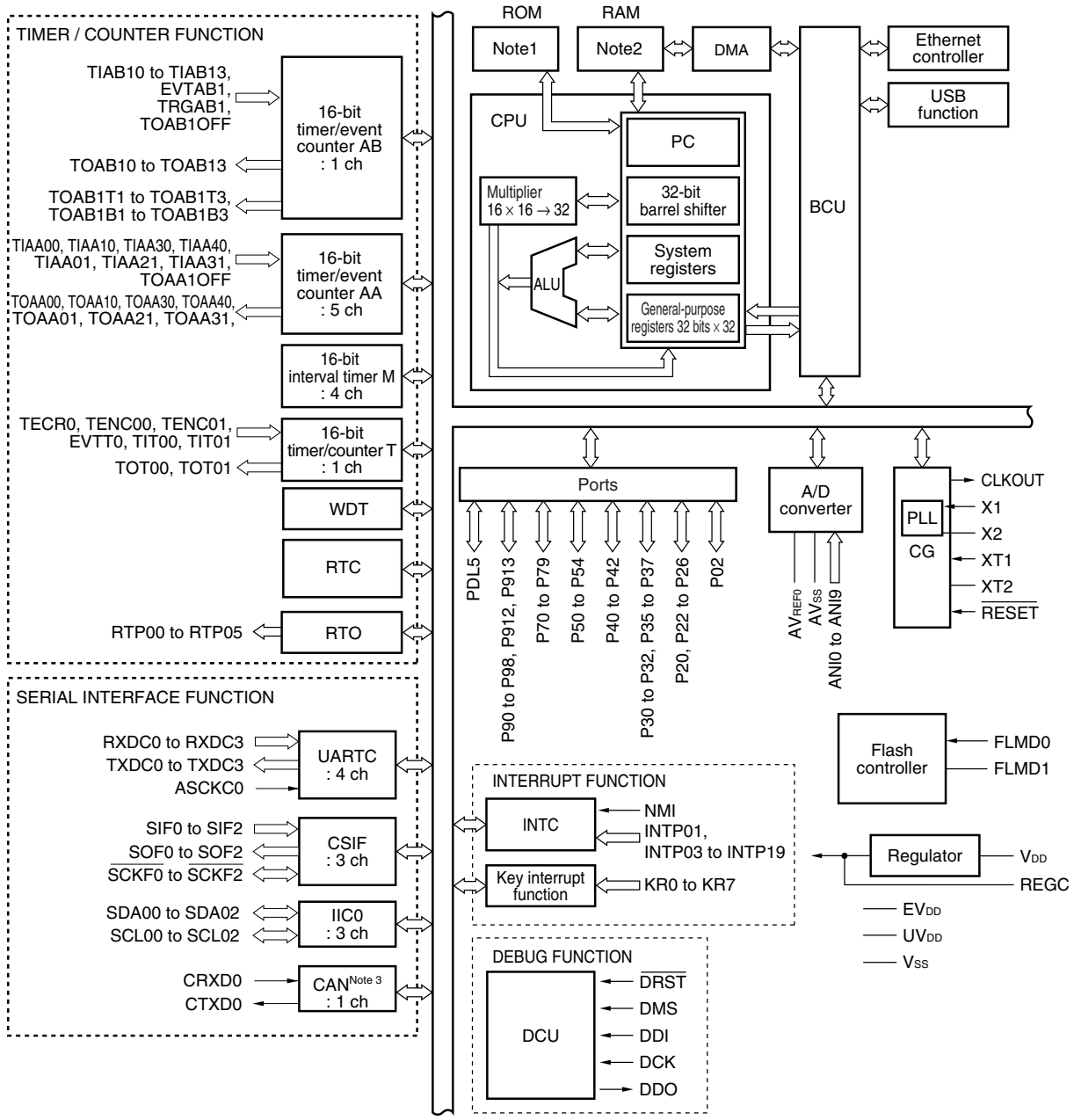
Note Under planning

Remark The V850ES/Jx3-E microcontrollers are lead-free products.

PIN IDENTIFICATION

ADTRG:	A/D Trigger Input
ANI0 to ANI9:	Analog Input
ASCKC0:	Asynchronous Serial Clock
AV_{REF0}:	Analog Reference Voltage
AV_{SS}:	Grand for Analog Pin
CRXD0:	CAN Receive Data
CTXD0:	CAN Transmit Data
DCK:	Debug Clock
DDI:	Debug Data Input
DDO:	Debug Data Output
DMS:	Debug Mode Select
$\overline{DRST}$:	Debug Reset
EV_{DD}:	Power Supply for External Pin
EVTAB1:	Timer Event Count Input
EXCLK	USB clock
FLMD0, FLMD1:	Flash Programming Mode
INTP00 to INTP20:	External Interrupt Input
KR0 to KR7:	Key Return
NMI:	Non-maskable Interrupt Request
P02, P03:	Port0
P1COL, P1CRS, P1MDC, P1MDIO, P1RXCLK, P1RXD0 to P1RXD3, P1RXDV, P1RXER P1TXCLK, P1TXD0 to P1TXD3, P1TXEN, P1TXER:	Ethernet PHY Interface
P20 to P26	Port2
P30 to P37:	Port3
P40 to P45:	Port4
P50 to P54:	Port5
P70 to P79:	Port7
P90 to P98, P912 to P915:	Port9
PDL0 to PDL10:	Port DL
REGC:	Regulator Control
$\overline{RESET}$:	Reset
RTC1HZ, RTCCL, RTCDIV:	Real-time Counter Clock Output
RTP00 to RTP05:	Real-time Output Port
RXDC0 to RXDC3	Receive Data
$\overline{SCKF0}$ to $\overline{SCKF4}$:	Serial Clock
SCL00 to SCL02:	Serial Clock
SDA00 to SDA02:	Serial Data
SIF0 to SIF4:	Serial Input
SOF0 to SOF4:	Serial Output
TECR0:	Timer Encoder Clear Input
TENC00, TENC01:	Timer Encoder Input
TIAA00, TIAA01, TIAA10, TIAA11, TIAA20, TIAA21, TIAA30, TIAA31, TIAA40, TIAA41, TIAB10 to TIAB13, TIT00, TIT01:	Timer Input
TOAA00, TOAA01, TOAA10, TOAA11, TOAA20, TOAA21, TOAA30, TOAA31, TOAA40, TOAA41, TOAB10 to TOAB13, TOAB1B1 to TOAB1B3, TOAB1T1 to TOAB1T3, TOT00, TOT01:	Timer Output
TOAA1OFF, TOAB1OFF	Timer Output Off
TRGAB1:	Timer Trigger Input
TXDC0 to TXDC3:	Serial Output
UDMF:	USB Data I/O (-) Function
UDPF:	USB Data I/O (+) Function
UV_{DD}:	Power Supply for External USB
V_{DD}:	Power Supply
V_{SS}:	Ground
X1, X2:	Crystal for Main Clock
XT1, XT2:	Crystal for Sub-clock

- **V850ES/JF3-E**



Notes 1. μPD70F3830: 64 KB
μPD70F3831: 128 KB
μPD70F3832, 70F3833: 256 KB

2. μPD70F3830: 32 KB (Including 16 KB of data RAM)
μPD70F3831: 48 KB (Including 16 KB of data RAM)
μPD70F3832, 70F3833: 64 KB (Including 16 KB of data RAM)

3. μPD70F3833 only.

CONTENTS

1. PIN FUNCTIONS

1.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
P02	I/O	Port 0 2-bit I/O port(V850ES/JG3-E) 1-bit I/O port(V850ES/JE3-E, V850ES/JF3-E) Input/output can be specified in 1-bit units.	NMI	3	3	3
P03			INTP00/ADTRG/EXCLK	–	–	4
P20	I/O	Port 2 7-bit I/O port(V850ES/JG3-E) 5-bit I/O port(V850ES/JF3-E) 1-bit I/O port(V850ES/JE3-E) Input/output can be specified in 1-bit units.	INTP01	4	4	5
P21			RTGDIV/RTCCL	–	–	6
P22			RTC1HZ/INTP02	–	–	7
P23			SIF1/TXDC1/SDA00/INTP03	–	13	16
P24			SOF1/RXDC1/SDL00/INTP04	–	14	17
P25			$\overline{\text{SCKF}}$1/TIAA30/TOAA30	–	15	18
P26			TIAA31/TOAA31/INTP05	–	16	19
P30	I/O	Port 3 8-bit I/O port(V850ES/JG3-E) 6-bit I/O port(V850ES/JF3-E) 5-bit I/O port(V850ES/JE3-E) Input/output can be specified in 1-bit units.	TXDC0/SIF2/TIAA00/TOAA00	13	17	20
P31			RXDC0/SOF2/TIAA01/TOAA01	14	18	21
P32			ASCKC0/$\overline{\text{SCKF2}}$/TIAA10/TOAA10	15	19	22
P33			SIF4/TIAA11/TOAA11	–	–	23
P34			SOF4/TIAA20/TOAA20	–	–	24
P35			$\overline{\text{SCKF4}}$/TIAA21/TOAA21 /TOAA1OFF/INTP06	–	–	80
			TIAA21/TOAA21/TOAA1OFF/INTP06	–	65	–
P36			TXDC2/SDA02/CTXD0[Note]	50	66	81
P37			RXDC2/SCL02/CRXD0[Note]	51	67	82
P40	I/O	Port 4 6-bit I/O port(V850ES/JG3-E) 3-bit I/O port(V850ES/JE3-E, V850ES/JF3-E) Input/output can be specified in 1-bit units.	SIF0/TXDC3/SDA01/RTP00	52	68	85
P41			SOF0/RXDC3/SCL01/RTP01	53	69	86
P42			$\overline{\text{SCKF0}}$/TIAA40/TOAA40/RTP02	54	70	87
P43			RTP03	–	–	88
P44			RTP04	–	–	89
P45			TIAA41/TOAA41/RTP05	–	–	90
P50	I/O	Port 5 5-bit I/O port Input/output can be specified in 1-bit units.	INTP07/DDI	16	20	25
P51			INTP08/DDO	17	21	26
P52			INTP09/DCK	18	22	27
P53			INTP10/DMS	19	23	28
P54			INTP11/$\overline{\text{DRST}}$	20	24	29

Note Available only in on-chip CAN controller products

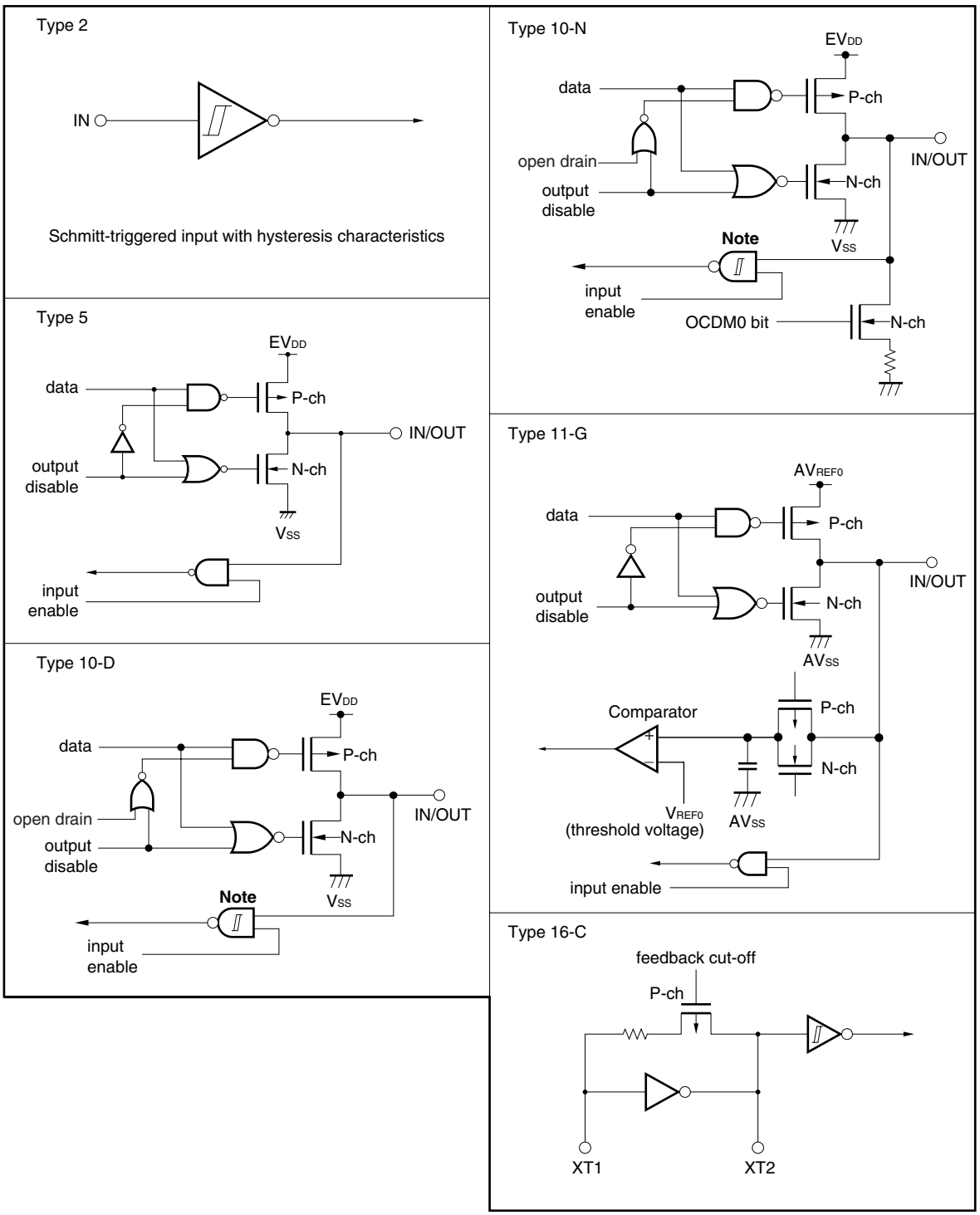
Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

(2/2)

Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
P70	I/O	Port 7 10-bit I/O port Input/output can be specified in 1-bit units.	ANI0	64	80	100
P71			ANI1	63	79	99
P72			ANI2	62	78	98
P73			ANI3	61	77	97
P74			ANI4	60	76	96
P75			ANI5	59	75	95
P76			ANI6	58	74	94
P77			ANI7	57	73	93
P78			ANI8	56	72	92
P79			ANI9	55	71	91
P90	I/O	Port 9 13-bit I/O port(V850ES/JG3-E) 11-bit I/O port(V850ES/JF3-E) Input/output can be specified in 1-bit units.	TOAB1T1/TOAB11/TIAB11/KR0/INTP12	–	57	72
P91			TOAB1B1/TIAB10/KR1/TOAB10	–	58	73
P92			TOAB1T2/TOAB12/TIAB12/KR2/INTP13	–	59	74
P93			TOAB1B2/TRGAB1/KR3/INTP14	–	60	75
P94			TOAB1T3/TOAB13/TIAB13/KR4/INTP15	–	61	76
P95			TOAB1B3/EVTB1/KR5/INTP16	–	62	77
P96			TECR0/TIT00/KR6/TOT00	–	31	40
P97			TENC00/TIT01/KR7/TOT01	–	32	41
P98			TENC01/INTP17	–	33	42
P912			TOAB1OFF/INTP18	–	63	78
P913			SIF31/INTP19	–	–	30
			INTP19	–	25	–
P914			SOF3/INTP20	–	–	31
P915			$\overline{\text{SCKF3}}$	–	–	32
PDL0	I/O	Port DL 11-bit I/O port(V850ES/JG3-E) 1-bit I/O port(V850ES/JF3-E, V850ES/JE3-E) Input/output can be specified in 1-bit units.	–	–	–	58
PDL1			–	–	–	59
PDL2			–	–	–	60
PDL3			–	–	–	66
PDL4			–	–	–	67
PDL5			FLMD1	49	64	79
PDL6			–	–	–	83
PDL7			–	–	–	84
PDL8			–	–	–	33
PDL9			–	–	–	34
PDL10			–	–	–	43

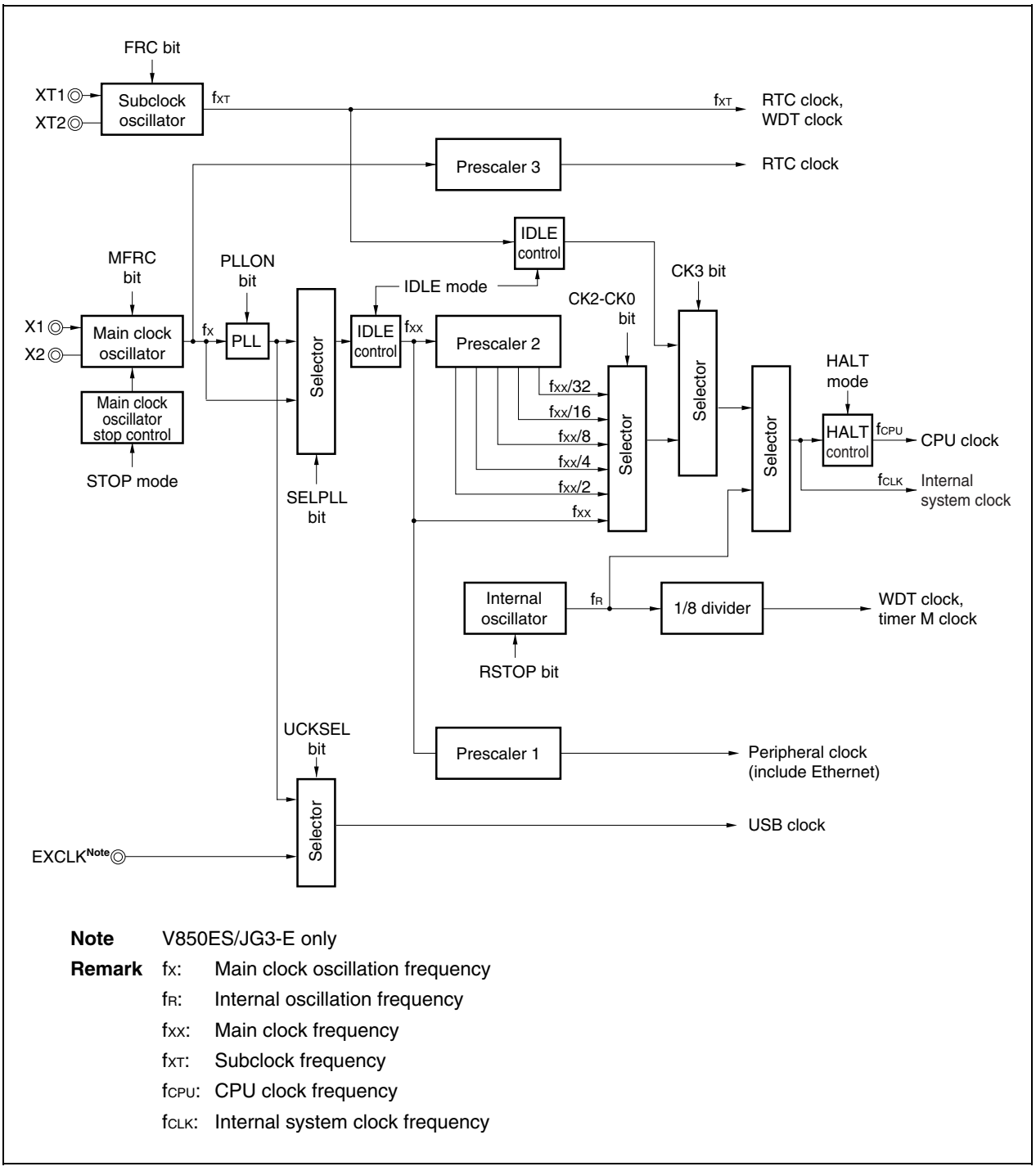
Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Figure 1-1. Pin I/O Circuits



Note Hysteresis characteristics are not available in port mode.

The following figure shows the configuration of the clock generation function.



Note V850ES/JG3-E only

Remark f_X: Main clock oscillation frequency
f_R: Internal oscillation frequency
f_{XX}: Main clock frequency
f_{XT}: Subclock frequency
f_{CPU}: CPU clock frequency
f_{CLK}: Internal system clock frequency

7. 16-BIT TIMER/EVENT COUNTER AB (TAB)

The number of TAB of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	1 channel (TAB1[Note])	1 channel (TAB1)	1 channel (TAB1)
Number of timer output	-	4	4

Note Interval timer function only.

The TAB function has the following features.

- 16-bit timer/counter (TAB1)
- Clock selection: 8 ways
- Capture/trigger input pins (TIAB10 to TIAB13): 4
- External event count input pin (EVTAB1): 1
- External trigger input pin (TRGAB1): 1
- Timer/counter: 1
- Capture/compare registers: 4
- Capture/compare match interrupt request signals: 4
- Timer output pins (TOAB10 to TOAB13): 4

The TAB1 function has the following features.

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Triangular wave PWM output
- Timer tuning function

14. A/D CONVERTER

An A/D converter unit with ten channels is provided in the V850ES/Jx3-E.

The A/D converter has the following features.

- 10-bit resolution
- 10 channels
- Successive approximation method
- Operating voltage: AV_{REF0} = 3.0 to 3.6 V
- Analog input voltage: 0 V to AV_{REF0}
- The following functions are provided as operation modes.
  - Continuous select mode
  - Continuous scan mode
  - One-shot select mode
  - One-shot scan mode
- The following functions are provided as trigger modes.
  - Software trigger mode
  - External trigger mode (external, 1)
  - Timer trigger mode
- Power-fail monitor function (conversion result compare function)

16. CLOCKED SERIAL INTERFACE F (CSIF)

The number of CSIF of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	2 channels (CSIF0 and CSIF2)	3 channels (CSIF0 to CSIF2)	5 channels (CSIF0 to CSIF4)

- Transfer rate: 8 Mbps max. (f_{XX} = 50 MHz, using internal clock)
- Master mode and slave mode selectable
- 8-bit to 16-bit transfer, 3-wire serial interface
- Interrupt request signals (INTCFnT, INTCFnR)
- Serial clock and data phase switchable
- Transfer data length selectable in 1-bit units between 8 and 16 bits
- Transfer data MSB-first/LSB-first switchable
- 3-wire SOFn: Serial data output
  SIFn: Serial data input
  $\overline{\text{SCKFn}}$: Serial clock I/O

  Transmission mode, reception mode, and transmission/reception mode specifiable

22. INTERRUPT/EXCEPTION PROCESSING FUNCTION

The features of interrupt/exception processing function is shown below.

○ Interrupts

		Internal			External		
		Non maskable	Maskable	Total	Non maskable	Maskable	Total
V850ES/JE3-E	μPD70F3826	1	53	54	1	6	7
	μPD70F3827	1	53	54	1	6	7
	μPD70F3828	1	53	54	1	6	7
	μPD70F3829	1	57	58	1	6	7
V850ES/JF3-E	μPD70F3830	1	56	57	1	18	19
	μPD70F3831	1	56	57	1	18	19
	μPD70F3832	1	56	57	1	18	19
	μPD70F3833	1	60	61	1	18	19
V850ES/JG3-E	μPD70F3834	1	60	61	1	21	22
	μPD70F3835	1	60	61	1	21	22
	μPD70F3836	1	60	61	1	21	22
	μPD70F3837	1	64	65	1	21	22

- 8 levels of programmable priorities
- Masks interrupt requests according to priority
- Masks can be specified for each maskable interrupt request.
- Noise elimination, edge detection, and valid edge specification for external interrupt request signals.

○ Exceptions

- Software exceptions: 32 sources
- Exception trap: 2 sources (illegal opcode exception, debug trap)

Interrupt/exception sources are listed in Table 22-1.

Table 22-1. Interrupt Source List (2/3

Type	Classification	Default Priority	Name	Trigger	Generating Unit	Interrupt Control Register	JE3E	JF3E	JG3E
Maskable	Interrupt	41	INTTAA0OV	TAA0 overflow	TAA0	TAA0OVIC	√	√	√
		42	INTTAA0CC0	TAA0 capture 0/compare 0 match	TAA0	TAA0CCIC0	√	√	√
		43	INTTAA0CC1	TAA0 capture 1/compare 1 match	TAA0	TAA0CCIC1	√	√	√
		44	INTTAA1OV	TAA1 overflow	TAA1	TAA1OVIC	√	√	√
		45	INTTAA1CC0	TAA1 capture 0/compare 0 match	TAA1	TAA1CCIC0	√	√	√
		46	INTTAA1CC1	TAA1 capture 1/compare 1 match	TAA1	TAA1CCIC1	√	√	√
		47	INTTAA2OV	TAA2 overflow	TAA2	TAA2OVIC	√	√	√
		48	INTTAA2CC0	TAA2 capture 0/compare 0 match	TAA2	TAA2CCIC0	√	√	√
		49	INTTAA2CC1	TAA2 capture 1/compare 1 match	TAA2	TAA2CCIC1	√	√	√
		50	INTTAA3OV	TAA3 overflow	TAA3	TAA3OVIC	√	√	√
		51	INTTAA3CC0	TAA3 capture 0/compare 0 match	TAA3	TAA3CCIC0	√	√	√
		52	INTTAA3CC1	TAA3 capture 1/compare 1 match	TAA3	TAA3CCIC1	√	√	√
		53	INTTAA4OV	TAA4 overflow	TAA4	TAA4OVIC	√	√	√
		54	INTTAA4CC0	TAA4 capture 0/compare 0 match	TAA4	TAA4CCIC0	√	√	√
		55	INTTAA4CC1	TAA4 capture 1/compare 1 match	TAA4	TAA4CCIC1	√	√	√
		59	INTTM0EQ0	TMM0 compare match	TMM0	TM0EQIC0	√	√	√
		60	INTTM1EQ0	TMM1 compare match	TMM1	TM1EQIC0	√	√	√
		61	INTTM2EQ0	TMM2 compare match	TMM2	TM2EQIC0	√	√	√
		62	INTTM3EQ0	TMM3 compare match	TMM3	TM3EQIC0	√	√	√
		67	INTCF0R /INTUC3R /INTIIC1	CSIF0 transfer completion/UARTC3 reception completion/UARTC3 reception error/IIC1 transfer completion	CSIF0 /UARTC3 /IIC1	CE0RIC /UC3RIC /IICIC1	√	√	√
		68	INTCF0T /INTUC3T	CSIF0 continuous transfer write enable/ UARTC3 continuous transfer write enable	CSIF0 /UARTC3	CF0TIC /UC3TIC	√	√	√
		69	INTCF1R /INTUC1R /INTIIC0	CSIF1 reception completion/ CSIF1 reception error /UARTC1 reception completion/UARTC1 reception error/IIC0 transfer completion	CSIF1 /UARTC1 /IIC0	CF1RIC /UC1RIC /IICIC0	–	–	√
		70	INTCF1T /INTUC1T	CSIF1 continuous transfer write enable/ UARTC1 continuous transfer write enable	CSIF1 /UARTC1	CF1TIC /UC1TIC	–	–	√
		71	INTCF2R /INTUC0R	CSIF2 reception completion/CSIF2 reception error/ UARTC0 reception completion/UARTC0 reception error	CSIF2 /UARTC0	CF2RIC /UC0RIC	√	√	√
		72	INTCF2T /INTUC0T	CSIF2 continuous transfer write enable/UARTC0 continuous transfer write enable	CSIF2 /UARTC0	CF2TIC /UC0TIC	√	√	√
		73	INTCF3R	CSIF3 reception completion/CSIF3 reception error	CSIF3	CF3RIC	–	√	√
		74	INTCF3T	CSIF3 continuous transfer write enable	CSIF3	CF3TIC	–	√	√
		78	INTCF4R	CSIF4 reception completion/CSIF4 reception error	CSIF4	CF4RIC	–	√	√
		79	INTCF4T	CSIF4 continuous transfer write enable	CSIF4	CF4TIC	–	√	√
		87	INTUC2R /INTIIC2	UARTC2 reception completion/UARTC2 reception error/IIC2 transfer completion	UARTC2 /IIC2	UC2RIC /IICIC2	√	√	√
		88	INTUC2T	UARTC2 continuous transfer write enable	UARTC2	UC2TIC	√	√	√
		90	INTAD	A/D converter completion	A/D	ADIC	√	√	√

24. STANDBY FUNCTION

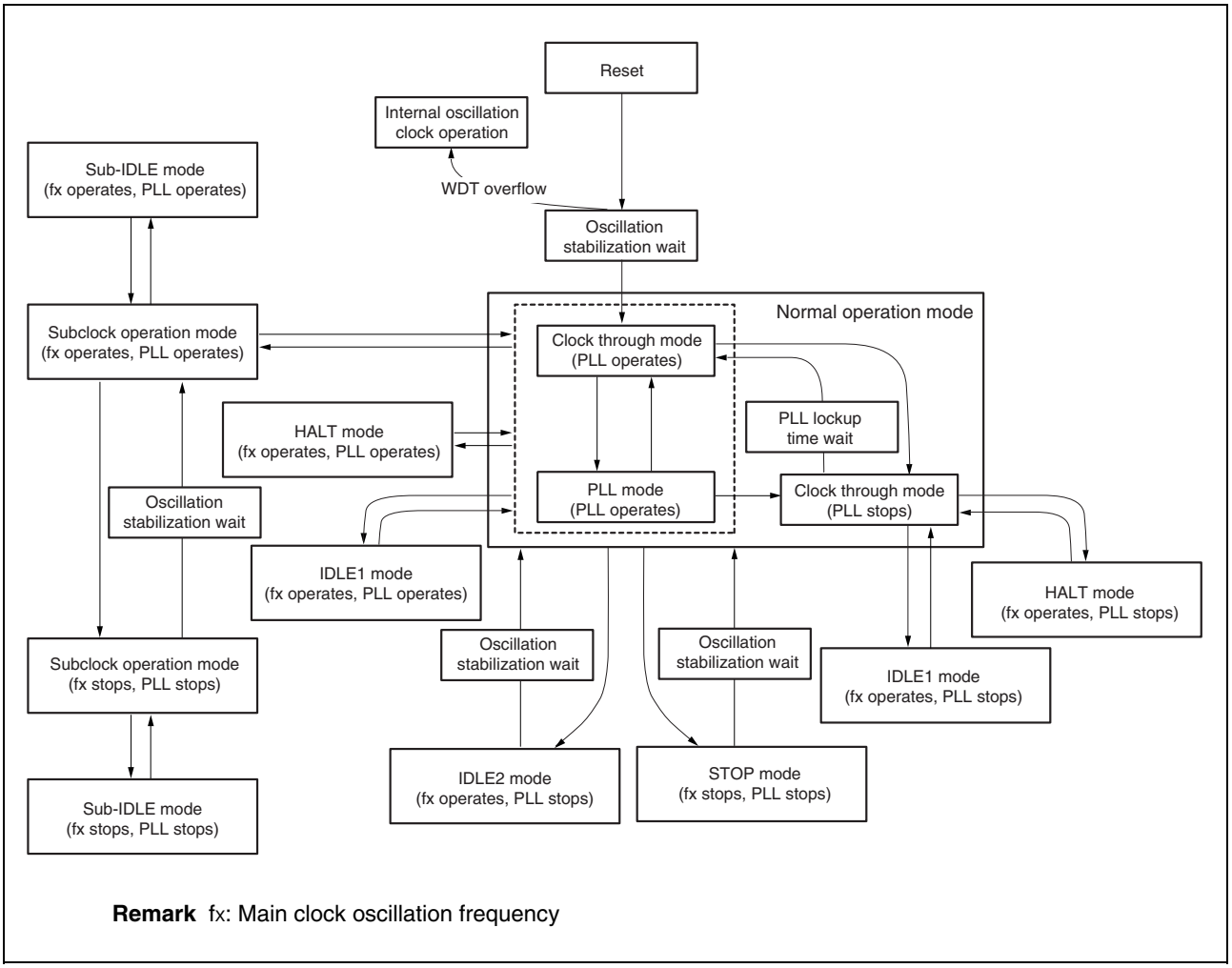
The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. The available standby modes are listed in Table 24-1.

Table 24-1. Standby Modes

Mode	Function Overview
HALT mode	Mode to stop only the operating clock of the CPU
IDLE1 mode	Mode to stop all the operations of the internal circuit except the oscillator, PLL operation[Note], and flash memory
IDLE2 mode	Mode to stop all the operations of the internal circuit except the oscillator
STOP mode	Mode to stop all the operations of the internal circuit except the subclock oscillator
Subclock operation mode	Mode to operate internal system clock by subclock
Sub-IDLE mode	Mode to stop all the operations of the internal circuit except the oscillator in subclock operation mode

Note PLL retains the previous operation status.

The following figure shows the status transitions of the standby function.



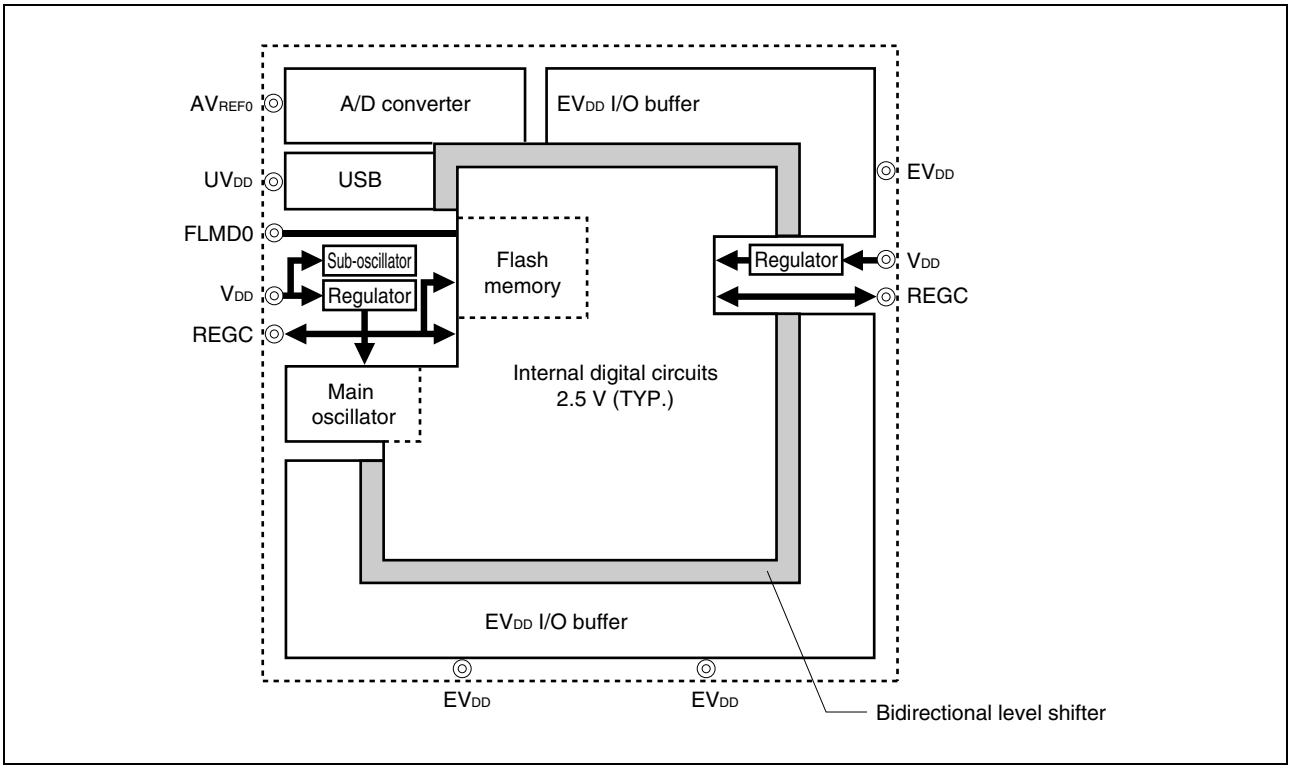
Remark fx: Main clock oscillation frequency

28. REGULATOR FUNCTION

The V850ES/Jx3-E includes a regulator to reduce power consumption and noise.

This regulator supplies a stepped-down V_{DD} power supply voltage to the oscillator block and internal logic circuits except the A/D converter and output buffers). The regulator output voltage is set to 2.5 V (TYP.).

The outline of the regulator functions is shown below.



29. FLASH MEMORY

Flash memory versions offer the following advantages for development environments and mass production applications.

- For altering software after the V850ES/Jx3-E is soldered onto the target system.
- For data adjustment when starting mass production.
- For differentiating software according to the specification in small scale production of various models.
- For facilitating inventory management.
- For updating software after shipment.

The flash memory in the V850ES/Jx3-E has the following features.

- 4-byte/1-clock access (when instruction is fetched)
- Memory size: 64/128/256 KB
- Rewrite voltage: Erase/write with a single power supply
- Rewriting method
  - Rewriting by communication with dedicated flash programmer via serial interface (on-board/off-board programming)
  - Rewriting flash memory by user program (self programming)
- Flash memory write prohibit function supported (security function)
- Safe rewriting of entire flash memory area by self programming using boot swap function
- Interrupts can be acknowledged during self programming.

Revision History	μPD70F3826, 70F3827, 70F3828, 70F3829, 70F3830, 70F3831, 70F3832, 70F3833, 70F3834, 70F3835, 70F3836, 70F3837 Data Sheet

Rev.	Date	Description	
		Page	Summary
0.01	Sep 30, 2010	–	First Eddition Issued

All documents should contain the following section break and paragraph as the last item. The footers of this document refer to the paragraph in order to reference the last page of the document.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.