Renesas Electronics America Inc - UPD70F3828GB(R)-GAH-AX Datasheet

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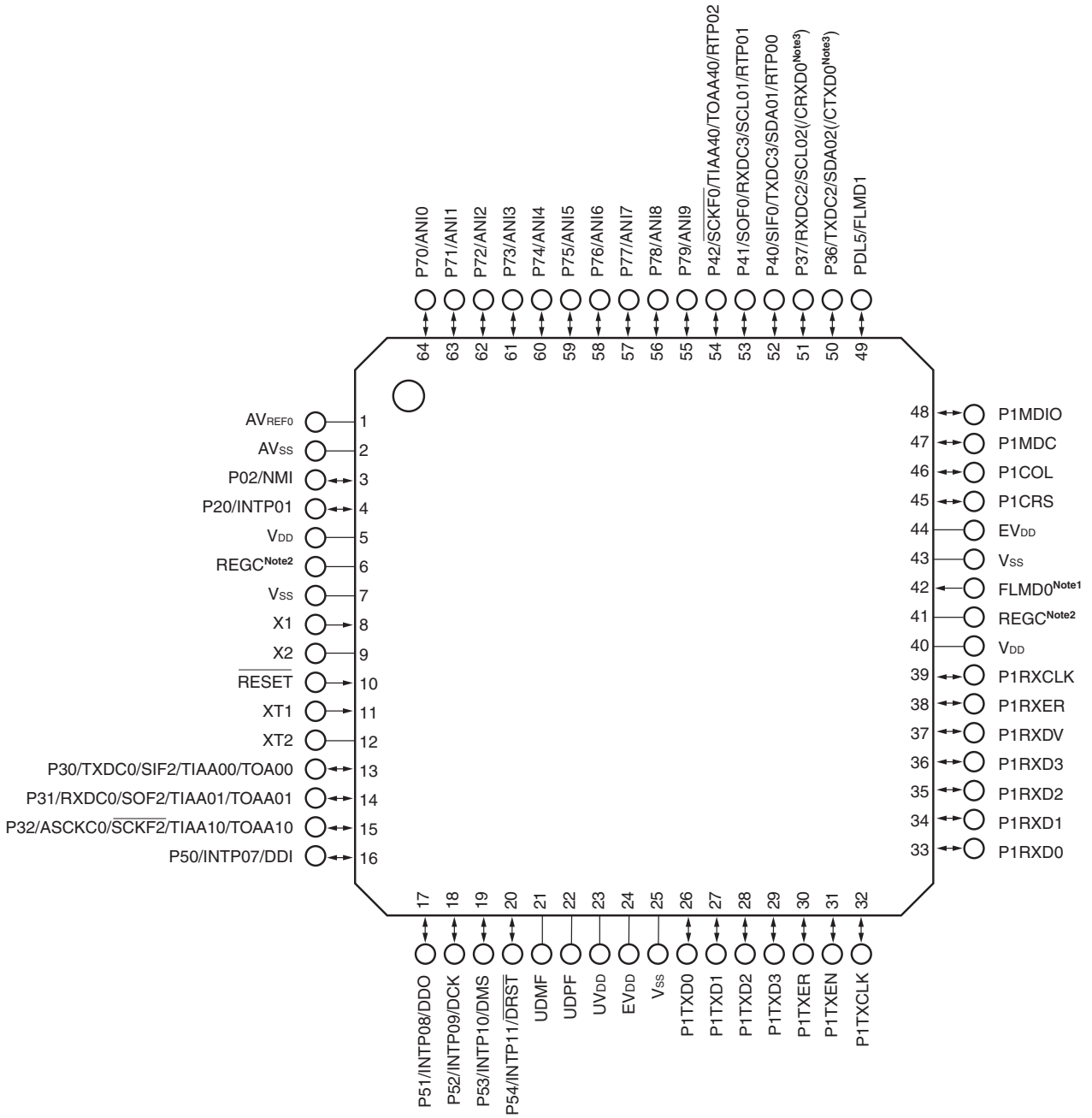
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, CSI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	26
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3828gb-r-gah-ax

PIN CONFIGURATION

- V850ES/JE3-E
  64-pin plastic LQFP (fine pitch) (10 × 10)
  μPD70F3826GB-GAH-AX μPD70F3827GB-GAH-AX
  μPD70F3828GB-GAH-AX μPD70F3829GB-GAH-AX



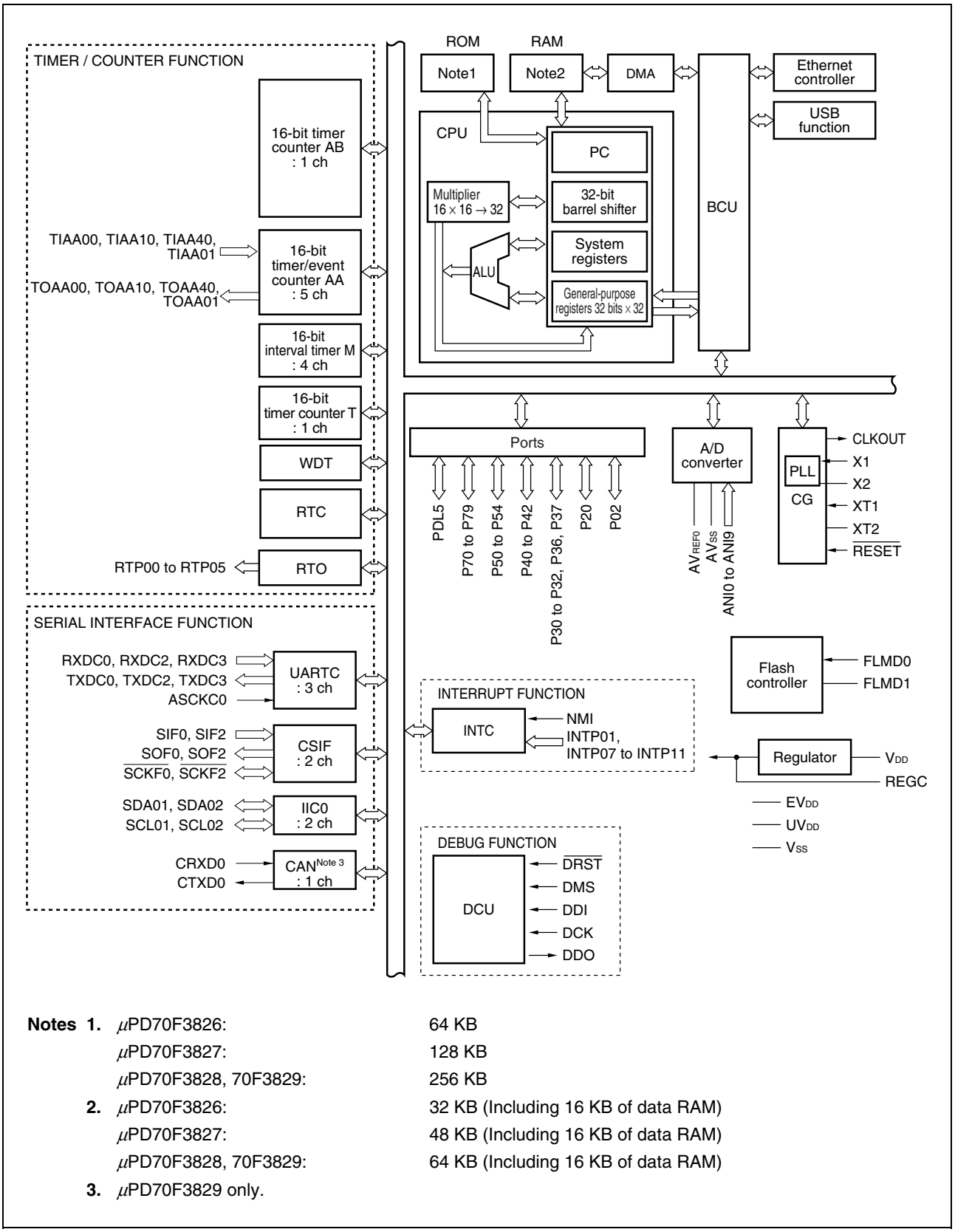
Notes 1. Connect to VSS in normal mode.

2. Connect the REGC pin to VSS via a 4.7 μF (preliminary value) capacitor.

3. μ PD70F3829 only.

INTERNAL BLOCK DIAGRAM

- **V850ES/JE3-E**

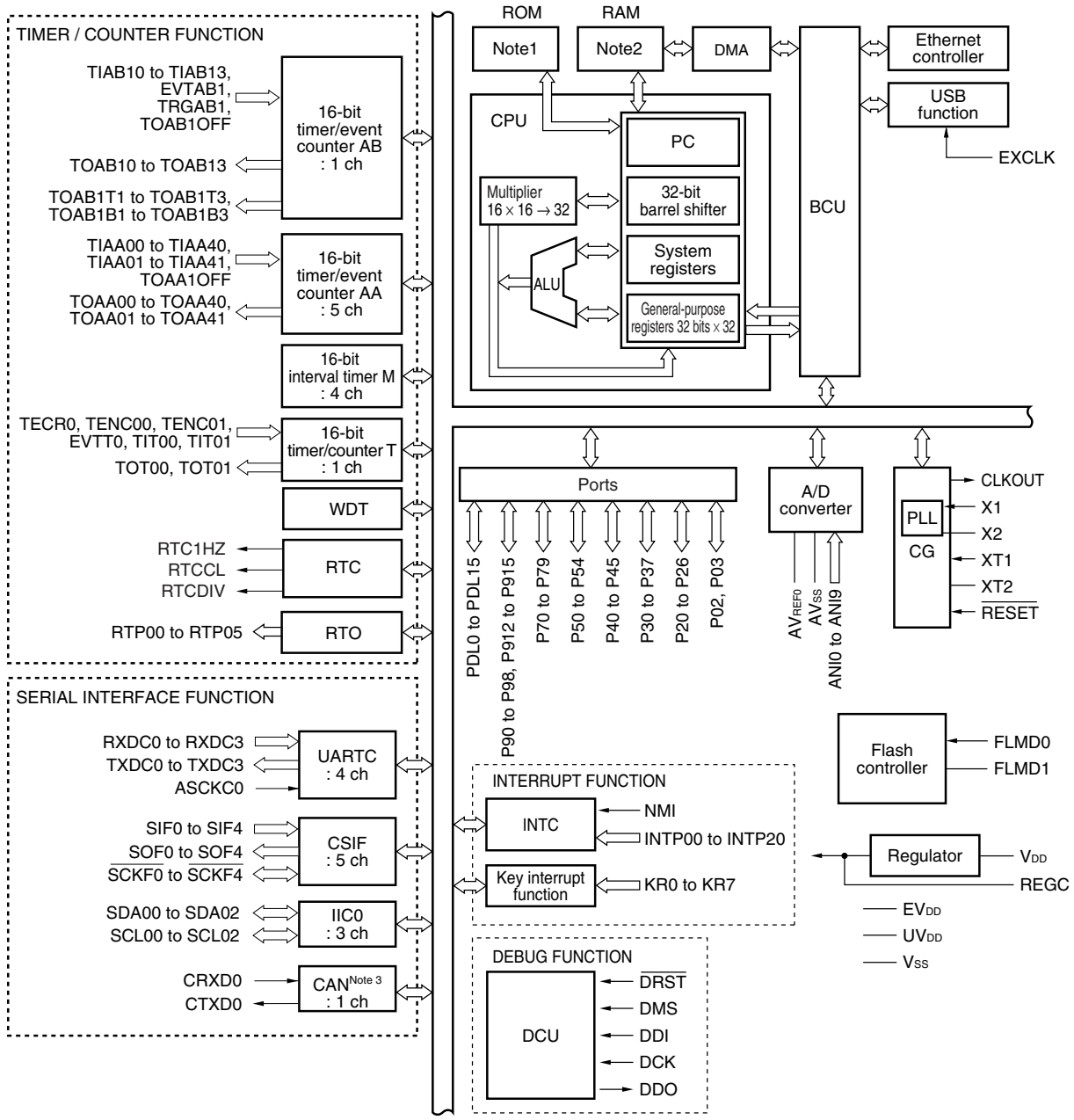


Notes 1. μPD70F3826: 64 KB
μPD70F3827: 128 KB
μPD70F3828, 70F3829: 256 KB

2. μPD70F3826: 32 KB (Including 16 KB of data RAM)
μPD70F3827: 48 KB (Including 16 KB of data RAM)
μPD70F3828, 70F3829: 64 KB (Including 16 KB of data RAM)

3. μPD70F3829 only.

- **V850ES/JG3-E**



Notes 1. μPD70F3834: 64 KB
μPD70F3835: 128 KB
μPD70F3836, 70F3837: 256 KB

2. μPD70F3834: 32 KB (Including 16 KB of data RAM)
μPD70F3835: 48 KB (Including 16 KB of data RAM)
μPD70F3836, 70F3837: 64 KB (Including 16 KB of data RAM)

3. μPD70F3837 only.

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
P70	I/O	Port 7 10-bit I/O port Input/output can be specified in 1-bit units.	ANI0	64	80	100
P71			ANI1	63	79	99
P72			ANI2	62	78	98
P73			ANI3	61	77	97
P74			ANI4	60	76	96
P75			ANI5	59	75	95
P76			ANI6	58	74	94
P77			ANI7	57	73	93
P78			ANI8	56	72	92
P79			ANI9	55	71	91
P90	I/O	Port 9 13-bit I/O port(V850ES/JG3-E) 11-bit I/O port(V850ES/JF3-E) Input/output can be specified in 1-bit units.	TOAB1T1/TOAB11/TIAB11/KR0/INTP12	–	57	72
P91			TOAB1B1/TIAB10/KR1/TOAB10	–	58	73
P92			TOAB1T2/TOAB12/TIAB12/KR2/INTP13	–	59	74
P93			TOAB1B2/TRGAB1/KR3/INTP14	–	60	75
P94			TOAB1T3/TOAB13/TIAB13/KR4/INTP15	–	61	76
P95			TOAB1B3/EVTB1/KR5/INTP16	–	62	77
P96			TECR0/TIT00/KR6/TOT00	–	31	40
P97			TENC00/TIT01/KR7/TOT01	–	32	41
P98			TENC01/INTP17	–	33	42
P912			TOAB1OFF/INTP18	–	63	78
P913			SIF31/INTP19	–	–	30
			INTP19	–	25	–
P914			SOF3/INTP20	–	–	31
P915			$\overline{\text{SCKF3}}$	–	–	32
PDL0	I/O	Port DL 11-bit I/O port(V850ES/JG3-E) 1-bit I/O port(V850ES/JF3-E, V850ES/JE3-E) Input/output can be specified in 1-bit units.	–	–	–	58
PDL1			–	–	–	59
PDL2			–	–	–	60
PDL3			–	–	–	66
PDL4			–	–	–	67
PDL5			FLMD1	49	64	79
PDL6			–	–	–	83
PDL7			–	–	–	84
PDL8			–	–	–	33
PDL9			–	–	–	34
PDL10			–	–	–	43

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
INTP11	Input	External interrupt request input (maskable, analog noise elimination).	P54/$\overline{\text{DRST}}$	20	24	29
INTP12			P90/TOAB1T1/TOAB11/TIAB11/KR0	–	57	72
INTP13			P92/TOAB1T2/TOAB12/TIAB12/KR2	–	59	74
INTP14			P93/TOAB1B2/TRGAB1/KR3	–	60	75
INTP15			P94/TOAB1T3/TOAB13/TIAB13/KR4	–	61	76
INTP16			P95/TOAB1B3/EVTAB1/KR5	–	62	77
INTP17			P98/TENC01	–	33	42
INTP18			P912/TOAB1OFF	–	63	78
INTP19			P913/SIF3	–	–	30
			P913	–	25	–
INTP20			P914/SOF3	–	–	31
KR0	Input	Key interrupt input (analog noise elimination)	P90/TOAB1T1/TOAB11/TIAB11/INTP12	–	57	72
KR1			P91/TOAB1B1/TIAB10/TOAB10	–	58	73
KR2			P92/TOAB1T2/TOAB12/TIAB12/INTP13	–	59	74
KR3			P93/TOAB1B2/TRGAB1/INTP14	–	60	75
KR4			P94/TOAB1T3/TOAB13/TIAB13/INTP15	–	61	76
KR5			P95/TOAB1B3/EVTAB1/INTP16	–	62	77
KR6			P96/TECR0/TIT00/TOT00	–	31	40
KR7			P97/TENC00/TIT01/TOT01	–	32	41
NMI	Input	External interrupt (non-maskable, ananlog noise elimination)	P02	3	3	3
P1COL	Input	Collision detection input for Ethernet	–	46	54	69
P1CRS	Input	Carrier detection input for Ethernet	–	45	53	68
P1MDC	Output	Seria transmit clock output	–	32	40	50
P1MDIO	I/O	Serial I/O	–	47	55	70
P1RXCLK	Input	Receive clock input for Ethernet	–	48	56	71
P1RXD0	Input	Receive data input for Ethernet	–	39	47	57
P1RXD1	Input	Receive data input for Ethernet	–	33	41	51
P1RXD2	Input	Receive data input for Ethernet	–	34	42	52
P1RXD3	Input	Receive data input for Ethernet	–	35	43	53
P1RXDV	Input	Receive data VALID input for Ethernet	–	36	44	54
P1RXER	Input	Receive data error input for Ethernet	–	37	45	55
P1TXCLK	Output	Transmit clock output for Ethernet	–	38	46	56
P1TXD0	Output	Transmit data output for Ethernet	–	26	34	44
P1TXD1	Output	Transmit data output for Ethernet	–	27	35	45
P1TXD2	Output	Transmit data output for Ethernet	–	28	36	46
P1TXD3	Output	Transmit data output for Ethernet	–	29	37	47
P1TXEN	Output	Transmit data enable output for Ethernet	–	31	39	49
P1TXER	Output	Transmit error output for Ethernet	–	30	38	48

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
REGC	–	Connecting capacitor for regulator output stabilization (4.7 μF (preliminary value))	–	6, 41	6, 49	9, 62
$\overline{\text{RESET}}$	Input	System reset input	–	10	10	13
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	P22/INTP02	–	–	7
RTCCL	Output	Real-time counter clock (original 32 kHz clock) output	P21/RTCDIV	–	–	6
RTCDIV	Output	Real-time counter clock (divided 32 kHz clock) output	P21/RTCCL	–	–	6
RTP00	Output	Real-time output port	P40/SIF0/TXDC3/SDA01	52	68	85
RTP01		RTP00, RTP01 are N-ch open-drain output selectable.	P41/SOF0/RXDC3/SCL01	53	69	86
RTP02			P42/$\overline{\text{SCKF0}}$/TIAA40/TOAA40	54	70	87
RTP03			P43	–	–	88
RTP04			P44	–	–	89
RTP05			P45TIAA41/TOAA41	–	–	90
RXDC0	Input	Serial receive data input (UARTC0 to UARTC3)	P31/SOF2/TIAA01/TOAA01	14	18	21
RXDC1			P24/SOF1/SDL00/INTP04	–	14	17
RXDC2			P37/SCL02/CRXD0[Note]	51	67	82
RXDC3			P41/SOF0/SCL01/RTP01	53	69	86
$\overline{\text{SCKF0}}$	I/O	Serial clock I/O (CSIF0 to CSIF4)	P42/TIAA40/TOAA40/RTP02	54	70	87
$\overline{\text{SCKF1}}$			P25/TIAA30/TOAA30	–	15	18
$\overline{\text{SCKF2}}$			P32/ASCKC0/TIAA10/TOAA10	15	19	22
$\overline{\text{SCKF3}}$			P915	–	–	32
$\overline{\text{SCKF4}}$			P35/TIAA21/TOAA21/TOAA1OFF /INTP06	–	–	80
SCL00	I/O	Serial clock I/O (I^2C00 to I^2C02)	P24/SOF1/RXDC1/INTP04	–	14	17
SCL01		N-ch open-drain output selectable.	P41/SOF0/RXDC3/RTP01	53	69	86
SCL02			P37/RXDC2/CRXD0[Note]	51	67	82
SDA00	I/O	Serial transmit/receive data I/O (I^2C00 to I^2C02)	P23/SIF1/TXDC1/INTP03	–	13	16
SDA01		N-ch open-drain output selectable.	P40/SIF0/TXDC3/RTP00	52	68	85
SDA02			P36/TXDC2/CTXD0[Note]	50	66	81
SIF0	Input	Serial receive data input (CSIF0 to CSIF4)	P40/TXDC3/SDA01/RTP00	52	68	85
SIF1			P23/TXDC1/SDA00/INTP03	–	13	16
SIF2			P30/TXDC0/TIAA00/TOAA00	13	17	20
SIF3			P913/INTP19	–	–	30
SIF4			P33/TIAA11/TOAA11	–	–	23
SOF0	Output	Serial transmit data output (CSIF0 to CSIF4)	P41/RXDC3/SCL01/RTP01	53	69	86
SOF1		N-ch open-drain output selectable.	P24/RXDC1/SDL00/INTP04	–	14	17
SOF2			P31/RXDC0/TIAA01/TOAA01	14	18	21
SOF3			P914/INTP20	–	–	31
SOF4			P34/TIAA20/TOAA20	–	–	24
TECR0	Input	Encoder clear input of TMT0	P96/TIT00/KR6/TOT00	–	31	40
TENC00		Encoder input/external event input/external trigger input of TMT0	P97/TIT01/KR7/TOT01	–	32	41
TENC01		Encoder input of TMT0	P98/INTP17	–	33	42

Note Available only in on-chip CAN controller products

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

1.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 1-1. For the schematic circuit diagram of each type, refer to **Figure 1-1**.

Table 1-1. Types of Pin I/O Circuits (1/3)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JE3-E	JF3-E	JG3-E
P02	NMI	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	3	3	3
P03	INTP00/ADTRG/EXCLK			–	–	4
P20	TOAB02/INTP01	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	4	4	5
P21	RTCDIV/RTCCL			–	–	6
P22	RTC1HZ/INTP02			–	–	7
P23	SIF1/TXDC1/SDA00/INTP03			–	13	16
P24	SOF1/RXDC1/SCL00/INTP04			–	14	17
P25	$\overline{\text{SCKF1}}$/TIAA30/TOAA30			–	15	18
P26	TIAA31/TOAA31/INTP05			–	16	19
P27	TIAB03/TOAB03/INTP21			4	4	5
P30	TXDC0/SIF2/TIAA00/TOAA00	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	13	17	20
P31	RXDC0/SOF2/TIAA01/TOAA01			14	18	21
P32	ASCKC0/$\overline{\text{SCKF2}}$/TIAA10/TOAA10			15	19	22
P33	SIF4/TIAA11/TOAA11			–	–	23
P34	SOF4/TIAA20/TOAA20			–	–	24
P35	$\overline{\text{SCKF4}}$/TIAA21/TOAA21/TOAA1OFF/INTP06			–	–	80
	TIAA21/TOAA21/TOAA1OFF/INTP06			–	65	–
P36	TXDC2/SDA02/CTXD0[Note]			50	66	81
P37	RXDC2/SCL02/CRXD0[Note]			51	67	82
P40	SIF0/TXDC3/SDA01/RTP00	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	52	68	85
P41	SOF0/RXDC3/SCL01/RTP01			53	69	86
P42	$\overline{\text{SCKF0}}$/TIAA40/TOAA40/RTP02			54	70	87
P43	RTP03			–	–	88
P44	RTP04			–	–	89
P45	TIAA41/TOAA41/RTP05			–	–	90
P50	INTP07/DDI	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	16	20	25
P51	INTP08/DDO			17	21	26
P52	INTP09/DCK			18	22	27
P53	INTP10/DMS			19	23	28
P54	INTP11/$\overline{\text{DRST}}$	10-N	Input: Independently connect to V_{SS} via a resistor. Fixing to V_{DD} level is prohibited. Output: Leave open. Internally pull-down after reset by $\overline{\text{RESET}}$ pin.	20	24	29
P70 to P79	ANI0 to ANI9	11-G	Input: Independently connect to AV_{REF0} or AV_{SS} via a resistor. Output: Leave open.	64 to 55	80 to 71	100 to 91

Note Available only in on-chip CAN controller products.

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

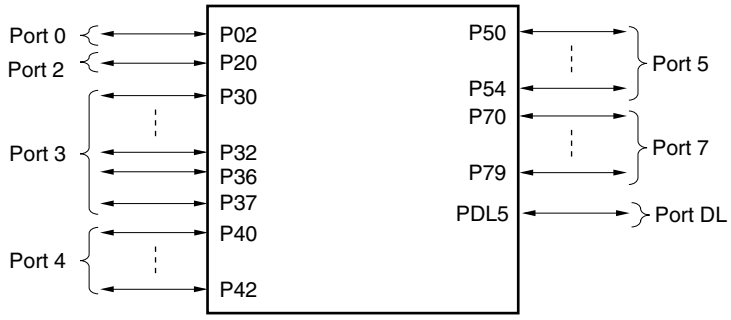
4. PORTS

The number of I/O ports of the V850ES/Jx3-E is shown below.

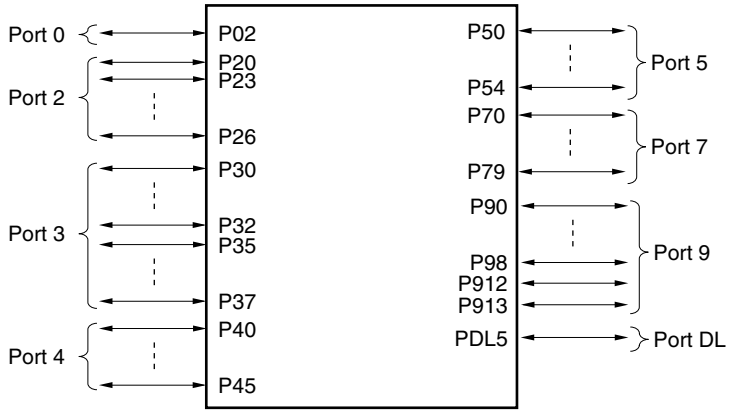
Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of ports (5 V tolerant)	26 (12)	42 (28)	62 (35)

The following figure shows the basic configurations of ports.

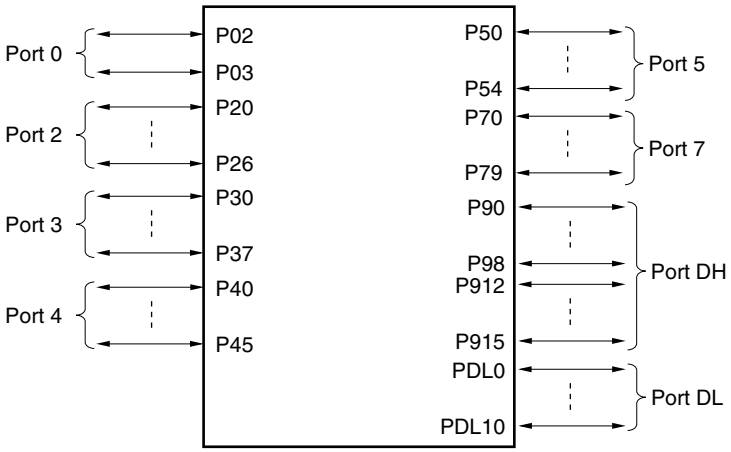
(a) V850ES/JE3-E



(b) V850ES/JF3-E



(c) V850ES/JG3-E



5. CLOCK GENERATION FUNCTION

The clock generation function has the following features.

- Main clock oscillator
  - PLL mode (×8): f_X = 3 to 6.25 MHz (f_{XX} = 24 to 50 MHz)
  - Clock through mode: f_X = 3 to 6.25 MHz (f_{XX} = 3 to 6.25 MHz)
- Subclock oscillator
  - f_{XT} = 32.768 kHz
- Internal oscillator (f_R = 220 kHz)
  - Default clock of watchdog timer
  - Sampling clock for clock monitor function of the main clock oscillator
  - Can be used as the internal system clock after the main clock is stopped
- Internal system clock generation
  - 7 levels (f_{XX}, f_{XX}/2, f_{XX}/4, f_{XX}/8, f_{XX}/16, f_{XX}/32, f_{XT})
- Peripheral clock generation
- Clock output function

8. 16-BIT TIMER/EVENT COUNTER T (TMT)

The number of TAB of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	1 channel (TMT0[Note])	1 channel (TMT0)	1 channel (TMT0)
Number of timer output	-	2	2

Note Interval timer function only.

The TMT function has the following features.

- 16 bit timer/counter (TMT)
- Clock selection: 8 ways
- Capture/trigger input pins (TIT00, TIT01) : 2
- External event count input pin[Note 1] : 1
- Encoder input pin (TENC00, TENC01) : 2
- Encoder clear input pin (TECR0) : 1
- External trigger input pin[Note 1]: 1
- Timer/counter: 1
- Capture/compare registers: 2
- Capture/compare match interrupt request signals: 2
- Timer output pins (TOT00, TOT01) : 2

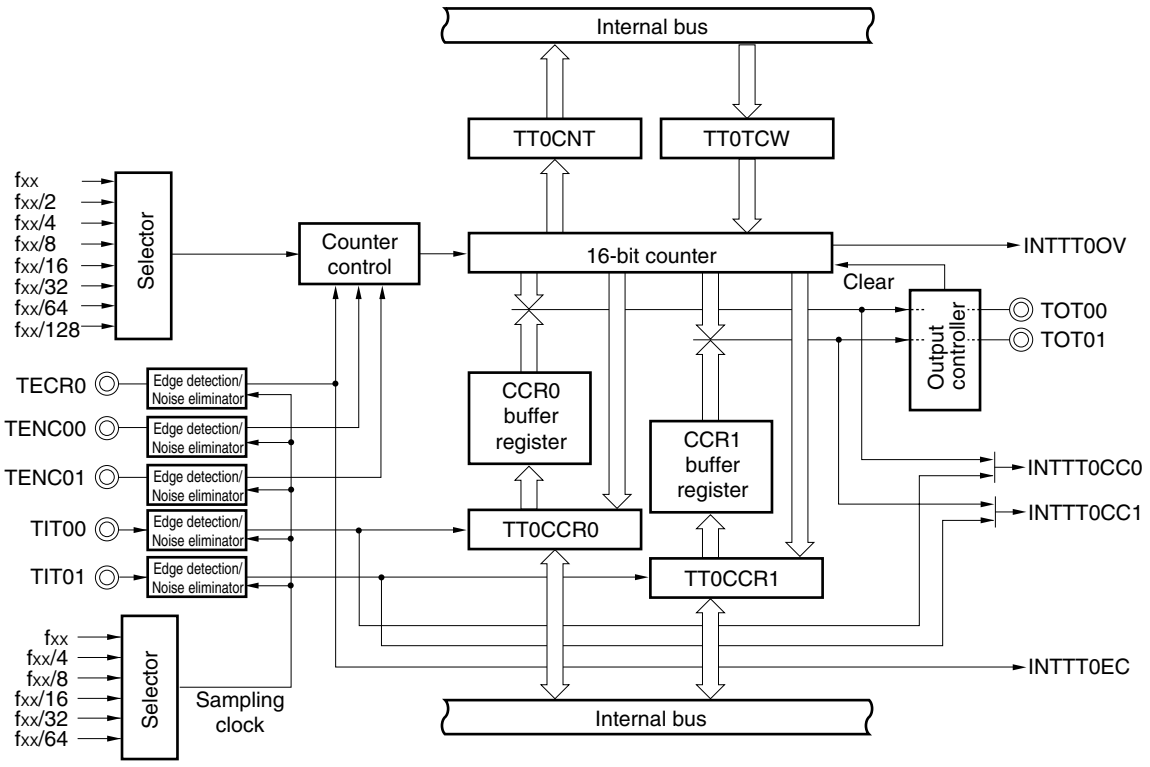
The TMT function has the following features[Note 2].

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Triangular wave PWM output
- Encoder count function

Notes1. The external trigger input pin and the external event count input pin also function as the encoder input pin (TENC00)

2. The TMT0 function of V850ES/JE3-E is only Interval timer.

The following figure shows the configuration of TMT.



Remark fxx: Main clock frequency

11. REAL-TIME COUNTER

In the V850ES/Jx3-E, one channel of real-time counter is provided.

The real-time counter has the following features.

- It has counters for year, month, week, day, hours, minutes and seconds, and it can count up to 99 years.
- The year, month, week, day, hour, minute and second counters show the count in BCD code[Note 1].
- Alarm interrupt function
- Fixed-cycle interrupt function (cycle: 1 month to 0.5 seconds)
- Interval interrupt function (cycle: 1.95 to 125 ms)
- 1 Hz pin output
- 32.768 kHz pin output
- 512 Hz or 16.384 kHz pin output
- Watch error correction function
- Subclock operation or main clock operation[Note 2] selectable

Notes 1. BCD (binary-coded decimal) code is the code that represents each digit of a decimal number in 4-bit binary numerals.

2. The main clock can be divided into 32.768 kHz f_{BRG} with the baud rate generator dedicated to the real-time counter.

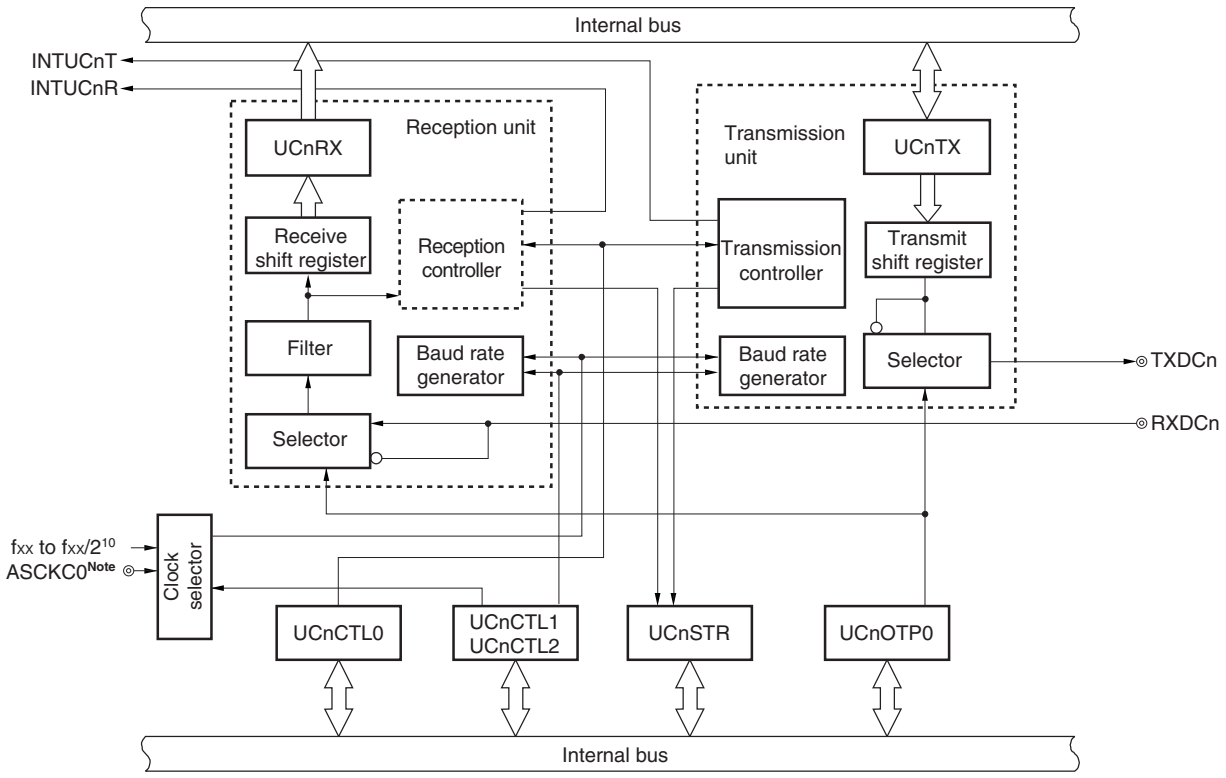
14. A/D CONVERTER

An A/D converter unit with ten channels is provided in the V850ES/Jx3-E.

The A/D converter has the following features.

- 10-bit resolution
- 10 channels
- Successive approximation method
- Operating voltage: AV_{REF0} = 3.0 to 3.6 V
- Analog input voltage: 0 V to AV_{REF0}
- The following functions are provided as operation modes.
  - Continuous select mode
  - Continuous scan mode
  - One-shot select mode
  - One-shot scan mode
- The following functions are provided as trigger modes.
  - Software trigger mode
  - External trigger mode (external, 1)
  - Timer trigger mode
- Power-fail monitor function (conversion result compare function)

The following figure shows the configuration of UARTC.



Note UARTC0 only

Remark fxx : Main clock frequency

16. CLOCKED SERIAL INTERFACE F (CSIF)

The number of CSIF of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	2 channels (CSIF0 and CSIF2)	3 channels (CSIF0 to CSIF2)	5 channels (CSIF0 to CSIF4)

- Transfer rate: 8 Mbps max. (f_{XX} = 50 MHz, using internal clock)
- Master mode and slave mode selectable
- 8-bit to 16-bit transfer, 3-wire serial interface
- Interrupt request signals (INTCFnT, INTCFnR)
- Serial clock and data phase switchable
- Transfer data length selectable in 1-bit units between 8 and 16 bits
- Transfer data MSB-first/LSB-first switchable
- 3-wire SOFn: Serial data output
  SIFn: Serial data input
  $\overline{\text{SCKFn}}$: Serial clock I/O

  Transmission mode, reception mode, and transmission/reception mode specifiable

17. I²C BUS

The number of I²C bus of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	2 channels (I²C01 and I²C02)	3 channels (I²C00 to I²C02)	3 channels (I²C00 to I²C02)

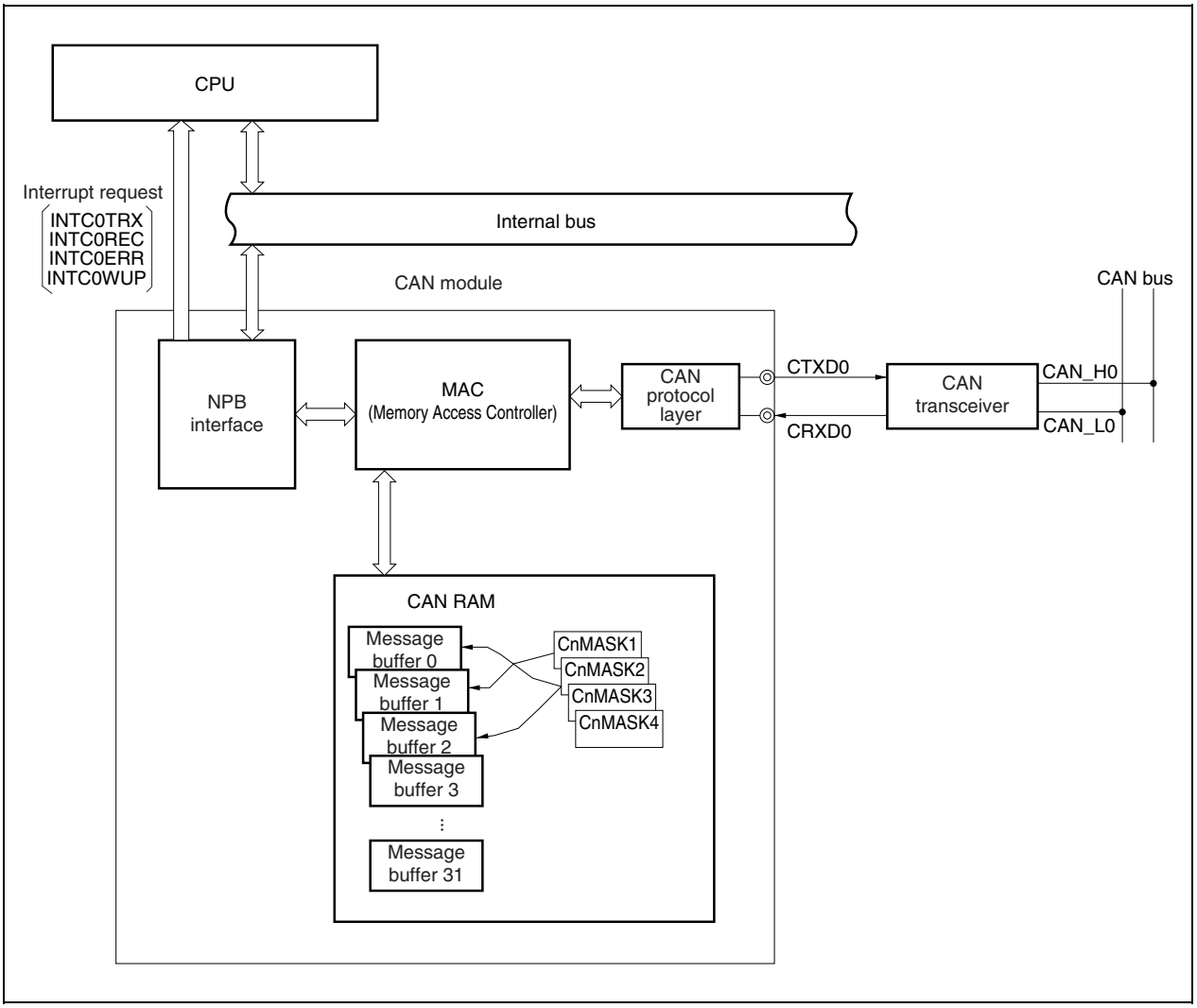
- Transfer rate: Standard mode (100 kbps max.)/high-speed mode (400 kbps max.)
- Conforms to I²C bus format (multimaster supported)
- 2-wire SCL0n: Serial clock pin
  SDA0n: Serial data bus pin

18. CAN CONTROLLER

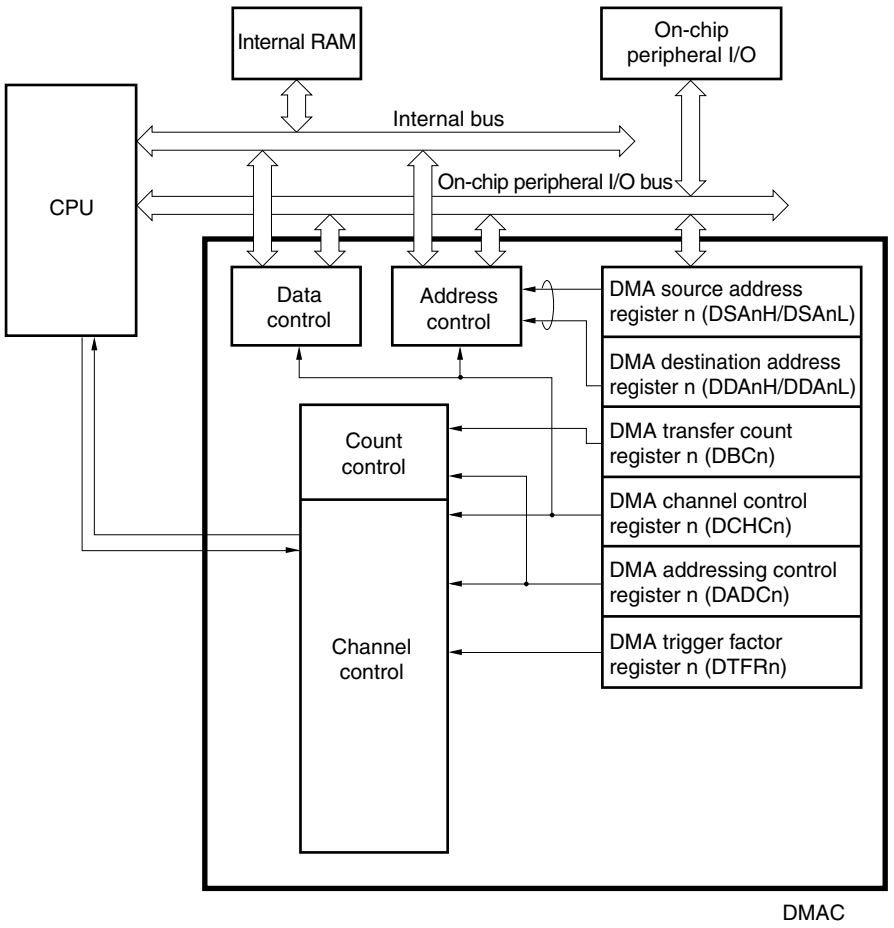
In the μPD70F3829, 70F3833, 70F3837, one channel of CAN controller is provided.

- Compliant with ISO 11898 and tested according to ISO/DIS 16845 (CAN conformance test)
- Standard frame and extended frame transmission/reception enabled
- Transfer rate: 1 Mbps max. (CAN clock input ≥ 8 MHz)
- 32 message buffers/channels
- Receive/transmit history list function
- Automatic block transmission function
- Multi-buffer receive block function
- Mask setting of four patterns is possible for each channel

The following figure shows the configuration of CAN controller.



The following figure shows the configuration of DMA controller.



Remark n = 0 to 3

26. CLOCK MONITOR, LOW-VOLTAGE DETECTOR

(1) Clock monitor

The clock monitor samples the main clock by using the internal oscillation clock (f_R) and generates a reset request signal when oscillation of the main clock is stopped.

(2) Low-voltage detector

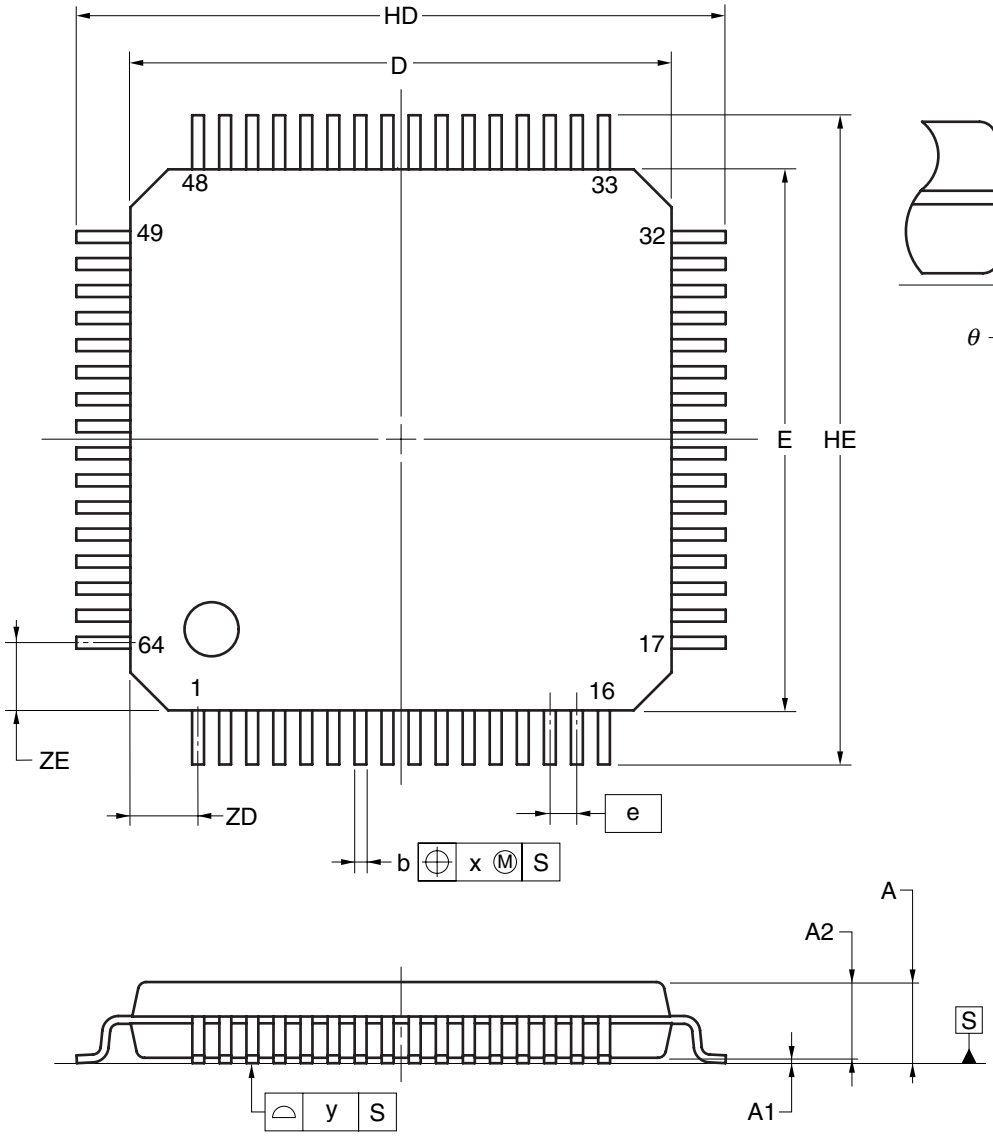
The low-voltage detector (LVI) has the following functions.

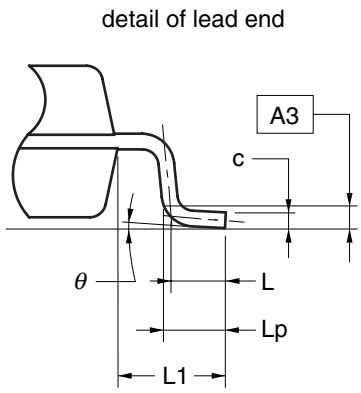
- Compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}) and generates an interrupt request signal or internal reset signal when $V_{DD} < V_{LVI}$.
- An interrupt request signal or internal reset signal can be selected.
- Can operate in STOP mode.
- Operation can be stopped by software.

31. PACKAGE DRAWINGS

- V850ES/JE3-E

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)





(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P64GB-50-GAH

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.