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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, CSI, Ethernet, I ² C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	26
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3829gb-r-gah-ax

- V850ES/JE3-E

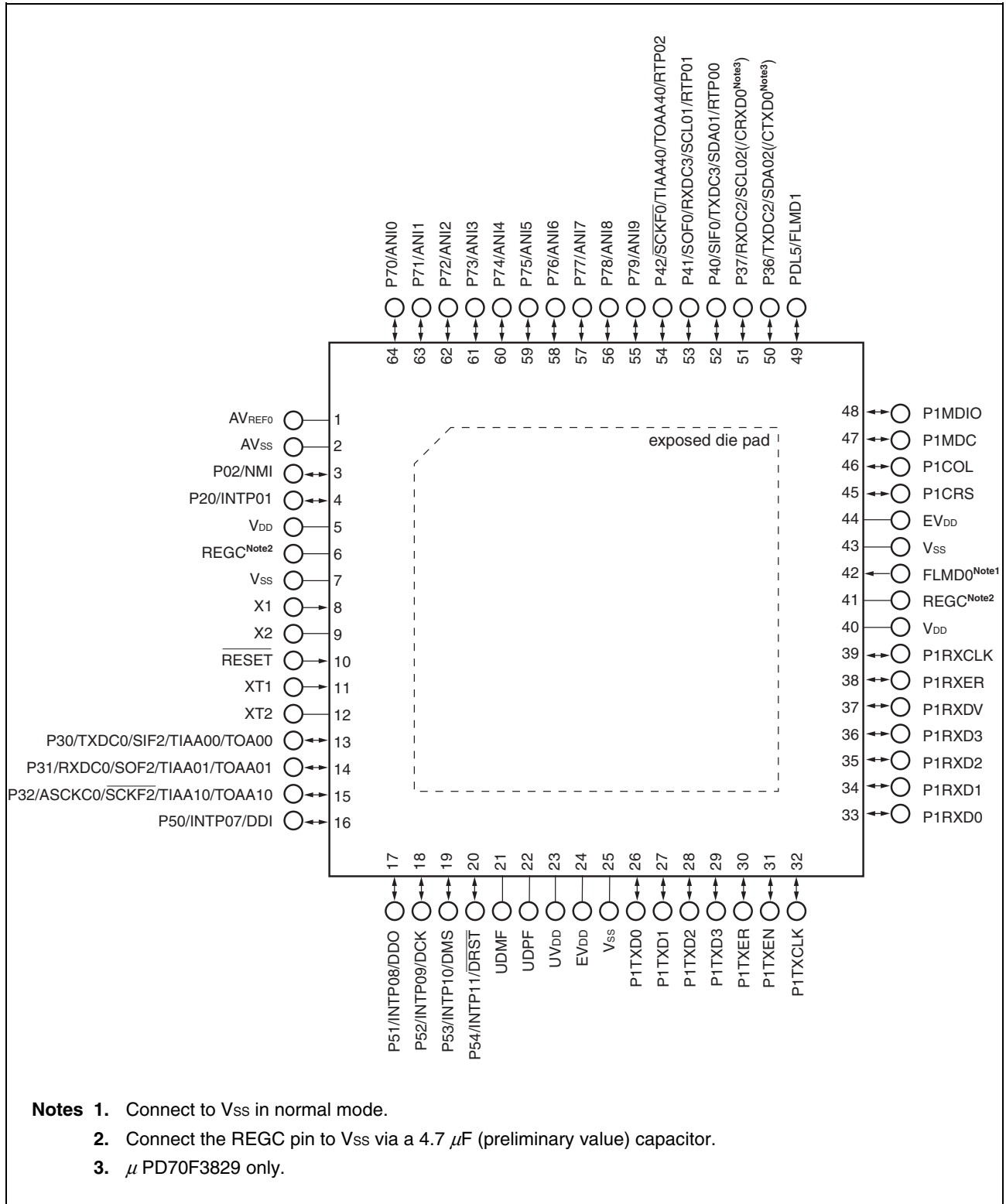
64-pin plastic WQFN (9 × 9)

μPD70F3826K8-6B4-AX

μPD70F3827K8-6B4-AX

μPD70F3828 K8-6B4-AX

μPD70F3829K8-6B4-AX

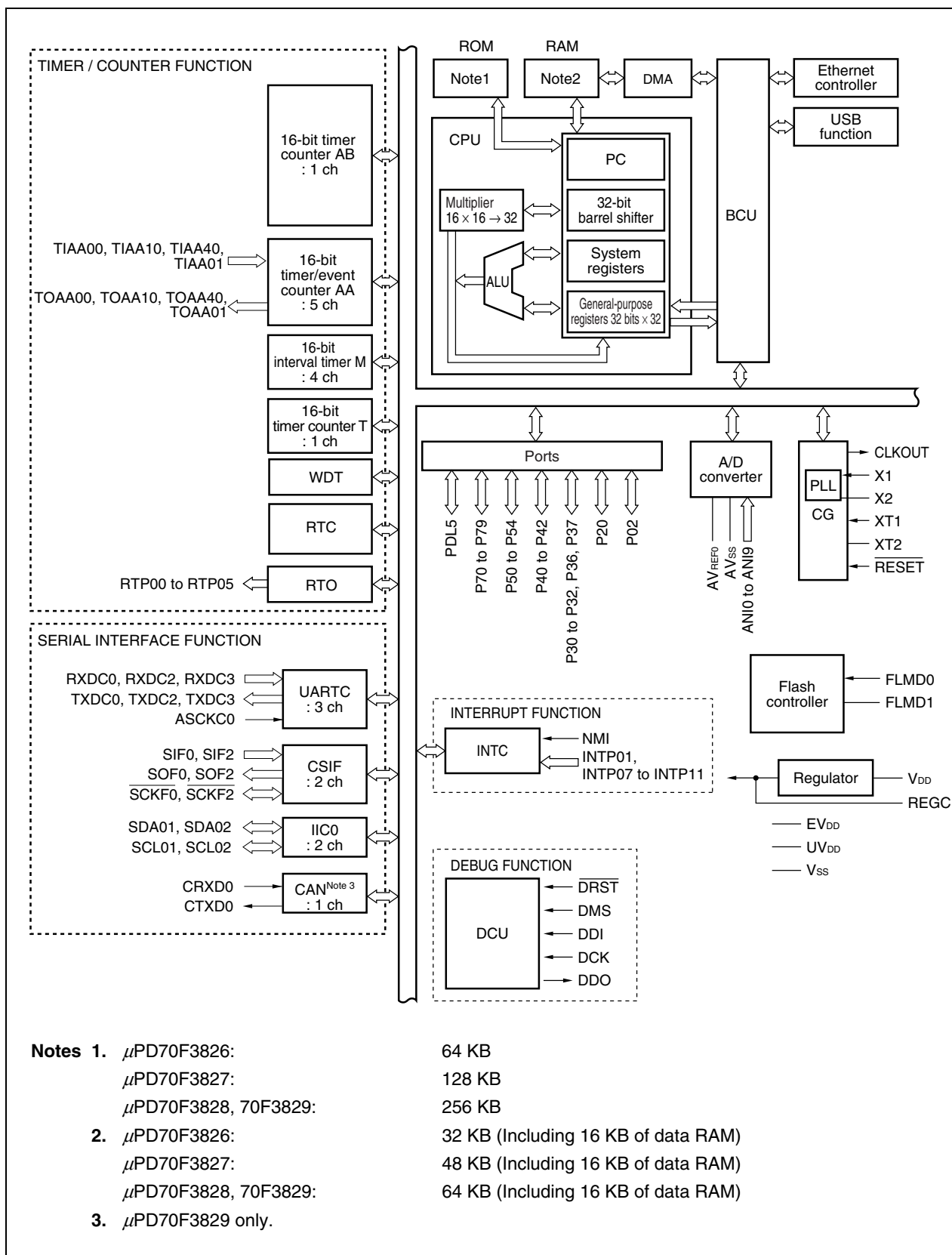


PIN IDENTIFICATION

ADTRG:	A/D Trigger Input	RXDC0 to RXDC3	Receive Data
ANI0 to ANI9:	Analog Input	$\overline{\text{SCKF0}}$ to $\overline{\text{SCKF4}}$:	Serial Clock
ASCKC0:	Asynchronous Serial Clock	SCL00 to SCL02:	Serial Clock
AV _{REF0} :	Analog Reference Voltage	SDA00 to SDA02:	Serial Data
AV _{SS} :	Grand for Analog Pin	SIF0 to SIF4:	Serial Input
CRXD0:	CAN Receive Data	SOF0 to SOF4:	Serial Output
CTXD0:	CAN Transmit Data	TECR0:	Timer Encoder Clear Input
DCK:	Debug Clock	TENC00, TENC01:	Timer Encoder Input
DDI:	Debug Data Input	TIAA00, TIAA01,	Timer Input
DDO:	Debug Data Output	TIAA10, TIAA11,	
DMS:	Debug Mode Select	TIAA20, TIAA21,	
$\overline{\text{DRST}}$:	Debug Reset	TIAA30, TIAA31,	
EV _{DD} :	Power Supply for External Pin	TIAA40, TIAA41,	
EVTAB1:	Timer Event Count Input	TIAB10 to TIAB13,	
EXCLK	USB clock	TIT00, TIT01:	
FLMD0, FLMD1:	Flash Programming Mode	TOAA00, TOAA01,	Timer Output
INTP00 to INTP20:	External Interrupt Input	TOAA10, TOAA11,	
KR0 to KR7:	Key Return	TOAA20, TOAA21,	
NMI:	Non-maskable Interrupt Request	TOAA30, TOAA31,	
P02, P03:	Port0	TOAA40, TOAA41,	
P1COL, P1CRS,	Ethernet PHY Interface	TOAB10 to TOAB13,	
P1MDC, P1MDIO,		TOAB1B1 to TOAB1B3,	
P1RXCLK,		TOAB1T1 to TOAB1T3,	
P1RXD0 to P1RXD3,		TOT00, TOT01:	
P1RXDV, P1RXER		TOAA1OFF,	Timer Output Off
P1TXCLK,		TOAB1OFF	
P1TXD0 to P1TXD3,		TRGAB1:	Timer Trigger Input
P1TXEN, P1TXER:		TXDC0 to TXDC3:	Serial Output
P20 to P26	Port2	UDMF:	USB Data I/O (-) Function
P30 to P37:	Port3	UDPF:	USB Data I/O (+) Function
P40 to P45:	Port4	UV _{DD} :	Power Supply for External USB
P50 to P54:	Port5	V _{DD} :	Power Supply
P70 to P79:	Port7	V _{SS} :	Ground
P90 to P98,	Port9	X1, X2:	Crystal for Main Clock
P912 to P915:		XT1, XT2:	Crystal for Sub-clock
PDL0 to PDL10:	Port DL		
REGC:	Regulator Control		
$\overline{\text{RESET}}$:	Reset		
RTC1HZ, RTCCL,	Real-time Counter Clock Output		
RTCDIV:			
RTP00 to RTP05:	Real-time Output Port		

INTERNAL BLOCK DIAGRAM

• V850ES/JE3-E



1.2 Non-Port Pins

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
ADTRG	Input	External trigger input for A/D converter	P03/INTP00/EXCLK	–	–	4
ANI0	Input	Analog voltage input for A/D converter	P70	64	80	100
ANI1			P71	63	79	99
ANI2			P72	62	78	98
ANI3			P73	61	77	97
ANI4			P74	60	76	96
ANI5			P75	59	75	95
ANI6			P76	58	74	94
ANI7			P77	57	73	93
ANI8			P78	56	72	92
ANI9			P79	55	71	91
ASCKC0	Input	UARTC0 baud rate clock input	P32/SCKF2/TIAA10/TOAA10	15	19	22
AVREF0	–	Reference voltage input for A/D converter, and positive power supply for port 7	–	1	1	1
AVSS	–	Ground voltage for A/D converter	–	2	2	2
CRXD0 ^{Note}	Input	CAN receive data input	P37/RXDC2/SCL02	51	67	82
CTXD0 ^{Note}	Output	CAN transmit data output	P36/TXDC2/SDA02	50	66	81
DCK	Input	Clock input for on-chip debugging	P52/INTP09	18	22	27
DDI	Input	Data input for on-chip debugging	P50/INTP07	16	20	25
DDO	Output	Data output for on-chip debugging In the on-chip debug mode, high-level output is forcibly set.	P51/INTP08	17	21	26
DMS	Input	Mode select signal input for on-chip debugging	P53/INTP10	19	23	28
DRST	Input	Reset signal input for on-chip debugging	P54/INTP11	20	24	29
EVDD	–	Positive power supply for external (same potential as VDD)	–	24, 44	29, 52	38, 65
EVTAB1	Input	External event count input of TAB1	P95/TOAB1B3/KR5/INTP16	–	62	77
EXCLK	Input	USB clock signal input	P03/INTP00/ADTRG	–	–	4
FLMD0	Input	Flash programming mode setting pins	–	42	50	63
FLMD1	Input		PDL5/AD5	49	64	79
INTP00	Input	External interrupt request input (maskable, analog noise elimination). Analog noise elimination or digital noise elimination selectable for INTP02 pin.	P03/ADTRG/EXCLK	–	–	4
INTP01			P20	4	4	5
INTP02			P22/RTC1HZ	–	–	7
INTP03			P23/SIF1/TXDC1/SDA00	–	13	16
INTP04			P24/SOF1/RXDC1/SDL00	–	14	17
INTP05			P26/TIAA31/TOAA31	–	16	19
INTP06			P35/SCKF4/TIAA21/TOAA21 /TOAA1OFF	–	–	80
			P35/TIAA21/TOAA21/TOAA1OFF	–	65	–
INTP07			P50/DDI	16	20	25
INTP08			P51/DDO	17	21	26
INTP09			P52/DCK	18	22	27
INTP10			P53/DMS	19	23	28

Note Available only in on-chip CAN controller products

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
INTP11	Input	External interrupt request input (maskable, analog noise elimination).	P54/DRST	20	24	29
INTP12			P90/TOAB1T1/TOAB11/TIAB11 /KR0	–	57	72
INTP13			P92/TOAB1T2/TOAB12/TIAB12 /KR2	–	59	74
INTP14			P93/TOAB1B2/TRGAB1/KR3	–	60	75
INTP15			P94/TOAB1T3/TOAB13/TIAB13 /KR4	–	61	76
INTP16			P95/TOAB1B3/EVTAB1/KR5	–	62	77
INTP17			P98/TENC01	–	33	42
INTP18			P912/TOAB1OFF	–	63	78
INTP19			P913/SIF3	–	–	30
			P913	–	25	–
INTP20			P914/SOF3	–	–	31
KR0	Input	Key interrupt input (analog noise elimination)	P90/TOAB1T1/TOAB11/TIAB11 /INTP12	–	57	72
KR1			P91/TOAB1B1/TIAB10/TOAB10	–	58	73
KR2			P92/TOAB1T2/TOAB12/TIAB12 /INTP13	–	59	74
KR3			P93/TOAB1B2/TRGAB1/INTP14	–	60	75
KR4			P94/TOAB1T3/TOAB13/TIAB13 /INTP15	–	61	76
KR5			P95/TOAB1B3/EVTAB1/INTP16	–	62	77
KR6			P96/TECR0/TIT00/TOT00	–	31	40
KR7			P97/TENC00/TIT01/TOT01	–	32	41
NMI	Input	External interrupt (non-maskable, analog noise elimination)	P02	3	3	3
P1COL	Input	Collision detection input for Ethernet	–	46	54	69
P1CRS	Input	Carrier detection input for Ethernet	–	45	53	68
P1MDC	Output	Serial transmit clock output	–	32	40	50
P1MDIO	I/O	Serial I/O	–	47	55	70
P1RXCLK	Input	Receive clock input for Ethernet	–	48	56	71
P1RXD0	Input	Receive data input for Ethernet	–	39	47	57
P1RXD1	Input	Receive data input for Ethernet	–	33	41	51
P1RXD2	Input	Receive data input for Ethernet	–	34	42	52
P1RXD3	Input	Receive data input for Ethernet	–	35	43	53
P1RXDV	Input	Receive data VALID input for Ethernet	–	36	44	54
P1RXER	Input	Receive data error input for Ethernet	–	37	45	55
P1TXCLK	Output	Transmit clock output for Ethernet	–	38	46	56
P1TXD0	Output	Transmit data output for Ethernet	–	26	34	44
P1TXD1	Output	Transmit data output for Ethernet	–	27	35	45
P1TXD2	Output	Transmit data output for Ethernet	–	28	36	46
P1TXD3	Output	Transmit data output for Ethernet	–	29	37	47
P1TXEN	Output	Transmit data enable output for Ethernet	–	31	39	49
P1TXER	Output	Transmit error output for Ethernet	–	30	38	48

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
TIAA00	Input	Capture trigger input/external event input/external trigger input (TAA0)	P30/TXDC0/SIF2/TOAA00	13	17	20
TIAA01		Capture trigger input (TAA0)	P31/RXDC0/SOF2/TOAA01	14	18	21
TIAA10		Capture trigger input/external event input/external trigger input (TAA1)	P32/ASCKC0/SCKF2/TOAA10	15	19	22
TIAA11		Capture trigger input (TAA1)	P33/SIF4/TXDB0/TOAA11	–	–	23
TIAA20		Capture trigger input/external event input/external trigger input (TAA2)	P34/SOF4/RXDB0/TOAA20	–	–	24
TIAA21		Capture trigger input (TAA2)	P35/SCKF4/TOAA21/TOAA1OFF /INTP06	–	–	80
			TIAA21/TOAA21/TOAA1OFF/INT P06	–	65	–
TIAA30		Capture trigger input/external event input/external trigger input (TAA3)	P25/SCKF1/TOAA30	–	15	18
TIAA31		Capture trigger input (TAA3)	P26/TOAA31/INTP05	–	16	19
TIAA40		Capture trigger input/external event input/external trigger input (TAA4)	P42/SCKF0/TOAA40/RTP02	54	70	87
TIAA41		Capture trigger input (TAA4)	P45/SCKE0/TOAA41/RTP05	–	–	90
TIAB10	Input	Capture trigger input/external event input/external trigger input (TAB1) N-ch open-drain output selectable.	P91/TOAB1B1/KR1/TOAB10	–	58	73
TIAB11		Capture trigger input (TAB1) N-ch open-drain output selectable.	P90/TOAB1T1/TOAB11/KR0/INTP12	–	57	72
TIAB12		P92/TOAB1T2/TOAB12/KR2/INTP13	–	59	74	
TIAB13		P94/TOAB1T3/TOAB13/KR4/INTP15	–	61	76	
TIT00	Input	Capture trigger input of TMT0	P96/TECR0/KR6/TOT00	–	31	40
TIT01		N-ch open-drain output selectable.	P97/TENC00/KR7/TOT01	–	32	41
TOAA00	Output	Timer output (TAA0) N-ch open-drain output selectable.	P30/TXDC0/SIF2/TIAA00	13	17	20
TOAA01		P31/RXDC0/SOF2/TIAA01	14	18	21	
TOAA10		Timer output (TAA1) N-ch open-drain output selectable.	P32/ASCKC0/SCKF2/TIAA10	15	19	22
TOAA11		P33/SIF4/TIAA11	–	–	23	
TOAA1OFF	Input	TAA1 High-impedance output control signal input	P35/SCKF4/TIAA21/TOAA21/INTP06	–	–	80
			P35/TIAA21/TOAA21/INTP06	–	65	–
TOAA20	Output	Timer output (TAA2)	P34/SOF4/TIAA20	–	–	24
TOAA21		N-ch open-drain output selectable.	P35/SCKF4/TIAA21/TOAA1OFF /INTP06	–	–	80
			P35/TIAA21/TOAA1OFF/INTP06	–	65	–
			TOAA30	Timer output (TAA3)	P25/SCKF1/TIAA30/	–
TOAA31		N-ch open-drain output selectable.	P26/TIAA31/INTP05	–	16	19
TOAA40		Timer output (TAA4)	P42/SCKF0/TIAA40/RTP02	54	70	87
TOAA41		N-ch open-drain output selectable.	P45/SCKE0/TIAA41/RTP05	–	–	90
TOAB10		Output	Timer output (TAB1)	P91/TOAB1B1/TIAB10/KR1	–	58
TOAB11	N-ch open-drain output selectable.		P90/TOAB1T1/TIAB11/KR0/INTP12	–	57	72
TOAB12	P92/TOAB1T2/TIAB12/KR2/INTP13		–	59	74	
TOAB13	P94/TOAB1T3/TIAB13/KR4/INTP15		–	61	76	

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
TOAB1B1	Output	Pulse signal output for 6-phase PWM low arm of TAB1	P91/TIAB10/KR1/TOAB10	–	58	73
TOAB1B2			P93/TRGAB1/KR3/INTP14	–	60	75
TOAB1B3			P95/EVTAB1/KR5/INTP16	–	62	77
TOAB1OFF	Input	TAB1 High-impedance output control signal input	P912/INTP18	–	63	78
TOAB1T1	Output	Pulse signal output for 6-phase PWM high arm of TAB1. N-ch open-drain output selectable.	P90/TOAB11/TIAB11/KR0/INTP12	–	57	72
TOAB1T2			P92/TOAB12/TIAB12/KR2/INTP13	–	59	74
TOAB1T3			P94/TOAB13/TIAB13/KR4/INTP15	–	61	76
TOT00	Output	Timer output of TMT0	P96/TECR0/TIT00/KR6	–	31	40
TOT01		N-ch open-drain output selectable	P97/TENC00/TIT01/KR7	–	32	41
TRGAB1	Input	External trigger input of TAB1 N-ch open-drain output selectable	P93/TOAB1B2/KR3/INTP14	–	60	75
TXDC0	Output	Serial transmit data output (UARTC0 to UARTC3) N-ch open-drain output selectable.	P30/SIF2/TIAA00/TOAA00	13	17	20
TXDC1			P23/SIF1/SDA00/INTP03	–	13	16
TXDC2			P36/SDA02/CTXD0 ^{Note}	50	66	81
TXDC3			P40/SIF0/SDA01/RTP00	52	68	85
UDMF	I/O	USB data I/O (–) function	–	21	26	35
UDPF		USB data I/O (+) function	–	22	27	36
UV _{DD}	–	3.3 V positive power supply for USB	–	23	28	37
V _{DD}	–	Positive power supply for internal circuit	–	5	5	8
V _{SS}	–	Ground potential for internal circuit	–	7	7	10
X1	Input	Connecting resonator for main clock	–	8	8	11
X2			–	9	9	12
XT1	Input	Connecting resonator for subclock	–	8	11	14
XT2			–	9	12	15

Note Available only in on-chip CAN controller products.

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

2. CPU FUNCTIONS

The CPU of the V850ES/JE3-E, V850ES/JF3-E and V850ES/JG3-E is based on RISC architecture and executes most instructions in a 1-clock cycle by using a 5-stage pipeline.

The features of the CPU are as follows.

- Minimum instruction execution time: 20 ns (@ 50 MHz operation with main clock (f_{xx}))
30.5 μs (@ 32.768 kHz operation with sub-clock (f_{XT}))
- Memory space Program space: 64 MB linear
 Data space: 4 GB linear
- General-purpose registers: 32 bits × 32 registers
- Internal 32-bit architecture
- 5-stage pipeline control
- Multiplication/division instructions
- Saturation operation instructions
- 1-clock 32-bit shift instruction
- Load/store instructions with long/short format
- Internal memory

Table 2-1. ROM/RAM

Generic Name	Products	Flash Memory Size	RAM Size	
			Internal RAM	Data RAM
V850ES/JE3-E	μPD70F3826	64 KB	16 KB	16 KB
	μPD70F3827	128 KB	32 KB	16 KB
	μPD70F3828	256 KB	48 KB	16 KB
	μPD70F3829	256 KB	48 KB	16 KB
V850ES/JF3-E	μPD70F3830	64 KB	16 KB	16 KB
	μPD70F3831	128 KB	32 KB	16 KB
	μPD70F3832	256 KB	48 KB	16 KB
	μPD70F3833	256 KB	48 KB	16 KB
V850ES/JG3-E	μPD70F3834	64 KB	16 KB	16 KB
	μPD70F3835	128 KB	32 KB	16 KB
	μPD70F3836	256 KB	48 KB	16 KB
	μPD70F3837	256 KB	48 KB	16 KB

- Four types of bit manipulation instructions
 - SET1
 - CLR1
 - NOT1
 - TST1

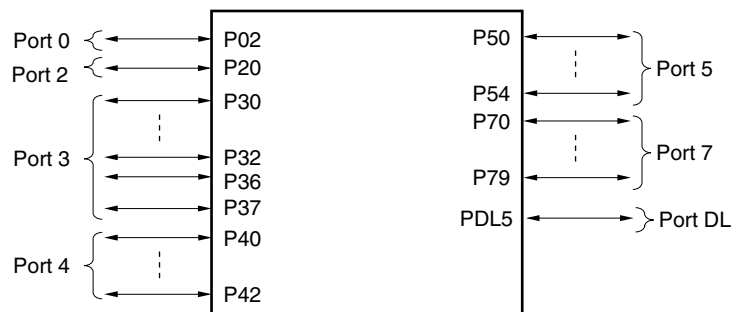
4. PORTS

The number of I/O ports of the V850ES/Jx3-E is shown below.

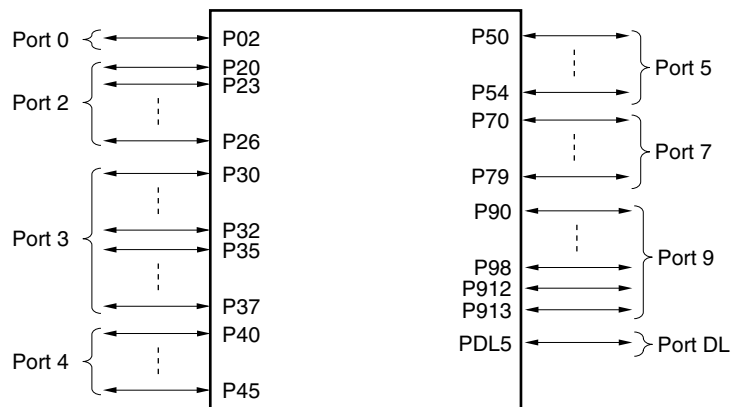
Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of ports (5 V tolerant)	26 (12)	42 (28)	62 (35)

The following figure shows the basic configurations of ports.

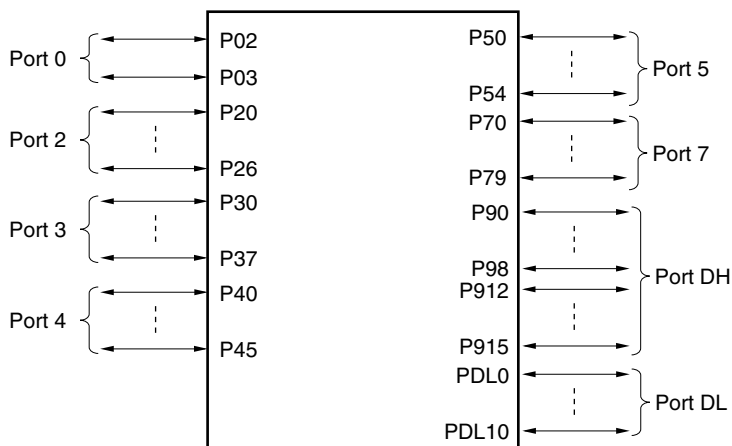
(a) V850ES/JE3-E



(b) V850ES/JF3-E



(c) V850ES/JG3-E



11. REAL-TIME COUNTER

In the V850ES/Jx3-E, one channel of real-time counter is provided.

The real-time counter has the following features.

- It has counters for year, month, week, day, hours, minutes and seconds, and it can count up to 99 years.
- The year, month, week, day, hour, minute and second counters show the count in BCD code^{Note 1}.
- Alarm interrupt function
- Fixed-cycle interrupt function (cycle: 1 month to 0.5 seconds)
- Interval interrupt function (cycle: 1.95 to 125 ms)
- 1 Hz pin output
- 32.768 kHz pin output
- 512 Hz or 16.384 kHz pin output
- Watch error correction function
- Subclock operation or main clock operation^{Note 2} selectable

Notes 1. BCD (binary-coded decimal) code is the code that represents each digit of a decimal number in 4-bit binary numerals.

2. The main clock can be divided into 32.768 kHz f_{BRG} with the baud rate generator dedicated to the real-time counter.

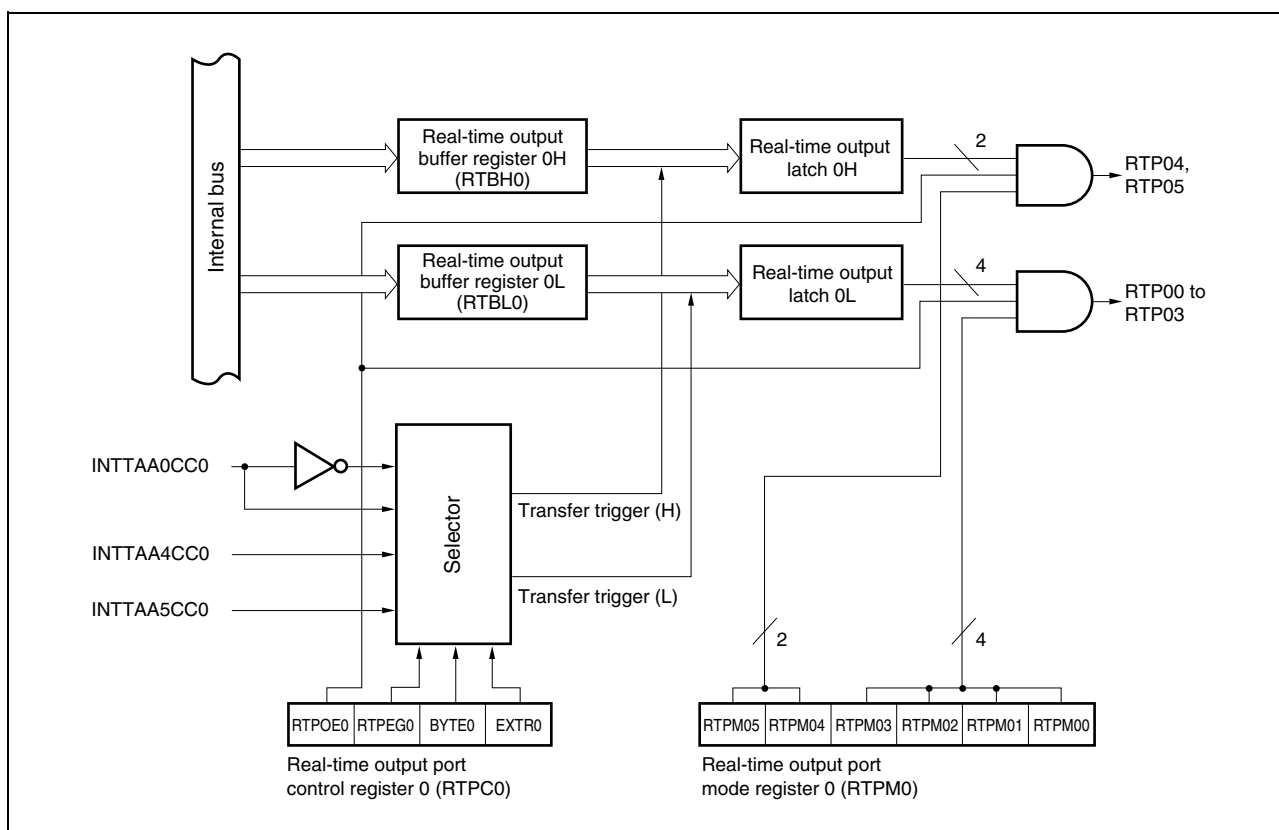
13. REAL-TIME OUTPUT FUNCTION (RTO)

In the V850ES/Jx3-E, one channel of real-time output is provided.

The RTO has the following features.

- 6-bit real-time output port: 1 channel
- The real-time output port can be set to the port mode or real-time output port mode in 1-bit units.

The RTO has the following configurations.



15. ASYNCHRONOUS SERIAL INTERFACE C (UARTC)

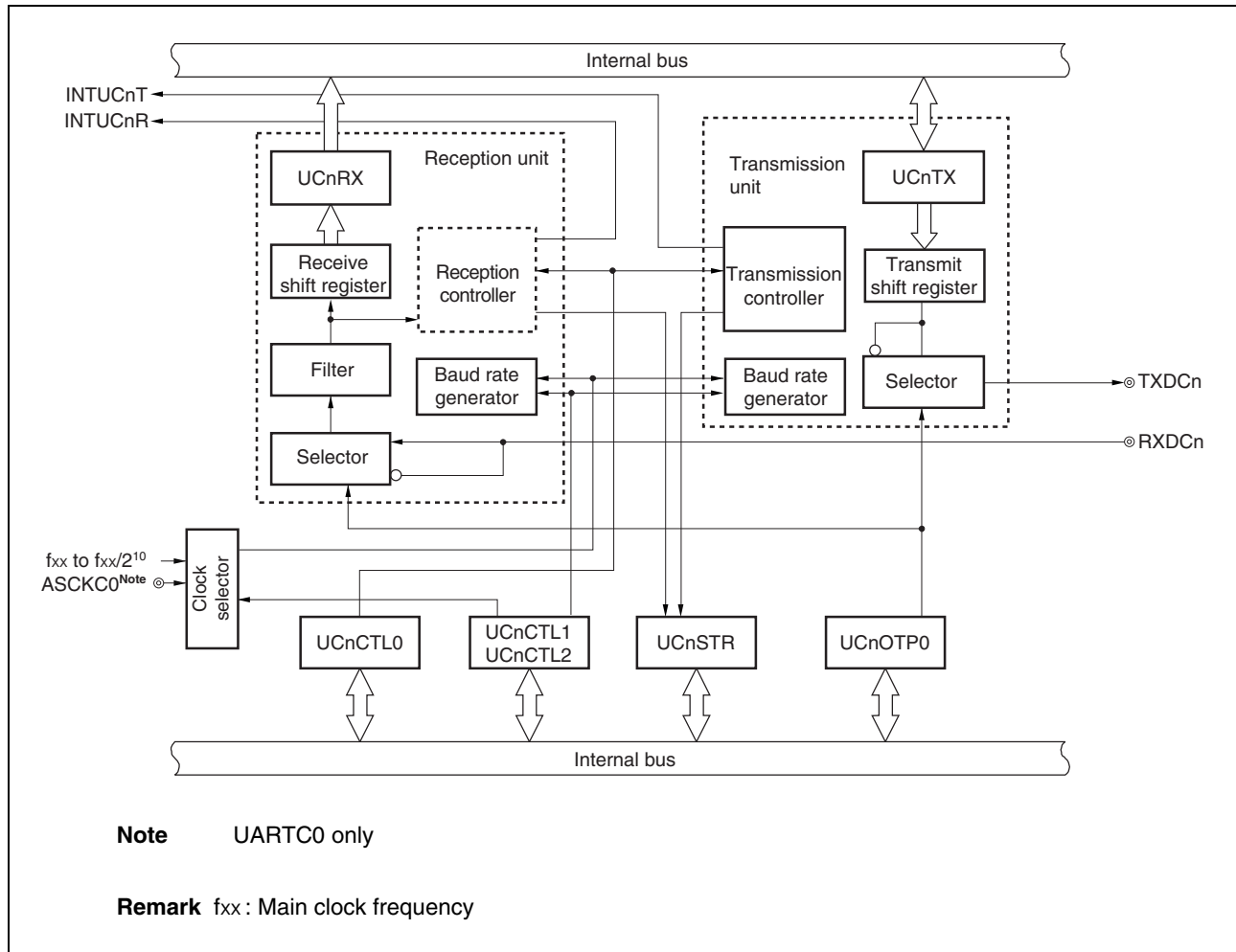
The number of UARTC of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	3 channels (UARTC0, UARTC2 and UARTC3)	4 channels (UARTC0 to UARTC3)	4 channels (UARTC0 to UARTC3)

The UARTC has the following features.

- Transfer rate: 300 bps to 3.125 Mbps (using internal system clock of 24 MHz and dedicated baud rate generator)
- Full-duplex communication: On-chip UARTCn receive data register (UCnRX)
On-chip UARTCn transmit data register (UCnTX)
- 2-pin configuration: TXDCn: Transmit data output pin
RXDCn: Receive data input pin
- Reception error detect function
 - Parity error
 - Framing error
 - Overrun error
 - LIN communication data consistency error detect function
 - SBF reception success detect function
- Interrupt sources: 2 types
 - Reception completion interrupt (INTUCnR): This interrupt occurs upon transfer of receive data from the receive shift register to receive data register after serial transfer completion, in the reception enabled status.
 - Transmission enable interrupt (INTUCnT): This interrupt occurs upon transfer of transmit data from the transmit data register to the transmit shift register in the transmission enabled status.
- Character length: 7, 8, 9 bits
- Parity function: Odd, even, 0, none
- Transmission stop bit: 1, 2 bits
- On-chip dedicated baud rate generator
- MSB-/LSB-first transfer selectable
- Transmit/receive data inverted input/output possible
- SBF (Sync Break Field) transmission/reception in the LIN (Local Interconnect Network) communication format possible
 - 13 to 20 bits are selectable for SBF transmission
 - Recognition of 11 bits or more possible for SBF reception in LIN format
 - SBF reception flag provided

The following figure shows the configuration of UARTC.



22. INTERRUPT/EXCEPTION PROCESSING FUNCTION

The features of interrupt/exception processing function is shown below.

○ Interrupts

		Internal			External		
		Non maskable	Maskable	Total	Non maskable	Maskable	Total
V850ES/JE3-E	μPD70F3826	1	53	54	1	6	7
	μPD70F3827	1	53	54	1	6	7
	μPD70F3828	1	53	54	1	6	7
	μPD70F3829	1	57	58	1	6	7
V850ES/JF3-E	μPD70F3830	1	56	57	1	18	19
	μPD70F3831	1	56	57	1	18	19
	μPD70F3832	1	56	57	1	18	19
	μPD70F3833	1	60	61	1	18	19
V850ES/JG3-E	μPD70F3834	1	60	61	1	21	22
	μPD70F3835	1	60	61	1	21	22
	μPD70F3836	1	60	61	1	21	22
	μPD70F3837	1	64	65	1	21	22

- 8 levels of programmable priorities
- Masks interrupt requests according to priority
- Masks can be specified for each maskable interrupt request.
- Noise elimination, edge detection, and valid edge specification for external interrupt request signals.

○ Exceptions

- Software exceptions: 32 sources
- Exception trap: 2 sources (illegal opcode exception, debug trap)

Interrupt/exception sources are listed in Table 22-1.

24. STANDBY FUNCTION

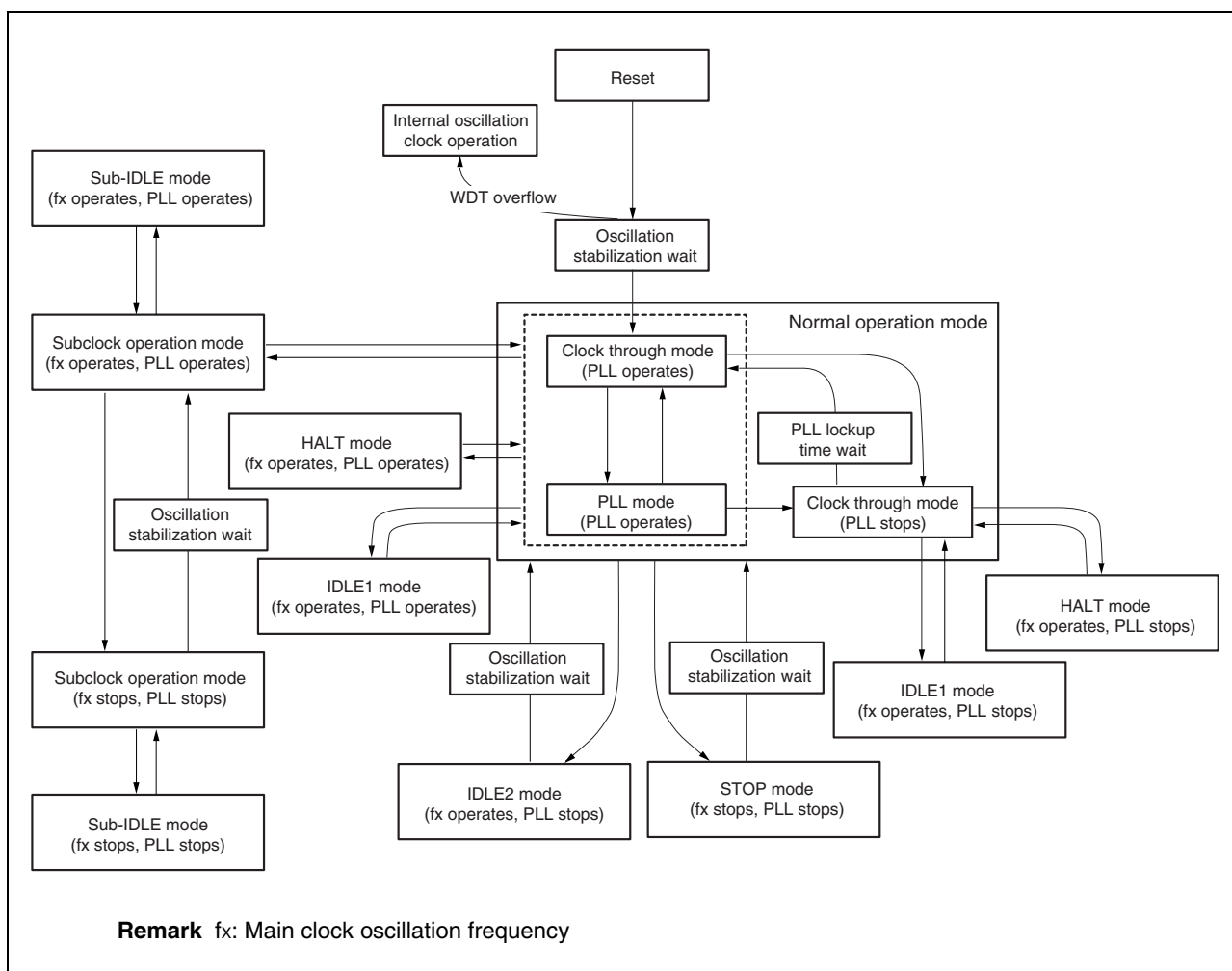
The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. The available standby modes are listed in Table 24-1.

Table 24-1. Standby Modes

Mode	Function Overview
HALT mode	Mode to stop only the operating clock of the CPU
IDLE1 mode	Mode to stop all the operations of the internal circuit except the oscillator, PLL operation ^{Note} , and flash memory
IDLE2 mode	Mode to stop all the operations of the internal circuit except the oscillator
STOP mode	Mode to stop all the operations of the internal circuit except the subclock oscillator
Subclock operation mode	Mode to operate internal system clock by subclock
Sub-IDLE mode	Mode to stop all the operations of the internal circuit except the oscillator in subclock operation mode

Note PLL retains the previous operation status.

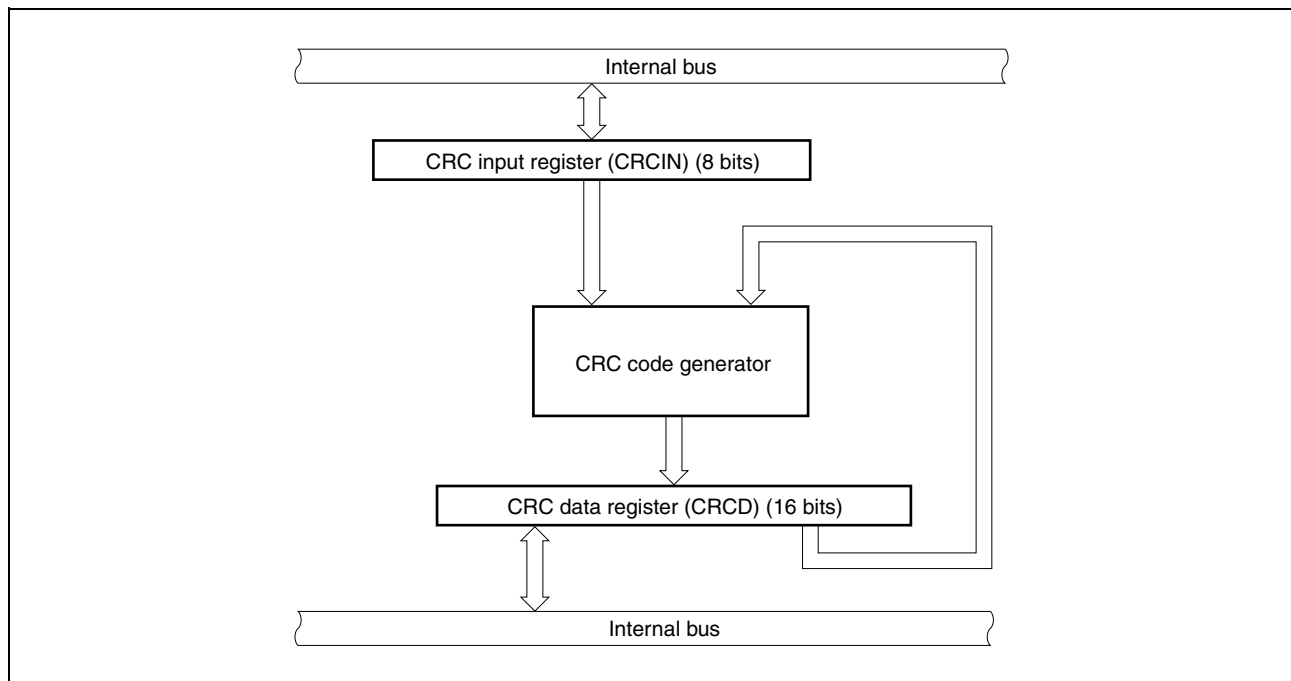
The following figure shows the status transitions of the standby function.



27. CRC FUNCTIONS

The outline of the CRC function is shown below.

- CRC operation circuit for detection of data block errors
- Generation of 16-bit CRC code using a CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) generation polynomial for blocks of data of any length in 8-bit units
- CRC code is set to the CRCD data register each time 1-byte data is transferred to the CRCIN register, after the initial value is set to the CRCD register.



30. ON-CHIP DEBUG FUNCTION

Debugging can be implemented with the V850ES/Jx3-E mounted on the target system.

The NEC Electronics on-chip debug emulators MINICUBE and MINICUBE2 are planned to support the V850ES/Jx3-E.

○ MINICUBE

An on-chip debug function is implemented by using the DCU (debug control unit) in the V850ES/Jx3-E, using the $\overline{\text{DRST}}$, DCK, DMS, DDI, and DDO pins as the debug interface pins.

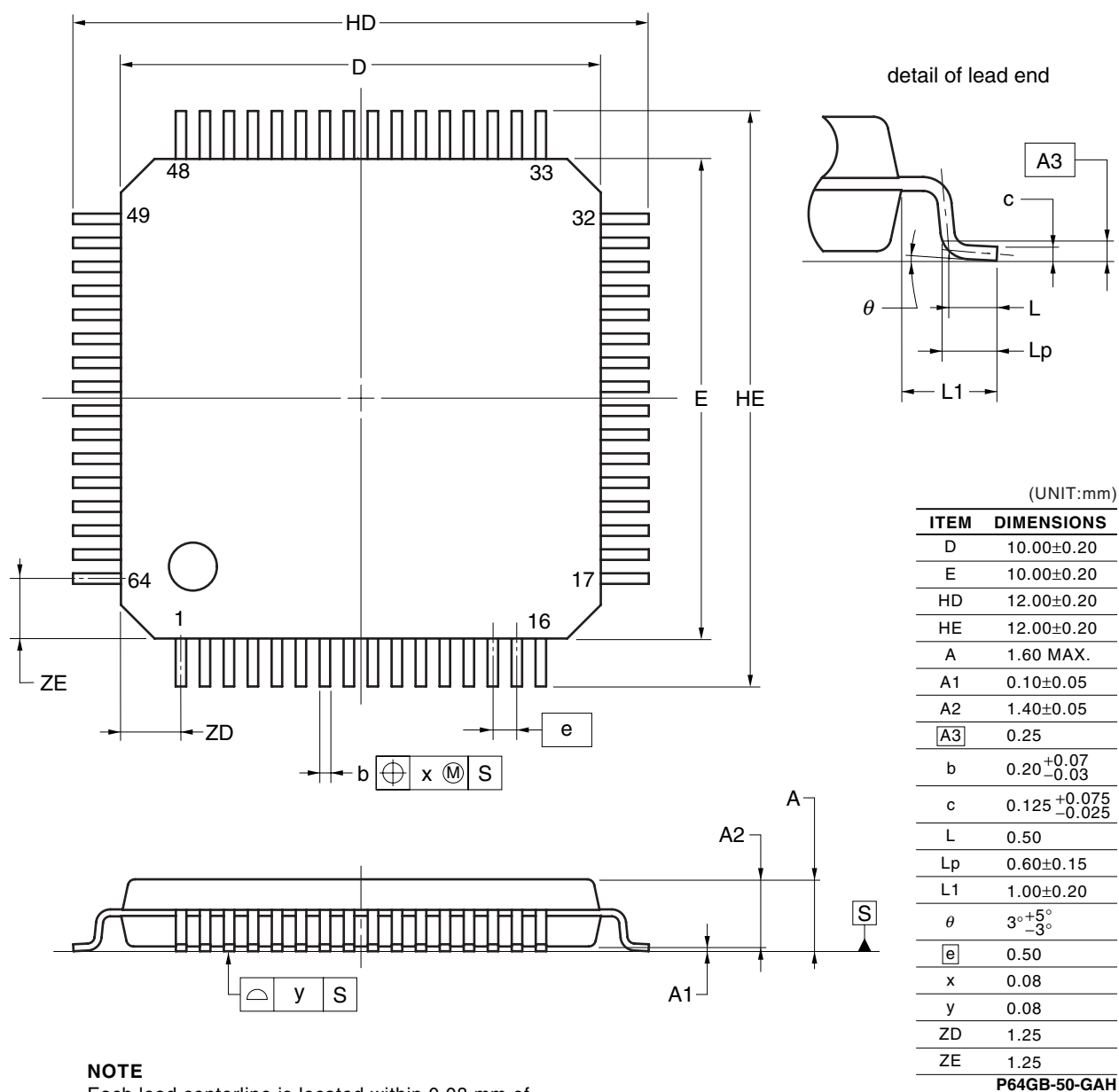
○ MINICUBE2

An on-chip debug function is implemented by using the user resources (on-chip flash memory, internal RAM, etc.) instead of the DCU, and using the SIF0, SOF0, and $\overline{\text{SCKF0}}$ pins or the SIF3, SOF3, and $\overline{\text{SCKF3}}$ pins or the RXDC0 and TXDC0 pins as the interface pins.

31. PACKAGE DRAWINGS

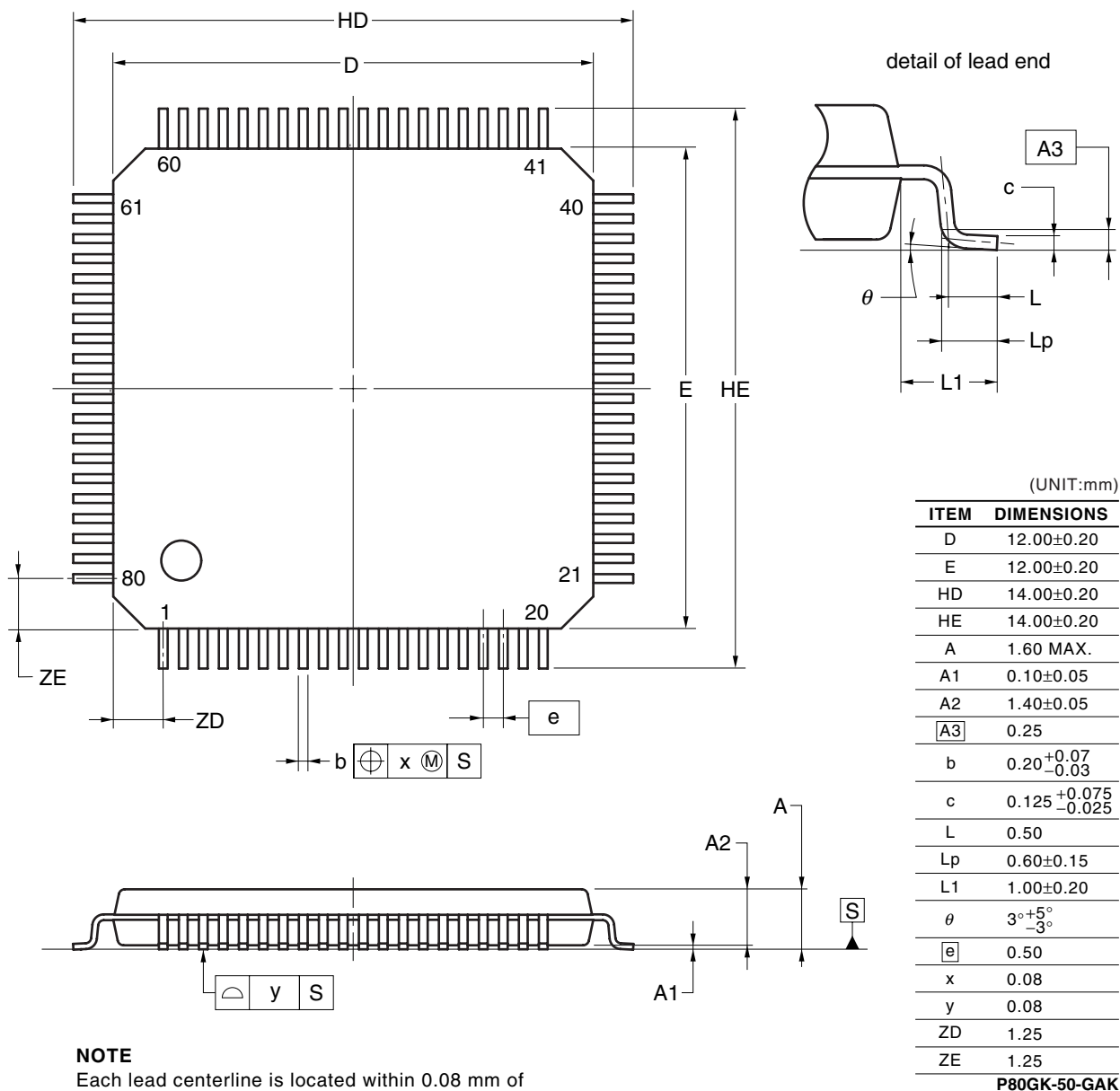
- V850ES/JE3-E

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)



- V850ES/JF3-E

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)



NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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