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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, CSI, Ethernet, I ² C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	62
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3835gc-r-ueu-ax

Function list (V850ES/JE3-E)

Generic Name		V850ES/JE3-E			
Product Name		μPD70F3826	μPD70F3827	μPD70F3828	μPD70F3829
Internal memory	Flash memory	64 KB	128 KB	256 KB	256 KB
	Internal RAM	16 KB	32 KB	48 KB	48 KB
	Data RAM	16 KB	16 KB	16 KB	16 KB
Memory space		64 MB			
General-purpose register		32 bits × 32 registers			
Clocks	Main clock oscillation	PLL mode : $f_x = 3$ to 6.25 MHz, $f_{xx} = 24$ to 50 MHz (multiplication by 8) Clock through mode : $f_x = 3$ to 6.25 MHz (internal : $f_{xx} = 3$ to 6.25 MHz)			
	Subclock oscillation	$f_{XT} = 32.768$ kHz			
	Internal oscillation	$f_R = 220$ kHz (TYP.)			
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{xx}))			
I/O ports		I/O: 26 (5 V tolerant : 12)			
Timer	16-bit TAA	5 channels (among which two channels have the interval function only)			
	16-bit TAB	—			
	16-bit TMM	4 channels			
	16-bit TMT	1 channel (Interval function only)			
	Motor control	—			
	Watch timer	1 channel (RTC)			
	WDT	1 channel			
Real-time output function		6 bits × 1 channel			
10-bit A/D converter		10 channels			
Serial interface	CSIF/UARTC	1 channel			
	CSIF/UARTC/I ² C	1 channel			
	CSIF	—			
	UARTC/I ² C	1 channel			—
	UARTC/I ² C/CAN	—			1 channel
USB function		1 channel			
Ethernet controller		1 channel			
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)			
Interrupt source	External ^{Note 1, 2}	7(7)	7(7)	7(7)	7(7)
	Internal	54	54	54	58
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes			
Reset factor		RESET pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)			
On-chip debugging		MINICUBE®, MINICUBE2 supported			
Operating supply voltage		2.85 to 3.6 V			
Operating ambient temperature		−40 to +85°C			
Package		64-pin plastic LQFP (fine pitch) (10 × 10 mm), 64-pin plastic WQFN (9 × 9 mm),			

- Notes**
1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.
 2. Include NMI.

Function list (V850ES/JF3-E)

Generic Name		V850ES/JF3-E			
Product Name		μPD70F3830	μPD70F3831	μPD70F3832	μPD70F3833
Internal memory	Flash memory	64 KB	128 KB	256 KB	256 KB
	Internal RAM	16 KB	32 KB	48 KB	48 KB
	Data RAM	16 KB	16 KB	16 KB	16 KB
Memory space		64 MB			
General-purpose register		32 bits × 32 registers			
Clocks	Main clock oscillation	PLL mode : $f_x = 3$ to 6.25 MHz, $f_{xx} = 24$ to 50 MHz (multiplication by 8) Clock through mode : $f_x = 3$ to 6.25 MHz (internal : $f_{xx} = 3$ to 6.25 MHz)			
	Subclock oscillation	$f_{XT} = 32.768$ kHz			
	Internal oscillation	$f_R = 220$ kHz (TYP.)			
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{xx}))			
I/O ports		I/O: 42 (5 V tolerant : 28)			
Timer	16-bit TAA	5 channels			
	16-bit TAB	1 channel			
	16-bit TMM	4 channels			
	16-bit TMT	1 channel			
	Motor control	1 channel			
	Watch timer	1 channel (RTC)			
	WDT	1 channel			
Real-time output function		6 bits × 1 channel			
10-bit A/D converter		10 channels			
Serial interface	CSIF/UARTC	1 channel			
	CSIF/UARTC/I ² C	2 channels			
	CSIF	—			
	UARTC/I ² C	1 channel			—
	UARTC/I ² C/CAN	—			1 channel
USB function		1 channel			
Ethernet controller		1 channel			
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)			
Interrupt source	External ^{Note 1, 2}	19(19)	19(19)	19(19)	19(19)
	Internal	57	57	57	61
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes			
Reset factor		RESET pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)			
On-chip debugging		MINICUBE, MINICUBE2 supported			
Operating supply voltage		2.85 to 3.6 V			
Operating ambient temperature		−40 to +85°C			
Package		80-pin plastic LQFP (fine pitch) (12 × 12 mm)			

- Notes**
1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.
 2. Include NMI.

APPLICATIONS

- Applications that require Ethernet controller
Home audio, printers, and scanners.

ORDERING INFORMATION

• V850ES/JE3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3826GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	64 KB
μPD70F3827GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	128 KB
μPD70F3828GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB
μPD70F3829GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB
μPD70F3826K8-6B4-AX	64-pin plastic WQFN (9 × 9)	64 KB
μPD70F3827K8-6B4-AX	64-pin plastic WQFN (9 × 9)	128 KB
μPD70F3828K8-6B4-AX	64-pin plastic WQFN (9 × 9)	256 KB
μPD70F3829K8-6B4-AX	64-pin plastic WQFN (9 × 9)	256 KB

• V850ES/JF3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3830GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	64 KB
μPD70F3831GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	128 KB
μPD70F3832GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	256 KB
μPD70F3833GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	256 KB

• V850ES/JG3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3834GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	64 KB
μPD70F3835GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	128 KB
μPD70F3836GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB
μPD70F3837GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB
μPD70F3837F1-CAH-AX ^{Note}	113-pin plastic FBGA (8 × 8)	256 KB

Note Under planning

Remark The V850ES/Jx3-E microcontrollers are lead-free products.

• V850ES/JE3-E

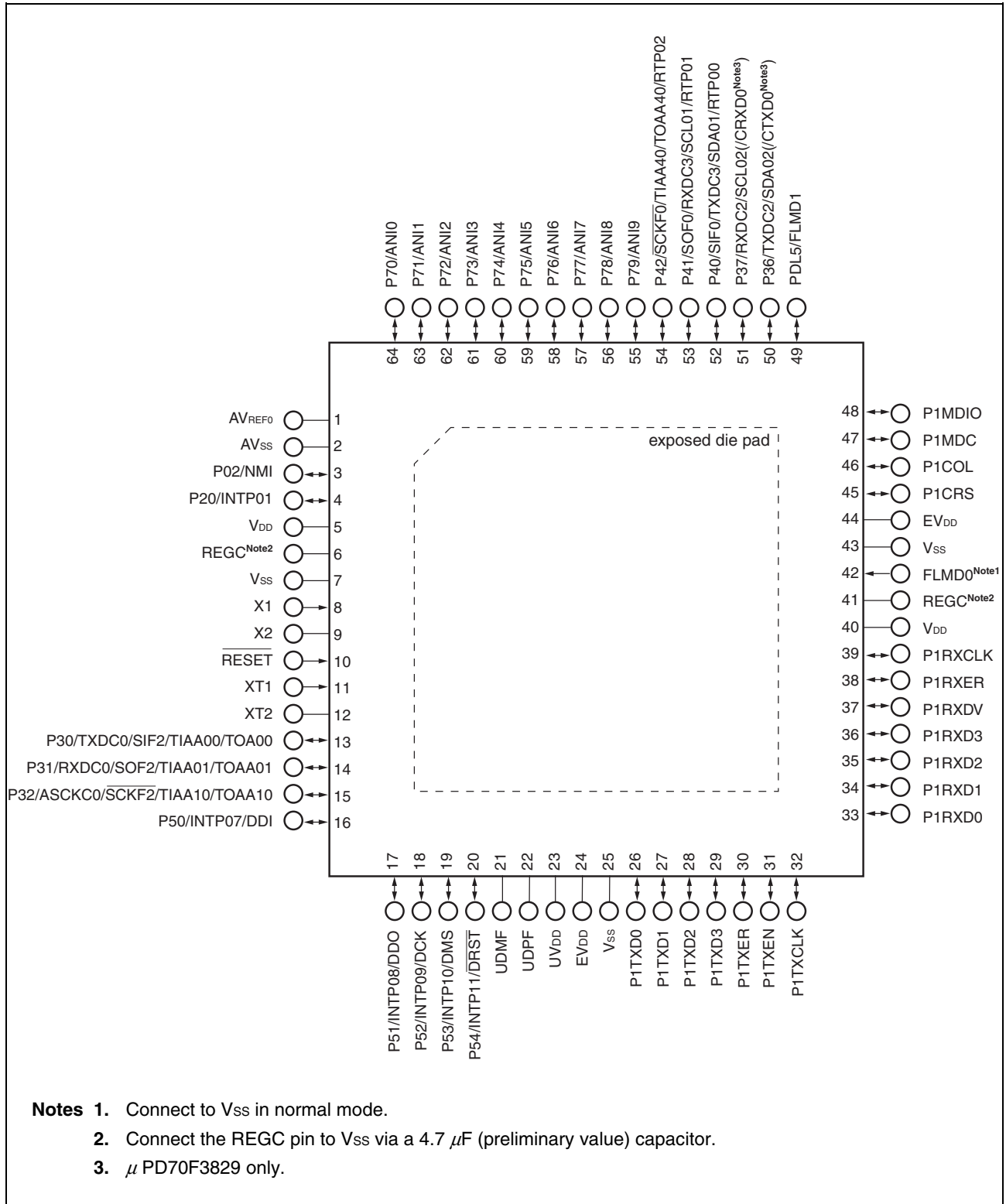
64-pin plastic WQFN (9 × 9)

μPD70F3826K8-6B4-AX

μPD70F3827K8-6B4-AX

μPD70F3828 K8-6B4-AX

μPD70F3829K8-6B4-AX



PIN IDENTIFICATION

ADTRG:	A/D Trigger Input	RXDC0 to RXDC3	Receive Data
ANI0 to ANI9:	Analog Input	$\overline{\text{SCKF0}}$ to $\overline{\text{SCKF4}}$:	Serial Clock
ASCKC0:	Asynchronous Serial Clock	SCL00 to SCL02:	Serial Clock
AVREF0:	Analog Reference Voltage	SDA00 to SDA02:	Serial Data
AVSS:	Grand for Analog Pin	SIF0 to SIF4:	Serial Input
CRXD0:	CAN Receive Data	SOF0 to SOF4:	Serial Output
CTXD0:	CAN Transmit Data	TECR0:	Timer Encoder Clear Input
DCK:	Debug Clock	TENC00, TENC01:	Timer Encoder Input
DDI:	Debug Data Input	TIAA00, TIAA01,	Timer Input
DDO:	Debug Data Output	TIAA10, TIAA11,	
DMS:	Debug Mode Select	TIAA20, TIAA21,	
$\overline{\text{DRST}}$:	Debug Reset	TIAA30, TIAA31,	
EVDD:	Power Supply for External Pin	TIAA40, TIAA41,	
EVTAB1:	Timer Event Count Input	TIAB10 to TIAB13,	
EXCLK	USB clock	TIT00, TIT01:	
FLMD0, FLMD1:	Flash Programming Mode	TOAA00, TOAA01,	Timer Output
INTP00 to INTP20:	External Interrupt Input	TOAA10, TOAA11,	
KR0 to KR7:	Key Return	TOAA20, TOAA21,	
NMI:	Non-maskable Interrupt Request	TOAA30, TOAA31,	
P02, P03:	Port0	TOAA40, TOAA41,	
P1COL, P1CRS,	Ethernet PHY Interface	TOAB10 to TOAB13,	
P1MDC, P1MDIO,		TOAB1B1 to TOAB1B3,	
P1RXCLK,		TOAB1T1 to TOAB1T3,	
P1RXD0 to P1RXD3,		TOT00, TOT01:	
P1RXDV, P1RXER		TOAA1OFF,	Timer Output Off
P1TXCLK,		TOAB1OFF	
P1TXD0 to P1TXD3,		TRGAB1:	Timer Trigger Input
P1TXEN, P1TXER:		TXDC0 to TXDC3:	Serial Output
P20 to P26	Port2	UDMF:	USB Data I/O (-) Function
P30 to P37:	Port3	UDPF:	USB Data I/O (+) Function
P40 to P45:	Port4	UVDD:	Power Supply for External USB
P50 to P54:	Port5	VDD:	Power Supply
P70 to P79:	Port7	VSS:	Ground
P90 to P98,	Port9	X1, X2:	Crystal for Main Clock
P912 to P915:		XT1, XT2:	Crystal for Sub-clock
PDL0 to PDL10:	Port DL		
REGC:	Regulator Control		
$\overline{\text{RESET}}$:	Reset		
RTC1HZ, RTCCL,	Real-time Counter Clock Output		
RTCDIV:			
RTP00 to RTP05:	Real-time Output Port		

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
P70	I/O	Port 7 10-bit I/O port Input/output can be specified in 1-bit units.	ANI0	64	80	100
P71			ANI1	63	79	99
P72			ANI2	62	78	98
P73			ANI3	61	77	97
P74			ANI4	60	76	96
P75			ANI5	59	75	95
P76			ANI6	58	74	94
P77			ANI7	57	73	93
P78			ANI8	56	72	92
P79			ANI9	55	71	91
P90	I/O	Port 9 13-bit I/O port(V850ES/JG3-E) 11-bit I/O port(V850ES/JF3-E) Input/output can be specified in 1-bit units.	TOAB1T1/TOAB11/TIAB11/KR0/INTP12	–	57	72
P91			TOAB1B1/TIAB10/KR1/TOAB10	–	58	73
P92			TOAB1T2/TOAB12/TIAB12/KR2/INTP13	–	59	74
P93			TOAB1B2/TRGAB1/KR3/INTP14	–	60	75
P94			TOAB1T3/TOAB13/TIAB13/KR4/INTP15	–	61	76
P95			TOAB1B3/EVTB1/KR5/INTP16	–	62	77
P96			TECR0/TIT00/KR6/TOT00	–	31	40
P97			TENC00/TIT01/KR7/TOT01	–	32	41
P98			TENC01/INTP17	–	33	42
P912			TOAB1OFF/INTP18	–	63	78
P913			SIF31/INTP19	–	–	30
			INTP19	–	25	–
P914			SOF3/INTP20	–	–	31
P915			SCKF3	–	–	32
PDL0	I/O	Port DL 11-bit I/O port(V850ES/JG3-E) 1-bit I/O port(V850ES/JF3-E, V850ES/JE3-E) Input/output can be specified in 1-bit units.	–	–	–	58
PDL1			–	–	–	59
PDL2			–	–	–	60
PDL3			–	–	–	66
PDL4			–	–	–	67
PDL5			FLMD1	49	64	79
PDL6			–	–	–	83
PDL7			–	–	–	84
PDL8			–	–	–	33
PDL9			–	–	–	34
PDL10			–	–	–	43

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

1.2 Non-Port Pins

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Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
ADTRG	Input	External trigger input for A/D converter	P03/INTP00/EXCLK	–	–	4
ANI0	Input	Analog voltage input for A/D converter	P70	64	80	100
ANI1			P71	63	79	99
ANI2			P72	62	78	98
ANI3			P73	61	77	97
ANI4			P74	60	76	96
ANI5			P75	59	75	95
ANI6			P76	58	74	94
ANI7			P77	57	73	93
ANI8			P78	56	72	92
ANI9			P79	55	71	91
ASCKC0	Input	UARTC0 baud rate clock input	P32/SCKF2/TIAA10/TOAA10	15	19	22
AVREF0	–	Reference voltage input for A/D converter, and positive power supply for port 7	–	1	1	1
AVSS	–	Ground voltage for A/D converter	–	2	2	2
CRXD0 ^{Note}	Input	CAN receive data input	P37/RXDC2/SCL02	51	67	82
CTXD0 ^{Note}	Output	CAN transmit data output	P36/TXDC2/SDA02	50	66	81
DCK	Input	Clock input for on-chip debugging	P52/INTP09	18	22	27
DDI	Input	Data input for on-chip debugging	P50/INTP07	16	20	25
DDO	Output	Data output for on-chip debugging In the on-chip debug mode, high-level output is forcibly set.	P51/INTP08	17	21	26
DMS	Input	Mode select signal input for on-chip debugging	P53/INTP10	19	23	28
DRST	Input	Reset signal input for on-chip debugging	P54/INTP11	20	24	29
EVDD	–	Positive power supply for external (same potential as VDD)	–	24, 44	29, 52	38, 65
EVTAB1	Input	External event count input of TAB1	P95/TOAB1B3/KR5/INTP16	–	62	77
EXCLK	Input	USB clock signal input	P03/INTP00/ADTRG	–	–	4
FLMD0	Input	Flash programming mode setting pins	–	42	50	63
FLMD1	Input		PDL5/AD5	49	64	79
INTP00	Input	External interrupt request input (maskable, analog noise elimination). Analog noise elimination or digital noise elimination selectable for INTP02 pin.	P03/ADTRG/EXCLK	–	–	4
INTP01			P20	4	4	5
INTP02			P22/RTC1HZ	–	–	7
INTP03			P23/SIF1/TXDC1/SDA00	–	13	16
INTP04			P24/SOF1/RXDC1/SDL00	–	14	17
INTP05			P26/TIAA31/TOAA31	–	16	19
INTP06			P35/SCKF4/TIAA21/TOAA21 /TOAA1OFF	–	–	80
			P35/TIAA21/TOAA21/TOAA1OFF	–	65	–
INTP07			P50/DDI	16	20	25
INTP08			P51/DDO	17	21	26
INTP09			P52/DCK	18	22	27
INTP10			P53/DMS	19	23	28

Note Available only in on-chip CAN controller products

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

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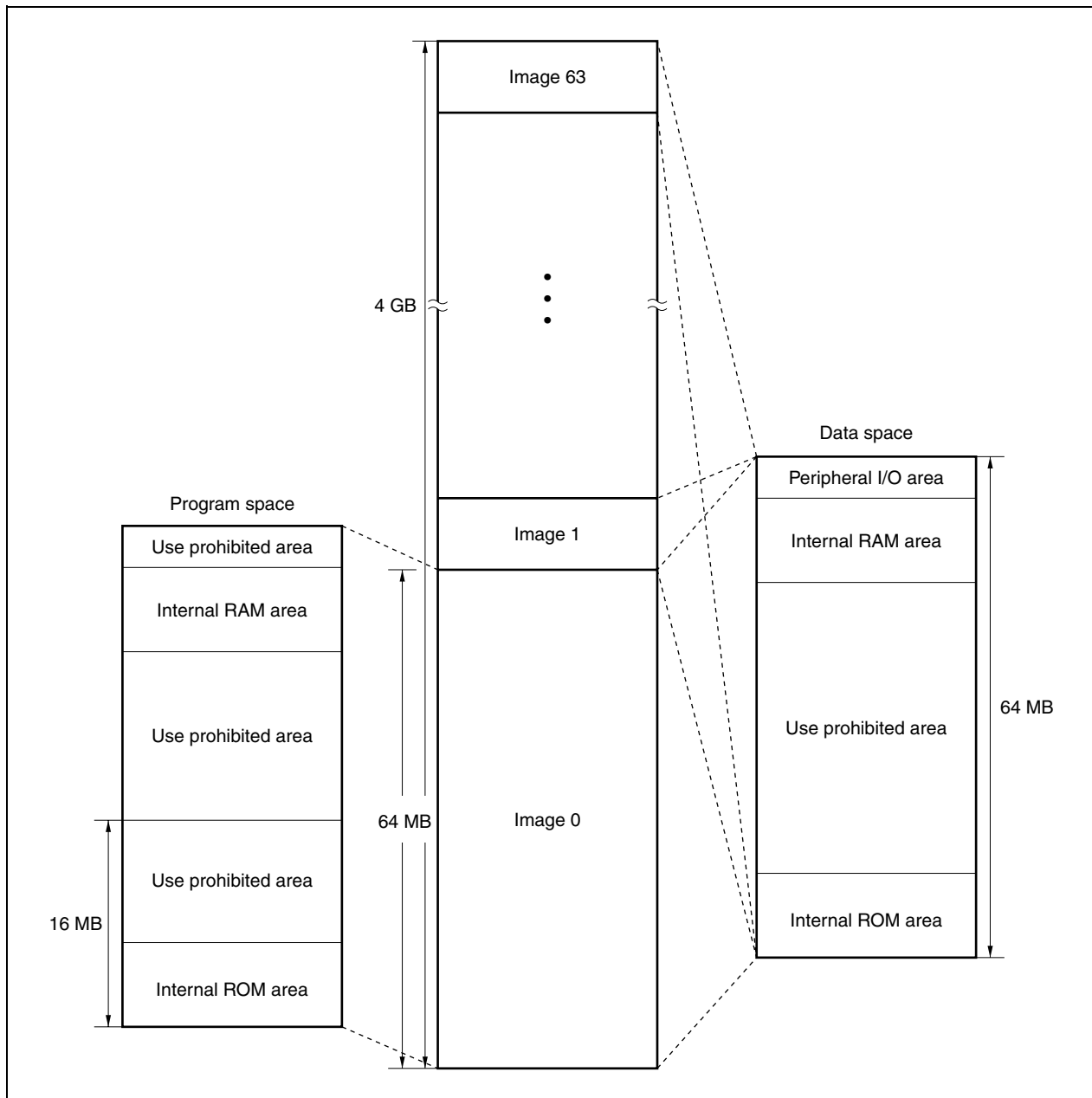
Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
TIAA00	Input	Capture trigger input/external event input/external trigger input (TAA0)	P30/TXDC0/SIF2/TOAA00	13	17	20
TIAA01		Capture trigger input (TAA0)	P31/RXDC0/SOF2/TOAA01	14	18	21
TIAA10		Capture trigger input/external event input/external trigger input (TAA1)	P32/ASCKC0/SCKF2/TOAA10	15	19	22
TIAA11		Capture trigger input (TAA1)	P33/SIF4/TXDB0/TOAA11	–	–	23
TIAA20		Capture trigger input/external event input/external trigger input (TAA2)	P34/SOF4/RXDB0/TOAA20	–	–	24
TIAA21		Capture trigger input (TAA2)	P35/SCKF4/TOAA21/TOAA1OFF /INTP06	–	–	80
			TIAA21/TOAA21/TOAA1OFF/INT P06	–	65	–
TIAA30		Capture trigger input/external event input/external trigger input (TAA3)	P25/SCKF1/TOAA30	–	15	18
TIAA31		Capture trigger input (TAA3)	P26/TOAA31/INTP05	–	16	19
TIAA40		Capture trigger input/external event input/external trigger input (TAA4)	P42/SCKF0/TOAA40/RTP02	54	70	87
TIAA41	Capture trigger input (TAA4)	P45/SCKE0/TOAA41/RTP05	–	–	90	
TIAB10	Input	Capture trigger input/external event input/external trigger input (TAB1) N-ch open-drain output selectable.	P91/TOAB1B1/KR1/TOAB10	–	58	73
TIAB11		Capture trigger input (TAB1) N-ch open-drain output selectable.	P90/TOAB1T1/TOAB11/KR0/INTP12	–	57	72
TIAB12			P92/TOAB1T2/TOAB12/KR2/INTP13	–	59	74
TIAB13			P94/TOAB1T3/TOAB13/KR4/INTP15	–	61	76
TIT00	Input	Capture trigger input of TMT0	P96/TECR0/KR6/TOT00	–	31	40
TIT01		N-ch open-drain output selectable.	P97/TENC00/KR7/TOT01	–	32	41
TOAA00	Output	Timer output (TAA0)	P30/TXDC0/SIF2/TIAA00	13	17	20
TOAA01		N-ch open-drain output selectable.	P31/RXDC0/SOF2/TIAA01	14	18	21
TOAA10		Timer output (TAA1)	P32/ASCKC0/SCKF2/TIAA10	15	19	22
TOAA11		N-ch open-drain output selectable.	P33/SIF4/TIAA11	–	–	23
TOAA1OFF	Input	TAA1 High-impedance output control signal input	P35/SCKF4/TIAA21/TOAA21/INTP06	–	–	80
			P35/TIAA21/TOAA21/INTP06	–	65	–
TOAA20	Output	Timer output (TAA2)	P34/SOF4/TIAA20	–	–	24
TOAA21		N-ch open-drain output selectable.	P35/SCKF4/TIAA21/TOAA1OFF /INTP06	–	–	80
			P35/TIAA21/TOAA1OFF/INTP06	–	65	–
			TOAA30	Timer output (TAA3)	P25/SCKF1/TIAA30/	–
TOAA31		N-ch open-drain output selectable.	P26/TIAA31/INTP05	–	16	19
TOAA40		Timer output (TAA4)	P42/SCKF0/TIAA40/RTP02	54	70	87
TOAA41		N-ch open-drain output selectable.	P45/SCKE0/TIAA41/RTP05	–	–	90
TOAB10	Output	Timer output (TAB1)	P91/TOAB1B1/TIAB10/KR1	–	58	73
TOAB11		N-ch open-drain output selectable.	P90/TOAB1T1/TIAB11/KR0/INTP12	–	57	72
TOAB12		P92/TOAB1T2/TIAB12/KR2/INTP13	–	59	74	
TOAB13		P94/TOAB1T3/TIAB13/KR4/INTP15	–	61	76	

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

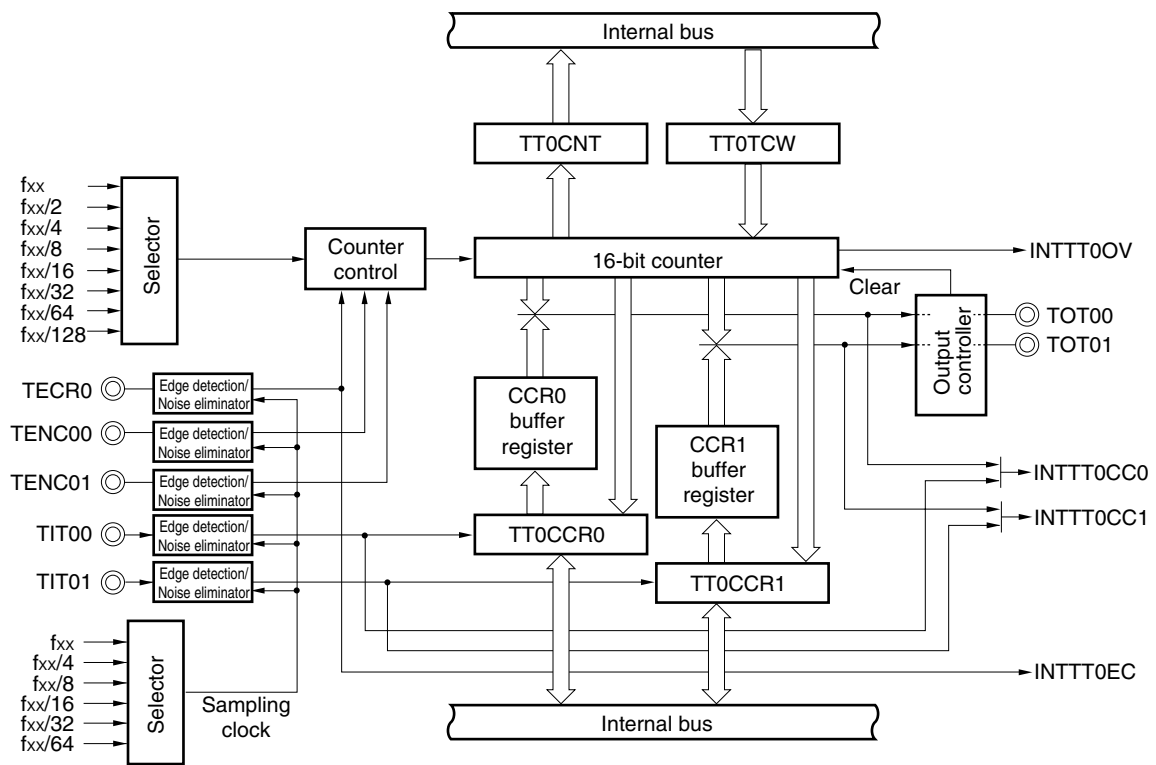
3. MEMORY MAP

The memory maps of the V850ES/JE3-E, V850ES/JF3-E and V850ES/JF3-E are shown below.

○ Address Space



The following figure shows the configuration of TMT.



Remark f_{xx} : Main clock frequency

15. ASYNCHRONOUS SERIAL INTERFACE C (UARTC)

The number of UARTC of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	3 channels (UARTC0, UARTC2 and UARTC3)	4 channels (UARTC0 to UARTC3)	4 channels (UARTC0 to UARTC3)

The UARTC has the following features.

- Transfer rate: 300 bps to 3.125 Mbps (using internal system clock of 24 MHz and dedicated baud rate generator)
- Full-duplex communication: On-chip UARTCn receive data register (UCnRX)
On-chip UARTCn transmit data register (UCnTX)
- 2-pin configuration: TXDCn: Transmit data output pin
RXDCn: Receive data input pin
- Reception error detect function
 - Parity error
 - Framing error
 - Overrun error
 - LIN communication data consistency error detect function
 - SBF reception success detect function
- Interrupt sources: 2 types
 - Reception completion interrupt (INTUCnR): This interrupt occurs upon transfer of receive data from the receive shift register to receive data register after serial transfer completion, in the reception enabled status.
 - Transmission enable interrupt (INTUCnT): This interrupt occurs upon transfer of transmit data from the transmit data register to the transmit shift register in the transmission enabled status.
- Character length: 7, 8, 9 bits
- Parity function: Odd, even, 0, none
- Transmission stop bit: 1, 2 bits
- On-chip dedicated baud rate generator
- MSB-/LSB-first transfer selectable
- Transmit/receive data inverted input/output possible
- SBF (Sync Break Field) transmission/reception in the LIN (Local Interconnect Network) communication format possible
 - 13 to 20 bits are selectable for SBF transmission
 - Recognition of 11 bits or more possible for SBF reception in LIN format
 - SBF reception flag provided

16. CLOCKED SERIAL INTERFACE F (CSIF)

The number of CSIF of the V850ES/Jx3-E is shown below.

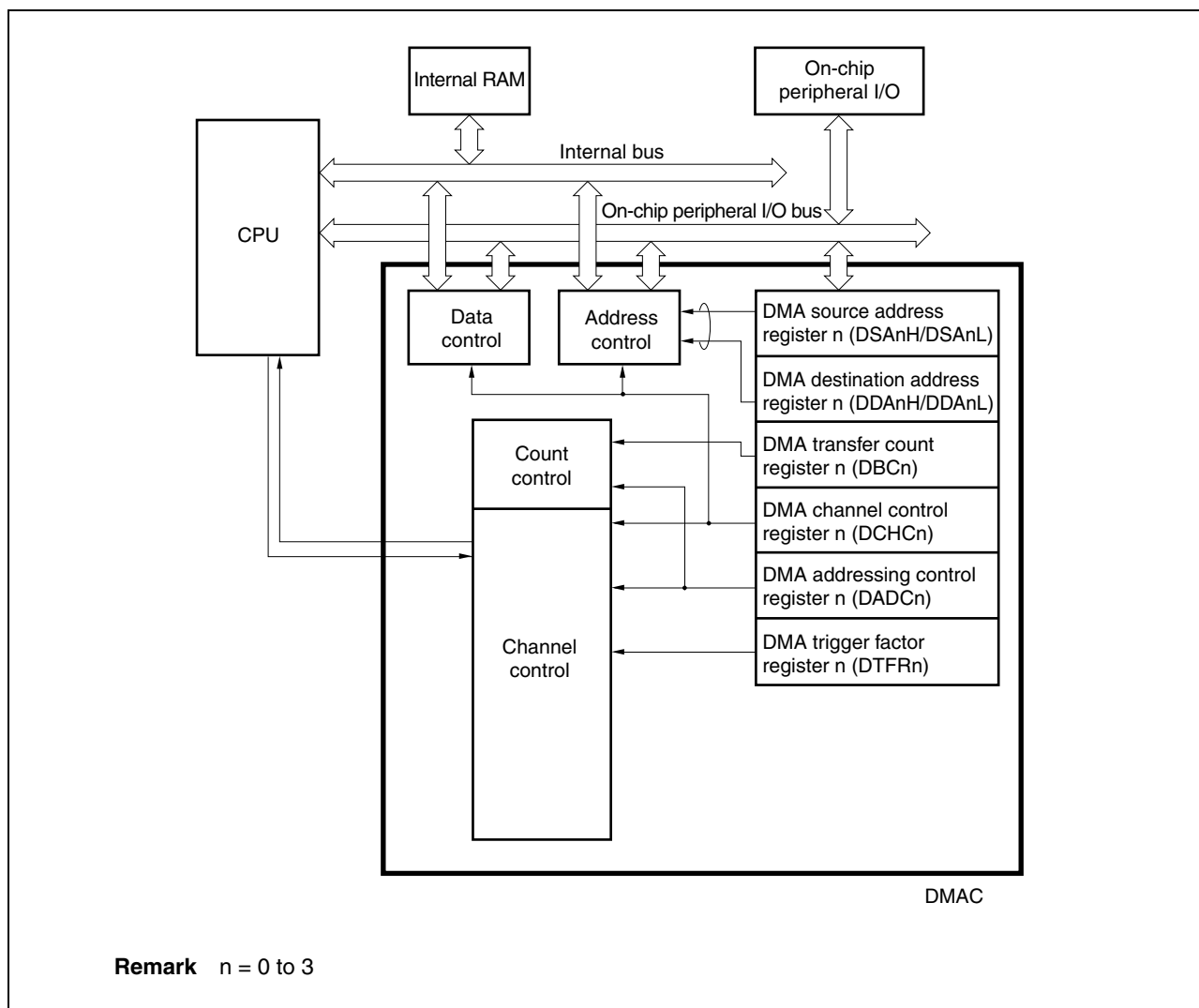
Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	2 channels (CSIF0 and CSIF2)	3 channels (CSIF0 to CSIF2)	5 channels (CSIF0 to CSIF4)

- Transfer rate: 8 Mbps max. (f_{xx} = 50 MHz, using internal clock)
 - Master mode and slave mode selectable
 - 8-bit to 16-bit transfer, 3-wire serial interface
 - Interrupt request signals (INTCFnT, INTCFnR)
 - Serial clock and data phase switchable
 - Transfer data length selectable in 1-bit units between 8 and 16 bits
 - Transfer data MSB-first/LSB-first switchable
 - 3-wire
 - SOFn: Serial data output
 - SIFn: Serial data input
 - SCKFn: Serial clock I/O
- Transmission mode, reception mode, and transmission/reception mode specifiable

The following figure shows the configuration of I²C.



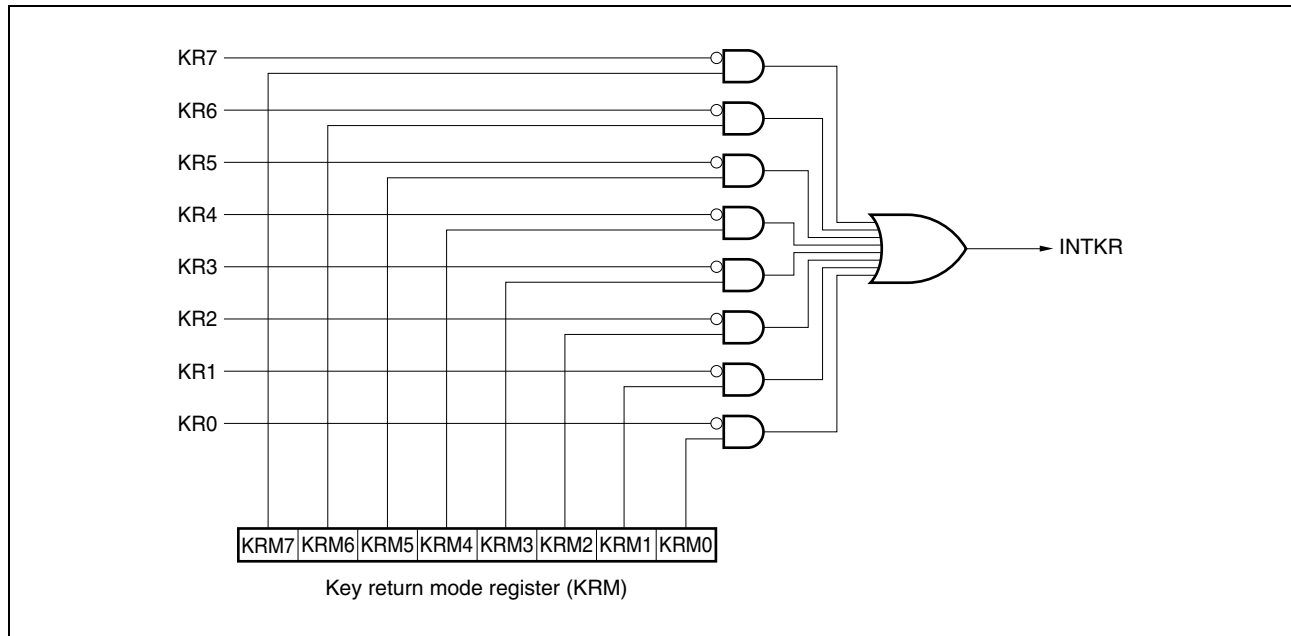
The following figure shows the configuration of DMA controller.



23. KEY INTERRUPT FUNCTION (V850ES/JF3-E, V850ES/JG3-E)

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins (KR0 to KR7).

The following figure shows the configuration of key interrupt.



24. STANDBY FUNCTION

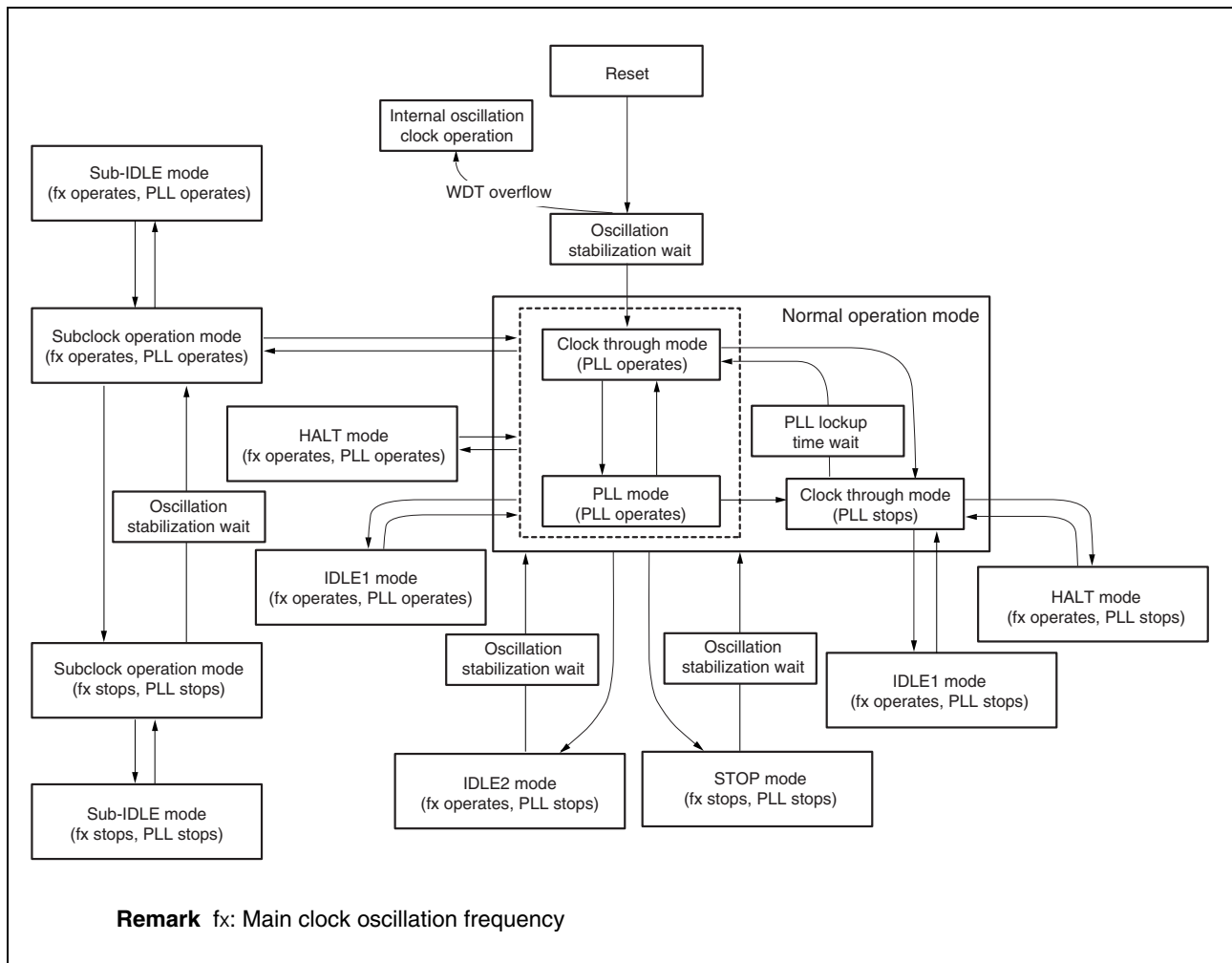
The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. The available standby modes are listed in Table 24-1.

Table 24-1. Standby Modes

Mode	Function Overview
HALT mode	Mode to stop only the operating clock of the CPU
IDLE1 mode	Mode to stop all the operations of the internal circuit except the oscillator, PLL operation ^{Note} , and flash memory
IDLE2 mode	Mode to stop all the operations of the internal circuit except the oscillator
STOP mode	Mode to stop all the operations of the internal circuit except the subclock oscillator
Subclock operation mode	Mode to operate internal system clock by subclock
Sub-IDLE mode	Mode to stop all the operations of the internal circuit except the oscillator in subclock operation mode

Note PLL retains the previous operation status.

The following figure shows the status transitions of the standby function.



25. RESET FUNCTIONS

The following reset functions are available.

(1) Four types of reset sources

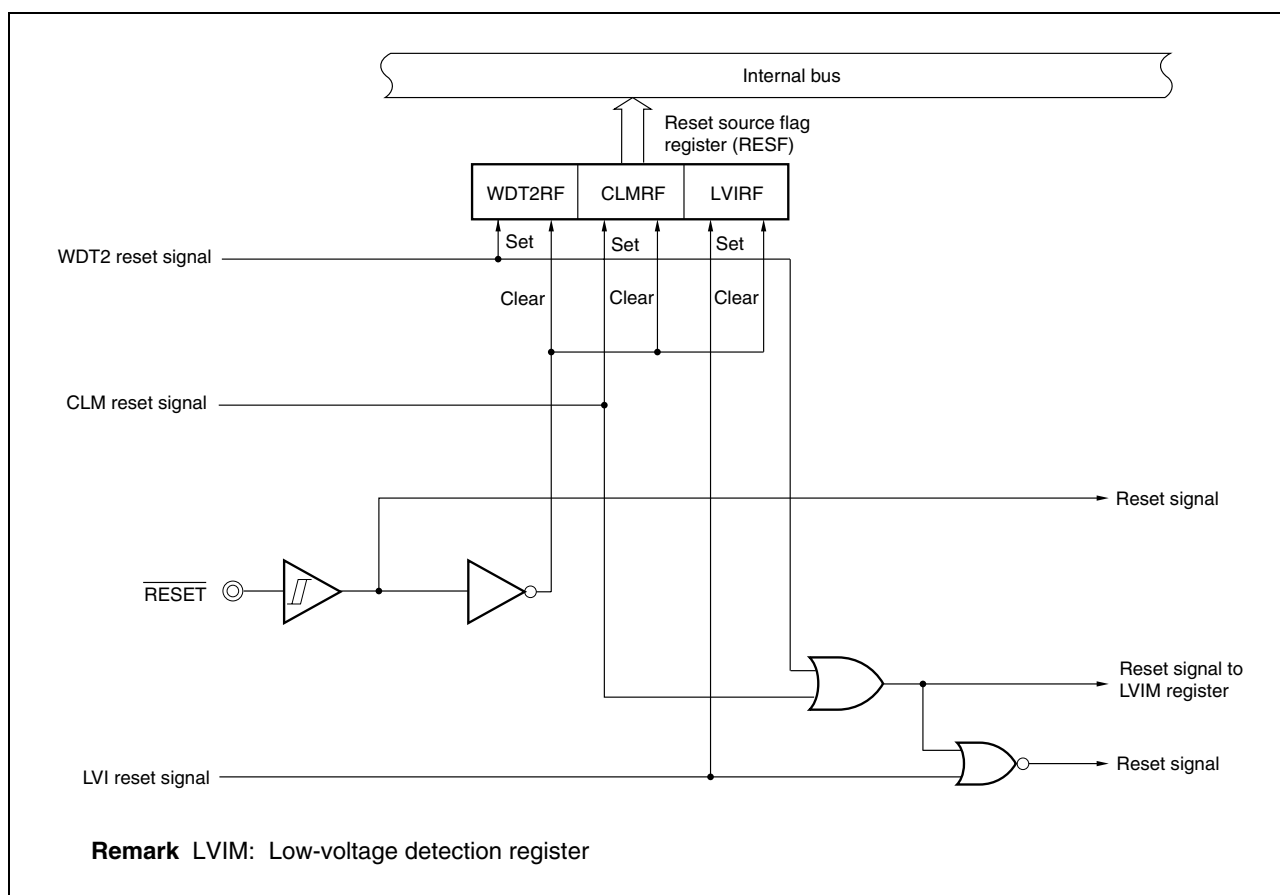
- External reset input via the $\overline{\text{RESET}}$ pin
- Reset via the watchdog timer 2 (WDT2) overflow (WDT2RES)
- System reset by comparing the supply voltage and detection voltage by using the low-voltage detector (LVI)
- System reset by the clock monitor (CLM) upon detection of oscillation stop

After a reset is released, the source of the reset can be confirmed with the reset source flag register (RESF).

(2) Emergency operation mode

If the WDT2 overflows during the main clock oscillation stabilization time inserted after reset, a main clock oscillation anomaly is judged and the CPU starts operating on the internal oscillation clock.

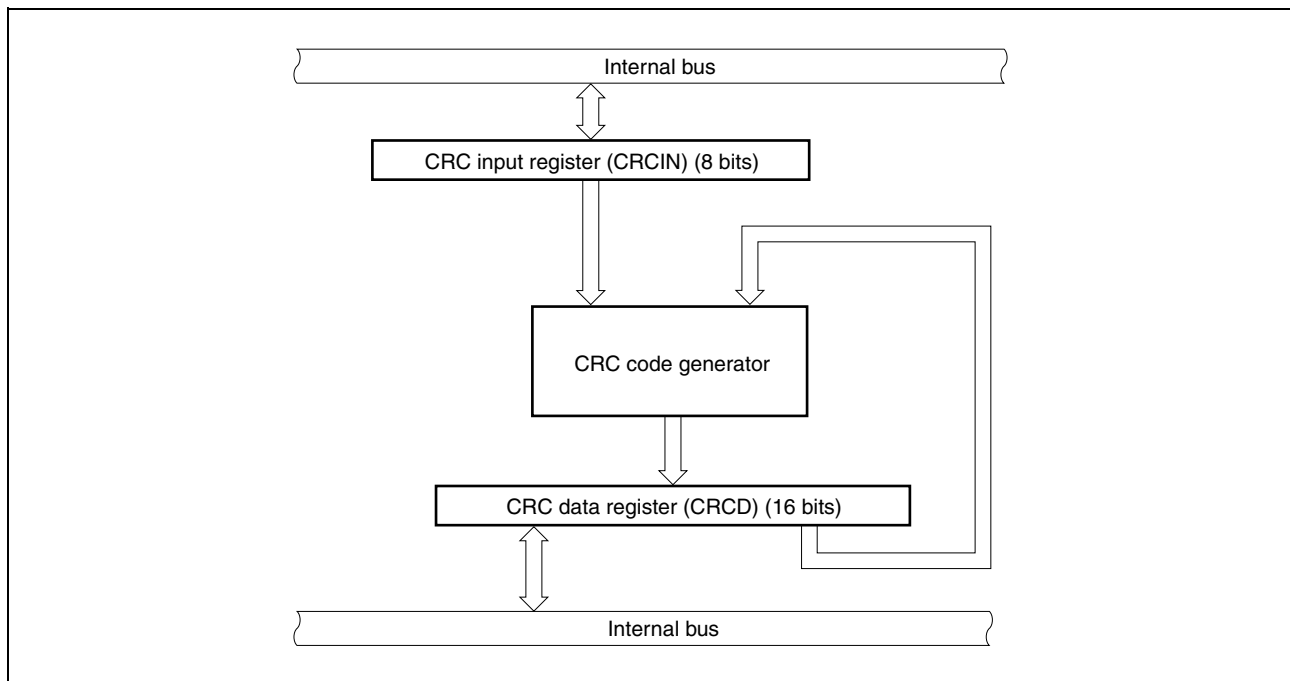
The outline of the reset functions is shown below.



27. CRC FUNCTIONS

The outline of the CRC function is shown below.

- CRC operation circuit for detection of data block errors
- Generation of 16-bit CRC code using a CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) generation polynomial for blocks of data of any length in 8-bit units
- CRC code is set to the CRCD data register each time 1-byte data is transferred to the CRCIN register, after the initial value is set to the CRCD register.



29. FLASH MEMORY

Flash memory versions offer the following advantages for development environments and mass production applications.

- For altering software after the V850ES/Jx3-E is soldered onto the target system.
- For data adjustment when starting mass production.
- For differentiating software according to the specification in small scale production of various models.
- For facilitating inventory management.
- For updating software after shipment.

The flash memory in the V850ES/Jx3-E has the following features.

- 4-byte/1-clock access (when instruction is fetched)
- Memory size: 64/128/256 KB
- Rewrite voltage: Erase/write with a single power supply
- Rewriting method
 - Rewriting by communication with dedicated flash programmer via serial interface (on-board/off-board programming)
 - Rewriting flash memory by user program (self programming)
- Flash memory write prohibit function supported (security function)
- Safe rewriting of entire flash memory area by self programming using boot swap function
- Interrupts can be acknowledged during self programming.

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