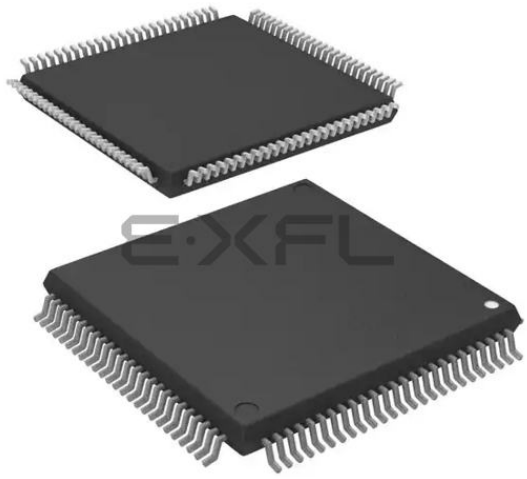
Renesas Electronics America Inc - UPD70F3836GC(R)-UEU-AX Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, CSI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	62
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3836gc-r-ueu-ax

Function list (V850ES/JF3-E)

Generic Name		V850ES/JF3-E			
Product Name		μPD70F3830	μPD70F3831	μPD70F3832	μPD70F3833
Internal memory	Flash memory	64 KB	128 KB	256 KB	256 KB
	Internal RAM	16 KB	32 KB	48 KB	48 KB
	Data RAM	16 KB	16 KB	16 KB	16 KB
Memory space		64 MB			
General-purpose register		32 bits × 32 registers			
Clocks	Main clock oscillation	PLL mode : f_X = 3 to 6.25 MHz, f_{XX} = 24 to 50 MHz (multiplication by 8) Clock through mode : f_X = 3 to 6.25 MHz (internal : f_{XX} = 3 to 6.25 MHz)			
	Subclock oscillation	f_{XT} = 32.768 kHz			
	Internal oscillation	f_R = 220 kHz (TYP.)			
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{XX}))			
I/O ports		I/O: 42 (5 V tolerant : 28)			
Timer	16-bit TAA	5 channels			
	16-bit TAB	1 channel			
	16-bit TMM	4 channels			
	16-bit TMT	1 channel			
	Motor control	1 channel			
	Watch timer	1 channel (RTC)			
	WDT	1 channel			
Real-time output function		6 bits × 1 channel			
10-bit A/D converter		10 channels			
Serial interface	CSIF/UARTC	1 channel			
	CSIF/UARTC/I²C	2 channels			
	CSIF	–			
	UARTC/I²C	1 channel			–
	UARTC/I²C/CAN	–			1 channel
USB function		1 channel			
Ethernet controller		1 channel			
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)			
Interrupt source	External Note 1, 2	19(19)	19(19)	19(19)	19(19)
	Internal	57	57	57	61
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes			
Reset factor		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)			
On-chip debugging		MINICUBE, MINICUBE2 supported			
Operating supply voltage		2.85 to 3.6 V			
Operating ambient temperature		–40 to +85°C			
Package		80-pin plastic LQFP (fine pitch) (12 × 12 mm)			

Notes 1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.

2. Include NMI.

APPLICATIONS

○ Applications that require Ethernet controller

Home audio, printers, and scanners.

ORDERING INFORMATION

- V850ES/JE3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3826GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	64 KB
μPD70F3827GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	128 KB
μPD70F3828GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB
μPD70F3829GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB
μPD70F3826K8-6B4-AX	64-pin plastic WQFN (9 × 9)	64 KB
μPD70F3827K8-6B4-AX	64-pin plastic WQFN (9 × 9)	128 KB
μPD70F3828K8-6B4-AX	64-pin plastic WQFN (9 × 9)	256 KB
μPD70F3829K8-6B4-AX	64-pin plastic WQFN (9 × 9)	256 KB

- V850ES/JF3-E

Part Number	Package	On-Chip Flash Memory
μPD70F3830GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	64 KB
μPD70F3831GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	128 KB
μPD70F3832GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	256 KB
μPD70F3833GK-GAK-AX	80-pin plastic LQFP (fine pitch) (12 × 12)	256 KB

- V850ES/JG3-E

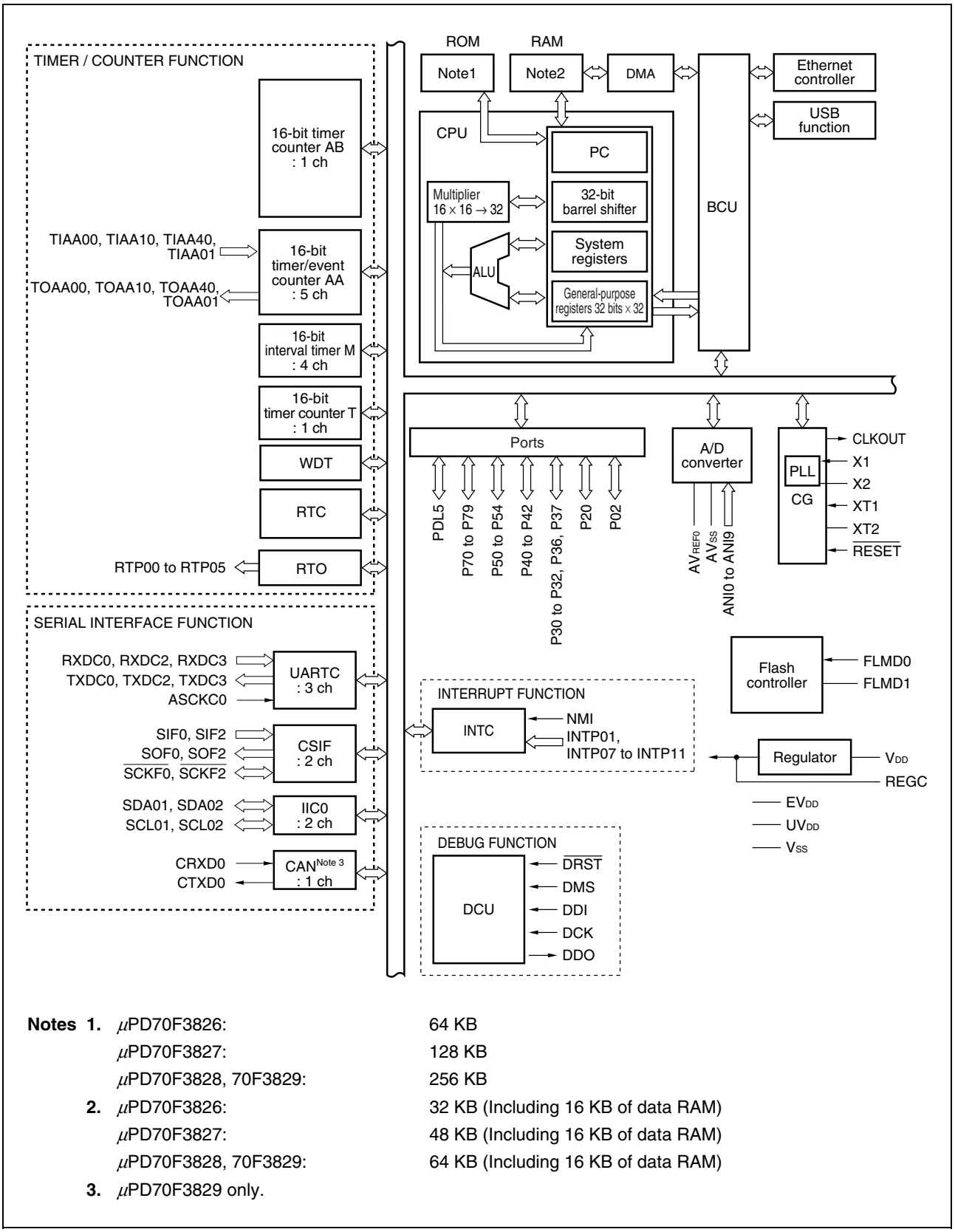
Part Number	Package	On-Chip Flash Memory
μPD70F3834GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	64 KB
μPD70F3835GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	128 KB
μPD70F3836GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB
μPD70F3837GC-UEU-AX	100-pin plastic LQFP (fine pitch) (14 × 14)	256 KB
μPD70F3837F1-CAH-AX[Note]	113-pin plastic FBGA (8 × 8)	256 KB

Note Under planning

Remark The V850ES/Jx3-E microcontrollers are lead-free products.

INTERNAL BLOCK DIAGRAM

- **V850ES/JE3-E**

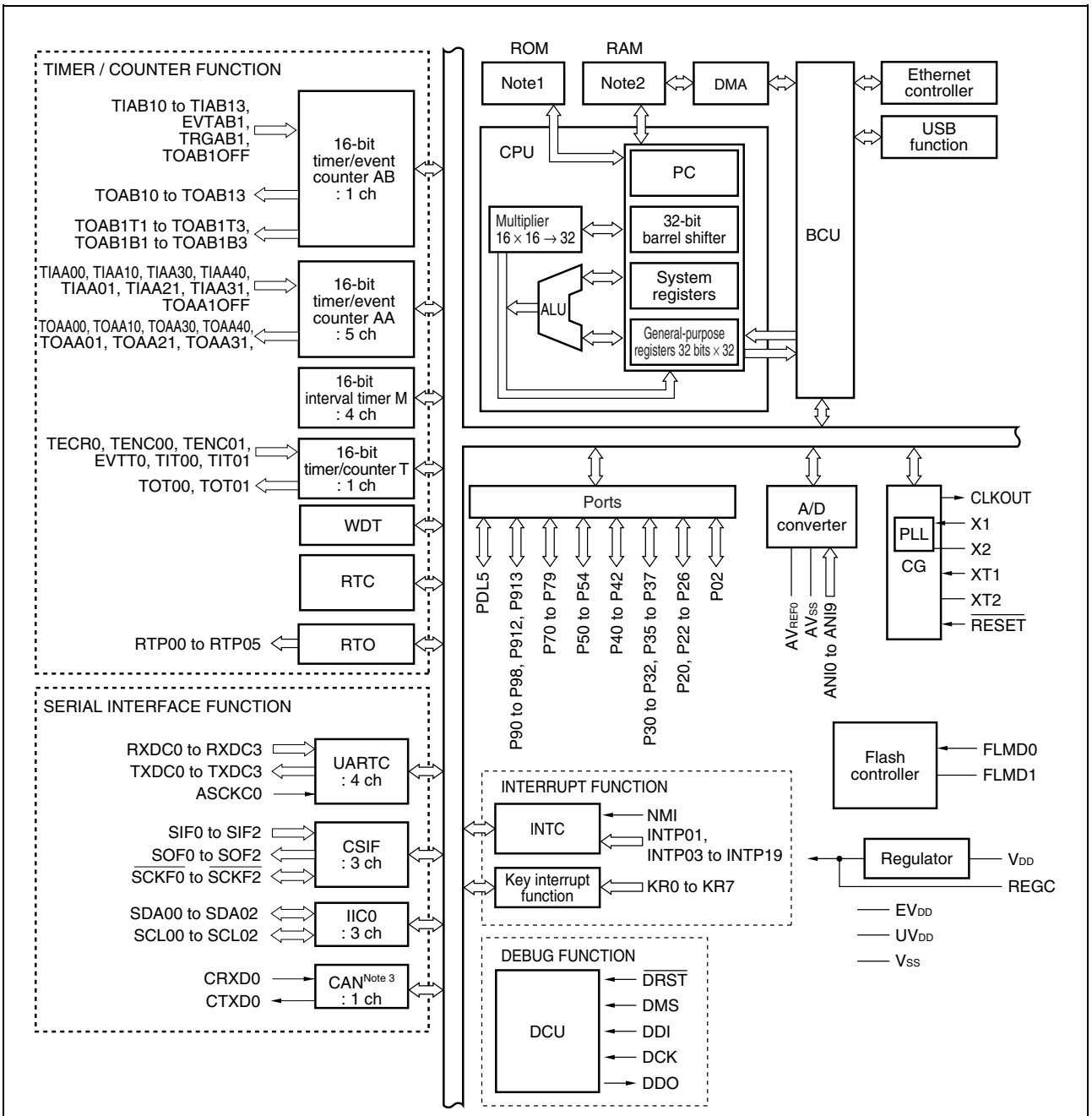


Notes 1. μPD70F3826: 64 KB
μPD70F3827: 128 KB
μPD70F3828, 70F3829: 256 KB

2. μPD70F3826: 32 KB (Including 16 KB of data RAM)
μPD70F3827: 48 KB (Including 16 KB of data RAM)
μPD70F3828, 70F3829: 64 KB (Including 16 KB of data RAM)

3. μPD70F3829 only.

- **V850ES/JF3-E**

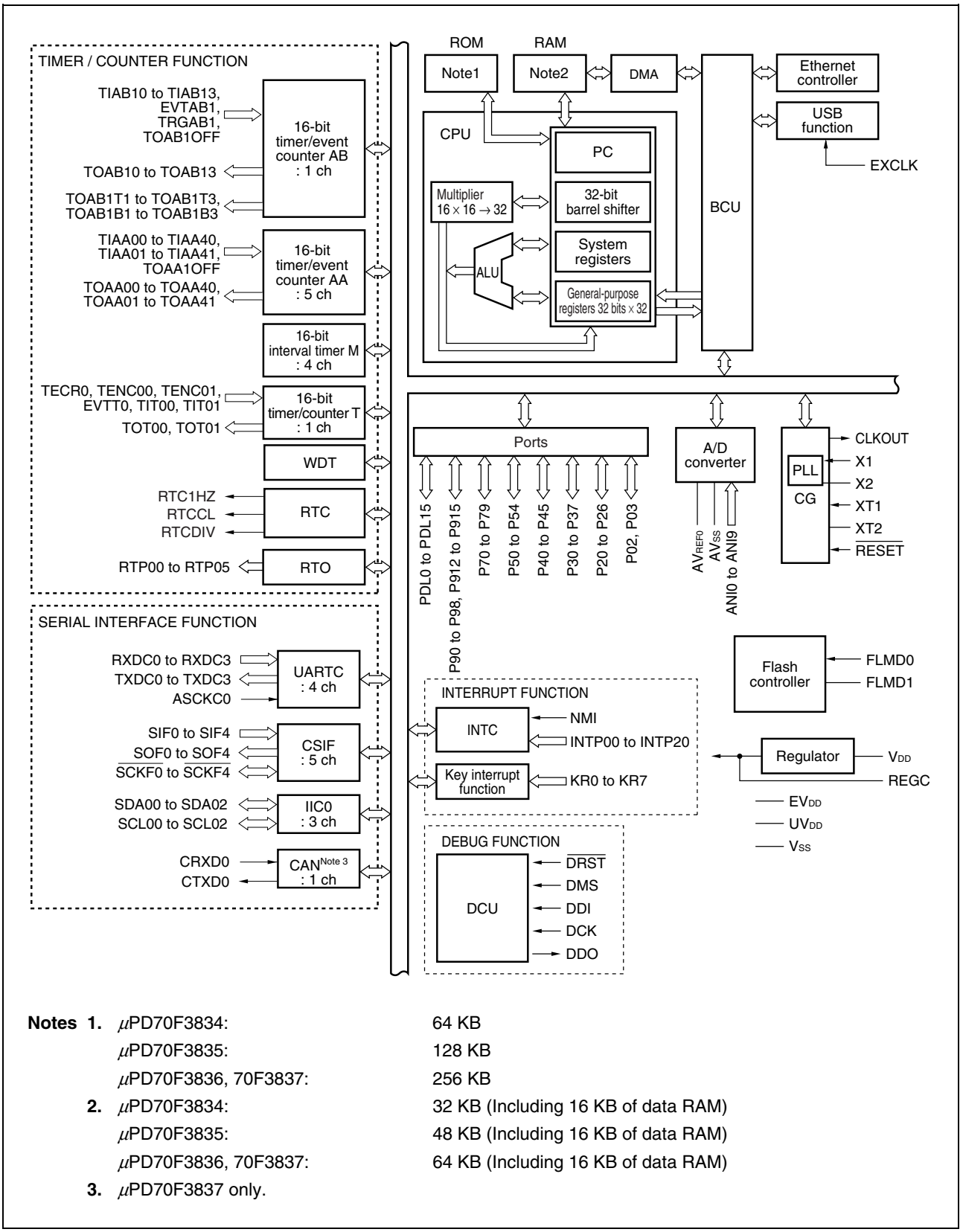


Notes 1. μPD70F3830: 64 KB
μPD70F3831: 128 KB
μPD70F3832, 70F3833: 256 KB

2. μPD70F3830: 32 KB (Including 16 KB of data RAM)
μPD70F3831: 48 KB (Including 16 KB of data RAM)
μPD70F3832, 70F3833: 64 KB (Including 16 KB of data RAM)

3. μPD70F3833 only.

- **V850ES/JG3-E**



Notes 1. μPD70F3834: 64 KB
μPD70F3835: 128 KB
μPD70F3836, 70F3837: 256 KB

2. μPD70F3834: 32 KB (Including 16 KB of data RAM)
μPD70F3835: 48 KB (Including 16 KB of data RAM)
μPD70F3836, 70F3837: 64 KB (Including 16 KB of data RAM)

3. μPD70F3837 only.

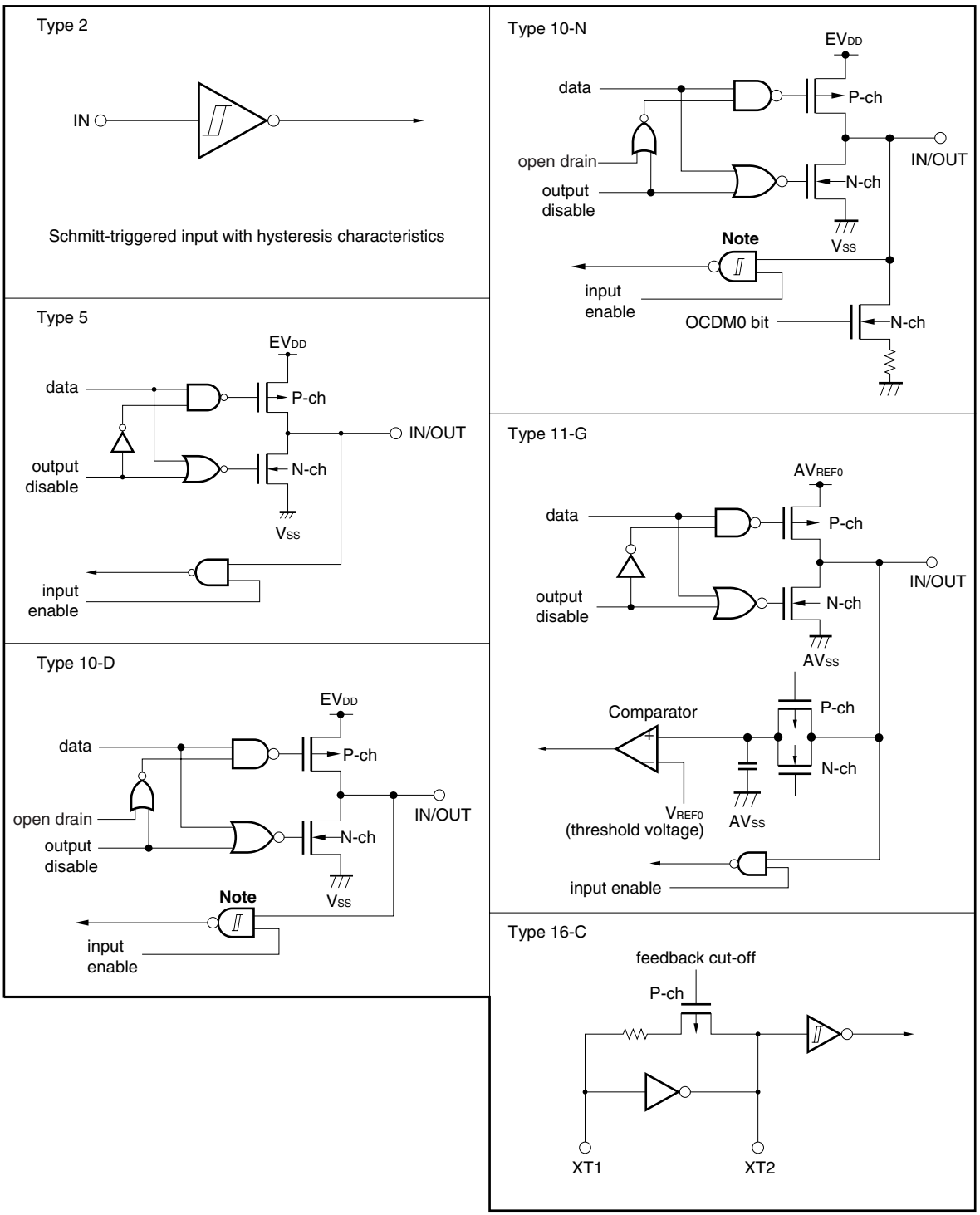
CONTENTS

Table 1-1. Types of Pin I/O Circuits (2/3)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JE3-E	JF3-E	JG3-E
P90	TOAB1T1/TOAB11/TIAB11/KR0 /INTP12	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	–	57	72
P91	TOAB1B1/TIAB10/KR1/TOAB10			–	58	73
P92	TOAB1T2/TOAB12/TIAB12/KR2 /INTP13			–	59	74
P93	TOAB1B2/TRGAB1/KR3/INTP14			–	60	75
P94	TOAB1T3/TOAB13/TIAB13/KR4 /INTP15			–	61	76
P95	TOAB1B3/EVTB1/KR5/INTP16			–	62	77
P96	TECR0/TIT00/KR6/TOT00			–	31	40
P97	TENC00/TIT01/KR7/TOT01			–	32	41
P98	TENC01/INTP17			–	33	42
P912	TOAB1OFF/INTP18			–	63	78
P913	SIF3/INTP19			–	–	30
	INTP19			–	25	–
P914	SOF3/INTP20			–	–	31
P915	$\overline{SCKF3}$			–	–	32
PDL0 to PDL4	–	5	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	–	–	58 to 67
PDL5	FLMD1	5		49	64	79
PDL6 to PDL10	–	5		–	–	83,84, 33,34, 43
AV_{REF0}	–	–	Directly connect to V_{DD} and always supply power.	1	1	1
AV_{SS}	–	–	Directly connect to V_{SS}.	2	2	2
EV_{DD}	–	–	Directly connect to V_{DD} and always supply power.	24, 44	29, 52	38, 65
FLMD0	–	–	Connect to V_{SS} in other than flash mode.	42	50	63
P1COL	–	5	Independently connect to EV_{DD} or V_{SS} via a resistor.	46	54	69
P1CRS	–	5		45	53	68
P1MDIO	–	5		47	55	70
P1RXCLK	–	5		48	56	71
P1RXD0	–	5		39	47	57
P1RXD1	–	5		33	41	51
P1RXD2	–	5		34	42	52
P1RXD3	–	5		35	43	53
P1RXDV	–	5		36	44	54
P1RXER	–	5		37	45	55
P1TXCLK	–	5		38	46	56
P1MDC	–	5	Leave open.	32	40	50
P1TXD0	–	5		26	34	44
P1TXD1	–	5		27	35	45
P1TXD2	–	5		28	36	46
P1TXD3	–	5		29	37	47
P1TXEN	–	5		31	39	49
P1TXER	–	5		30	38	48

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Figure 1-1. Pin I/O Circuits



Note Hysteresis characteristics are not available in port mode.

5. CLOCK GENERATION FUNCTION

The clock generation function has the following features.

- Main clock oscillator
  - PLL mode (×8): f_X = 3 to 6.25 MHz (f_{XX} = 24 to 50 MHz)
  - Clock through mode: f_X = 3 to 6.25 MHz (f_{XX} = 3 to 6.25 MHz)
- Subclock oscillator
  - f_{XT} = 32.768 kHz
- Internal oscillator (f_R = 220 kHz)
  - Default clock of watchdog timer
  - Sampling clock for clock monitor function of the main clock oscillator
  - Can be used as the internal system clock after the main clock is stopped
- Internal system clock generation
  - 7 levels (f_{XX}, f_{XX}/2, f_{XX}/4, f_{XX}/8, f_{XX}/16, f_{XX}/32, f_{XT})
- Peripheral clock generation
- Clock output function

8. 16-BIT TIMER/EVENT COUNTER T (TMT)

The number of TAB of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	1 channel (TMT0[Note])	1 channel (TMT0)	1 channel (TMT0)
Number of timer output	-	2	2

Note Interval timer function only.

The TMT function has the following features.

- 16 bit timer/counter (TMT)
- Clock selection: 8 ways
- Capture/trigger input pins (TIT00, TIT01) : 2
- External event count input pin[Note 1] : 1
- Encoder input pin (TENC00, TENC01) : 2
- Encoder clear input pin (TECR0) : 1
- External trigger input pin[Note 1]: 1
- Timer/counter: 1
- Capture/compare registers: 2
- Capture/compare match interrupt request signals: 2
- Timer output pins (TOT00, TOT01) : 2

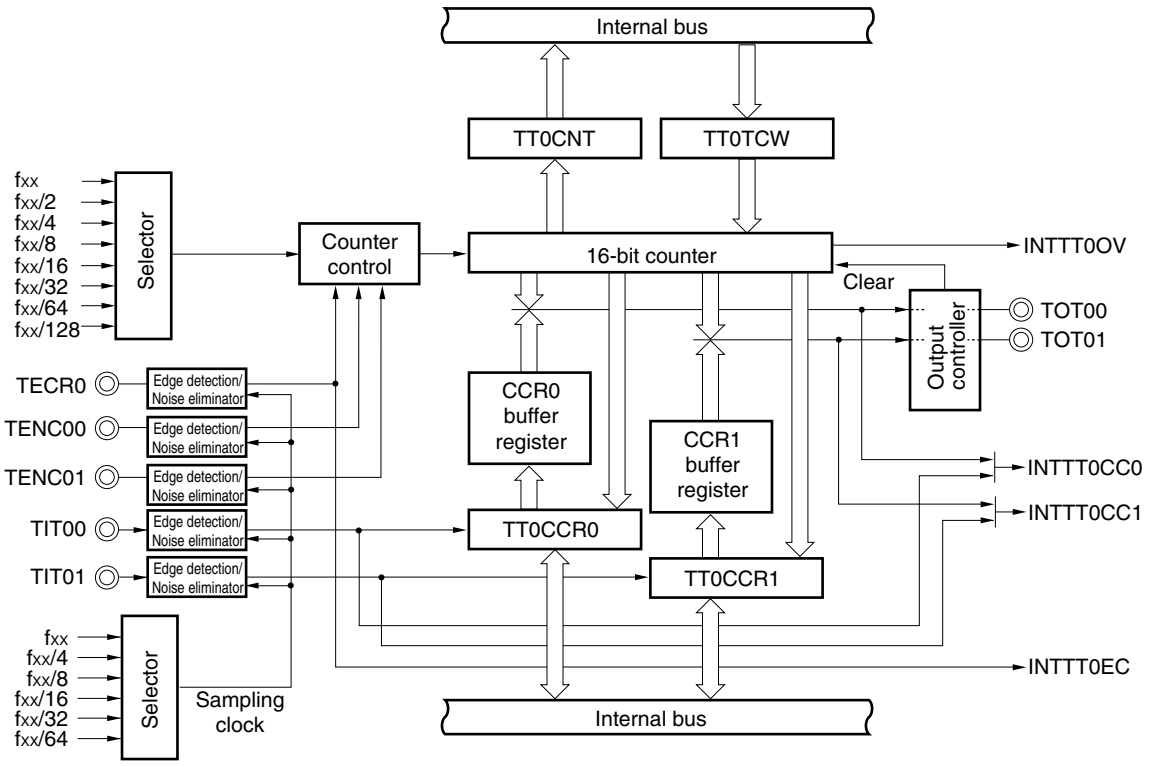
The TMT function has the following features[Note 2].

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Triangular wave PWM output
- Encoder count function

Notes1. The external trigger input pin and the external event count input pin also function as the encoder input pin (TENC00)

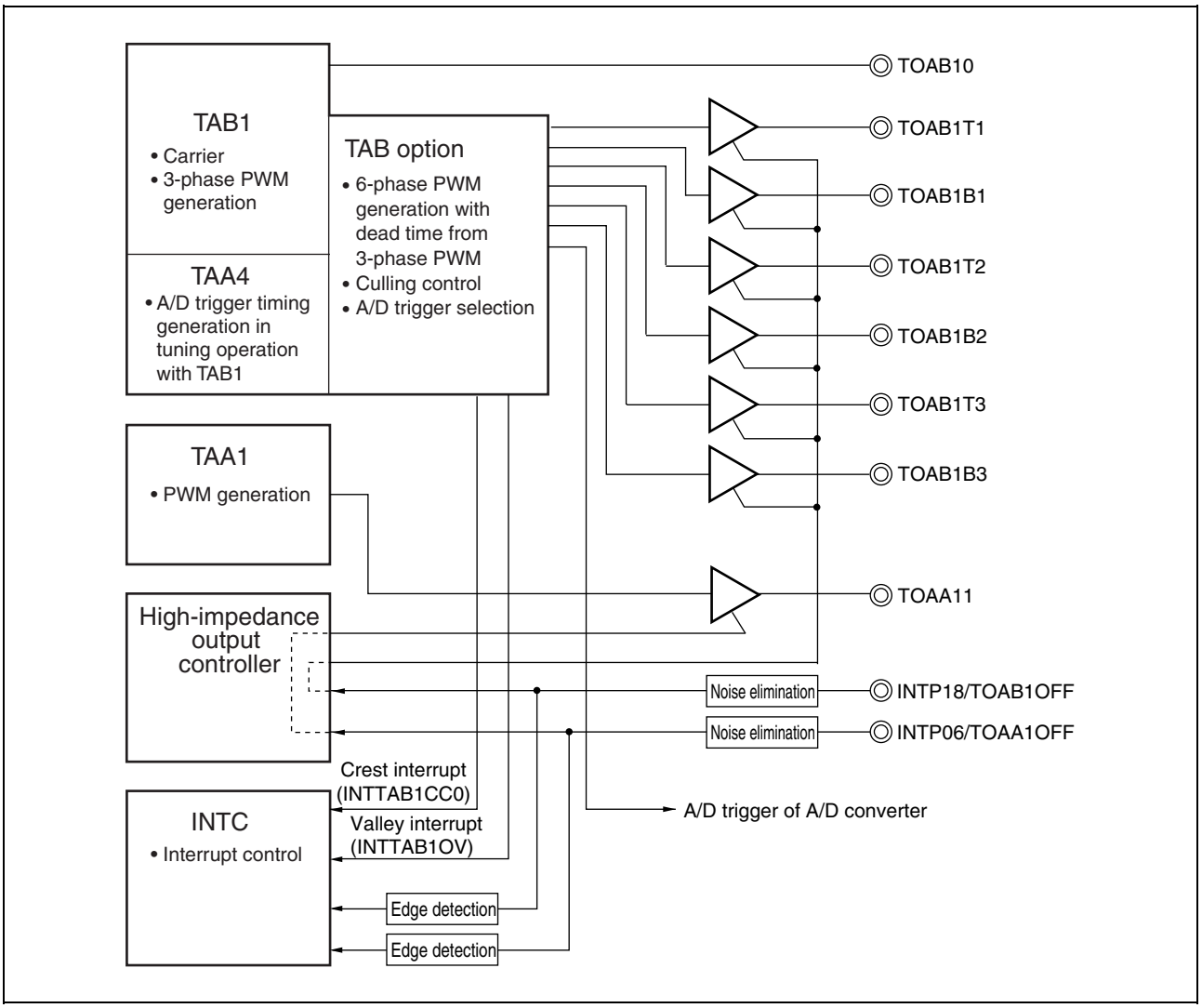
2. The TMT0 function of V850ES/JE3-E is only Interval timer.

The following figure shows the configuration of TMT.



Remark fxx: Main clock frequency

The following figure shows the configuration of motor control function.



11. REAL-TIME COUNTER

In the V850ES/Jx3-E, one channel of real-time counter is provided.

The real-time counter has the following features.

- It has counters for year, month, week, day, hours, minutes and seconds, and it can count up to 99 years.
- The year, month, week, day, hour, minute and second counters show the count in BCD code[Note 1].
- Alarm interrupt function
- Fixed-cycle interrupt function (cycle: 1 month to 0.5 seconds)
- Interval interrupt function (cycle: 1.95 to 125 ms)
- 1 Hz pin output
- 32.768 kHz pin output
- 512 Hz or 16.384 kHz pin output
- Watch error correction function
- Subclock operation or main clock operation[Note 2] selectable

Notes 1. BCD (binary-coded decimal) code is the code that represents each digit of a decimal number in 4-bit binary numerals.

2. The main clock can be divided into 32.768 kHz f_{BRG} with the baud rate generator dedicated to the real-time counter.

14. A/D CONVERTER

An A/D converter unit with ten channels is provided in the V850ES/Jx3-E.

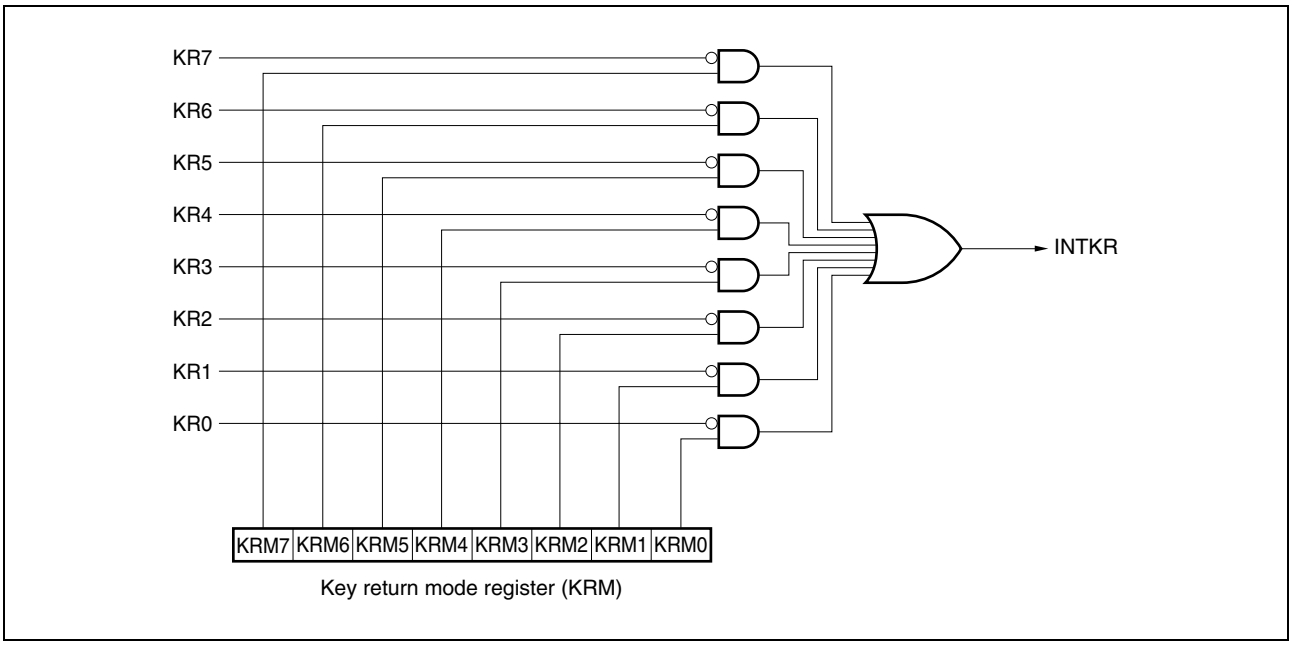
The A/D converter has the following features.

- 10-bit resolution
- 10 channels
- Successive approximation method
- Operating voltage: AV_{REF0} = 3.0 to 3.6 V
- Analog input voltage: 0 V to AV_{REF0}
- The following functions are provided as operation modes.
  - Continuous select mode
  - Continuous scan mode
  - One-shot select mode
  - One-shot scan mode
- The following functions are provided as trigger modes.
  - Software trigger mode
  - External trigger mode (external, 1)
  - Timer trigger mode
- Power-fail monitor function (conversion result compare function)

23. KEY INTERRUPT FUNCTION (V850ES/JF3-E, V850ES/JG3-E)

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins (KR0 to KR7).

The following figure shows the configuration of key interrupt.



26. CLOCK MONITOR, LOW-VOLTAGE DETECTOR

(1) Clock monitor

The clock monitor samples the main clock by using the internal oscillation clock (f_R) and generates a reset request signal when oscillation of the main clock is stopped.

(2) Low-voltage detector

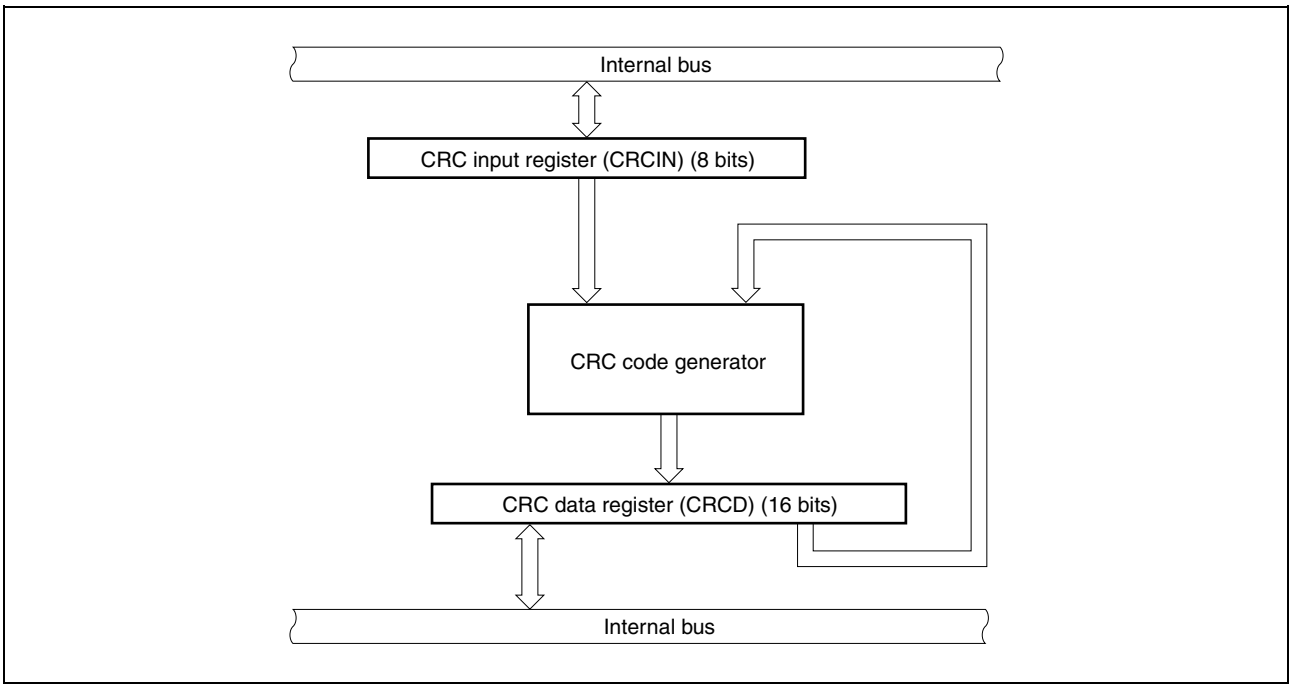
The low-voltage detector (LVI) has the following functions.

- Compares the supply voltage (V_{DD}) and detection voltage (V_{LVI}) and generates an interrupt request signal or internal reset signal when $V_{DD} < V_{LVI}$.
- An interrupt request signal or internal reset signal can be selected.
- Can operate in STOP mode.
- Operation can be stopped by software.

27. CRC FUNCTIONS

The outline of the CRC function is shown below.

- CRC operation circuit for detection of data block errors
- Generation of 16-bit CRC code using a CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) generation polynomial for blocks of data of any length in 8-bit units
- CRC code is set to the CRCD data register each time 1-byte data is transferred to the CRCIN register, after the initial value is set to the CRCD register.

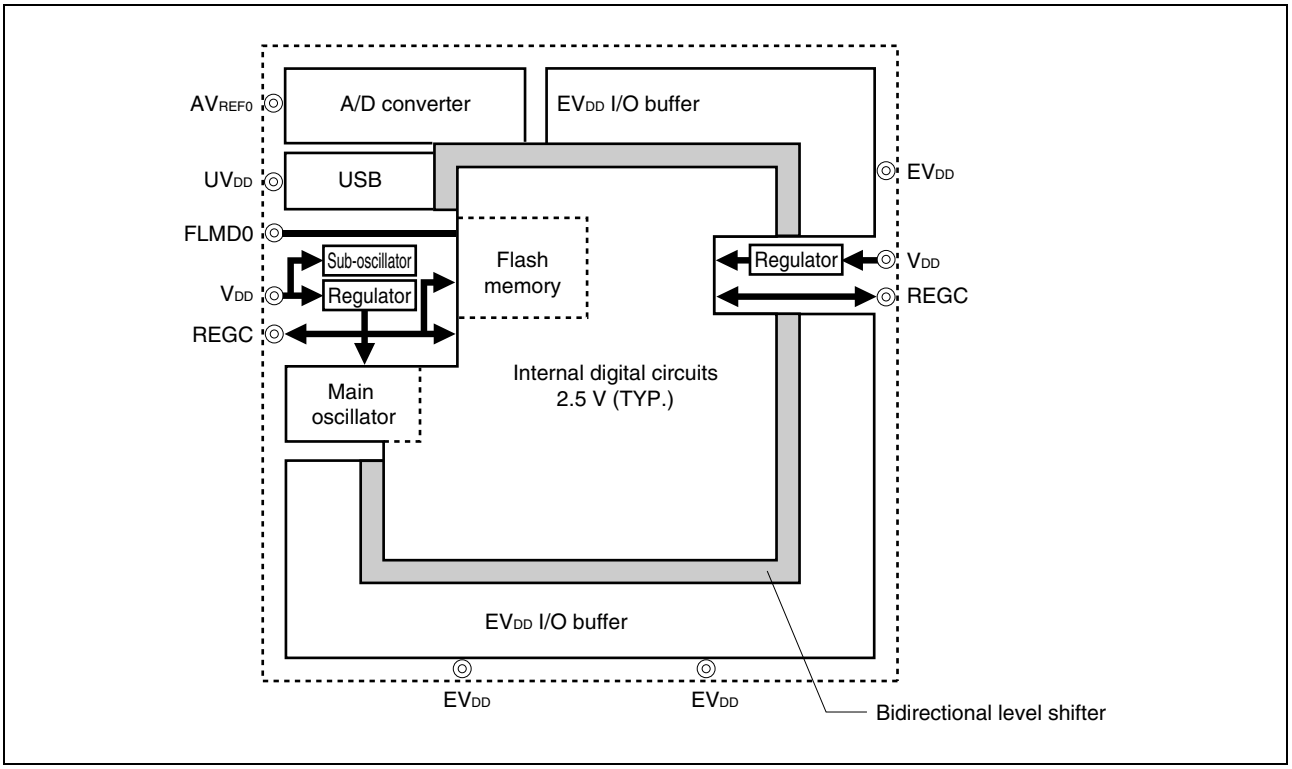


28. REGULATOR FUNCTION

The V850ES/Jx3-E includes a regulator to reduce power consumption and noise.

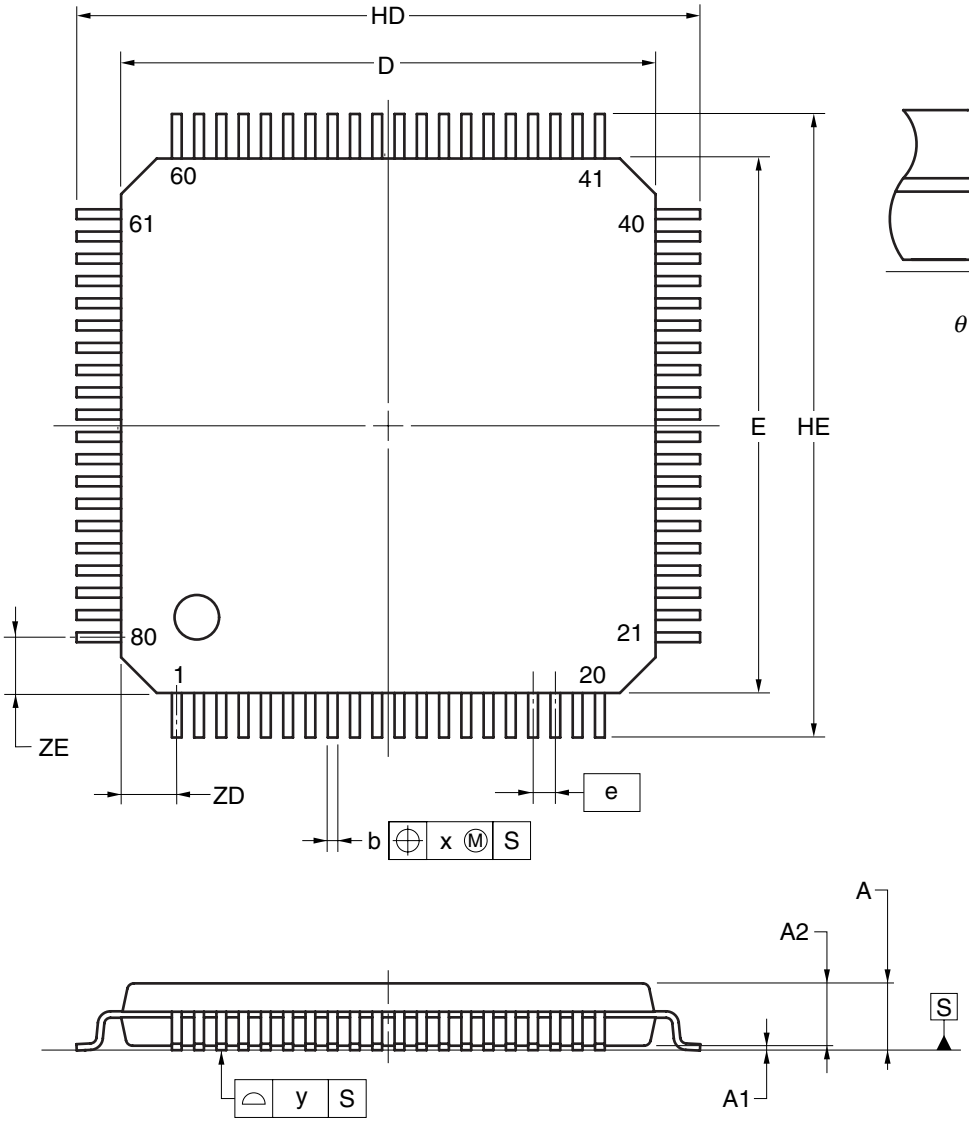
This regulator supplies a stepped-down V_{DD} power supply voltage to the oscillator block and internal logic circuits except the A/D converter and output buffers). The regulator output voltage is set to 2.5 V (TYP.).

The outline of the regulator functions is shown below.

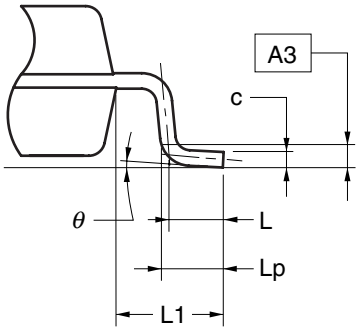


- V850ES/JF3-E

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P80GK-50-GAK

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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