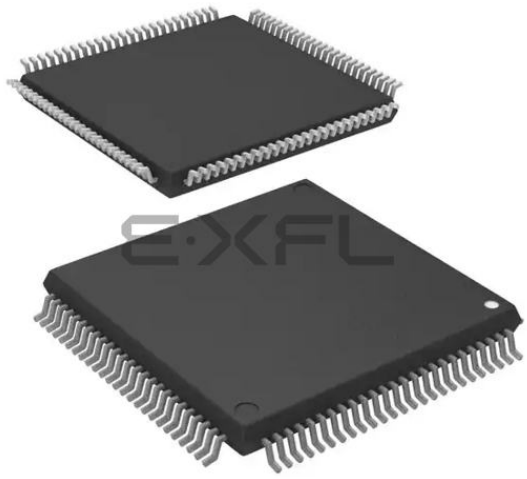

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	CANbus, CSI, Ethernet, I²C, UART/USART, USB
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	62
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.85V ~ 3.6V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3837gc-r-ueu-ax

Function list (V850ES/JE3-E)

Generic Name		V850ES/JE3-E			
Product Name		μPD70F3826	μPD70F3827	μPD70F3828	μPD70F3829
Internal memory	Flash memory	64 KB	128 KB	256 KB	256 KB
	Internal RAM	16 KB	32 KB	48 KB	48 KB
	Data RAM	16 KB	16 KB	16 KB	16 KB
Memory space		64 MB			
General-purpose register		32 bits × 32 registers			
Clocks	Main clock oscillation	PLL mode : f_X = 3 to 6.25 MHz, f_{XX} = 24 to 50 MHz (multiplication by 8) Clock through mode : f_X = 3 to 6.25 MHz (internal : f_{XX} = 3 to 6.25 MHz)			
	Subclock oscillation	f_{XT} = 32.768 kHz			
	Internal oscillation	f_R = 220 kHz (TYP.)			
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{XX}))			
I/O ports		I/O: 26 (5 V tolerant : 12)			
Timer	16-bit TAA	5 channels (among which two channels have the interval function only)			
	16-bit TAB	–			
	16-bit TMM	4 channels			
	16-bit TMT	1 channel (Interval function only)			
	Motor control	–			
	Watch timer	1 channel (RTC)			
	WDT	1 channel			
Real-time output function		6 bits × 1 channel			
10-bit A/D converter		10 channels			
Serial interface	CSIF/UARTC	1 channel			
	CSIF/UARTC/I²C	1 channel			
	CSIF	–			
	UARTC/I²C	1 channel			–
	UARTC/I²C/CAN	–			1 channel
USB function		1 channel			
Ethernet controller		1 channel			
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)			
Interrupt source	External Note 1, 2	7(7)	7(7)	7(7)	7(7)
	Internal	54	54	54	58
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes			
Reset factor		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)			
On-chip debugging		MINICUBE®, MINICUBE2 supported			
Operating supply voltage		2.85 to 3.6 V			
Operating ambient temperature		–40 to +85°C			
Package		64-pin plastic LQFP (fine pitch) (10 × 10 mm), 64-pin plastic WQFN (9 × 9 mm),			

Notes 1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.

2. Include NMI.

Function list (V850ES/JG3-E)

Generic Name		V850ES/JG3-E			
Product Name		μPD70F3834	μPD70F3835	μPD70F3836	μPD70F3837
Internal memory	Flash memory	64 KB	128 KB	256 KB	256 KB
	Internal RAM	16 KB	32 KB	48 KB	48 KB
	Data RAM	16 KB	16 KB	16 KB	16 KB
Memory space		64 MB			
General-purpose register		32 bits × 32 registers			
Clocks	Main clock oscillation	PLL mode : f_X = 3 to 6.25 MHz, f_{XX} = 24 to 50 MHz (multiplication by 8) Clock through mode : f_X = 3 to 6.25 MHz (internal : f_{XX} = 3 to 6.25 MHz)			
	Subclock oscillation	f_{XT} = 32.768 kHz			
	Internal oscillation	f_R = 220 kHz (TYP.)			
	Minimum instruction execution time	20 ns (@ 50 MHz operation with main system clock (f_{XX}))			
I/O ports		I/O: 62 (5 V tolerant : 35)			
Timer	16-bit TAA	5 channels			
	16-bit TAB	1 channel			
	16-bit TMM	4 channels			
	16-bit TMT	1 channel			
	Motor control	1 channel			
	Watch timer	1 channel (RTC)			
	WDT	1 channel			
Real-time output function		6 bits × 1 channel			
10-bit A/D converter		10 channels			
Serial interface	CSIF/UARTC	1 channel			
	CSIF/UARTC/I²C	2 channels			
	CSIF	2 channels			
	UARTC/I²C	1 channel			–
	UARTC/I²C/CAN	–			1 channel
USB function		1 channel			
Ethernet controller		1 channel			
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)			
Interrupt source	External Note 1, 2	22(22)	22(22)	22(22)	22(22)
	Internal	61	61	61	65
Power-save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE modes			
Reset factor		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)			
On-chip debugging		MINICUBE, MINICUBE2 supported			
Operating supply voltage		2.85 to 3.6 V			
Operating ambient temperature		–40 to +85°C			
Package		100-pin plastic LQFP (fine pitch) (14 × 14 mm), 113-pin plastic FBGA Note3			

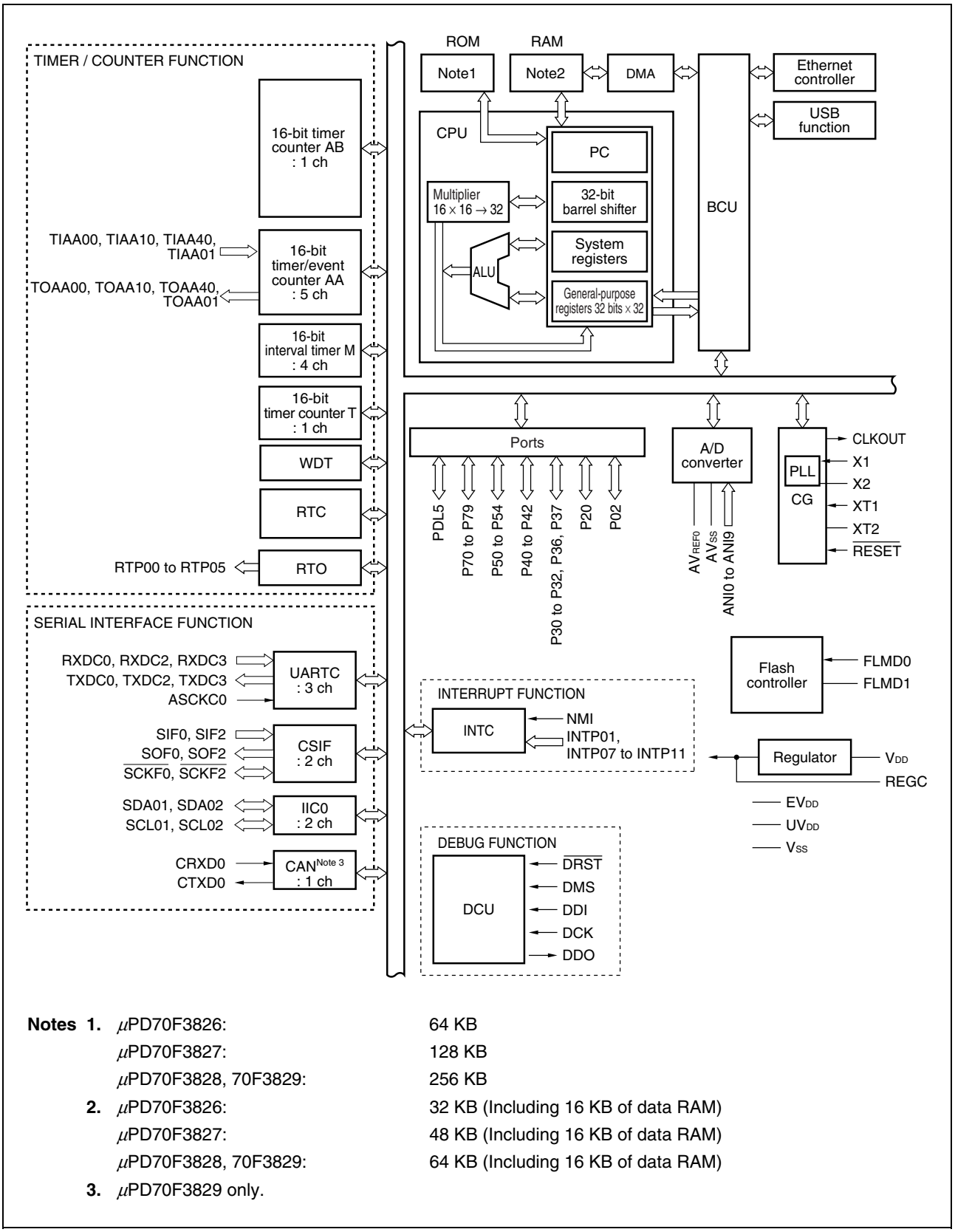
Notes 1. The figure in parentheses indicates the number of external interrupts that can release the STOP mode.

2. Include NMI.

3. Under planning.

INTERNAL BLOCK DIAGRAM

- **V850ES/JE3-E**



Notes 1. μPD70F3826: 64 KB
μPD70F3827: 128 KB
μPD70F3828, 70F3829: 256 KB

2. μPD70F3826: 32 KB (Including 16 KB of data RAM)
μPD70F3827: 48 KB (Including 16 KB of data RAM)
μPD70F3828, 70F3829: 64 KB (Including 16 KB of data RAM)

3. μPD70F3829 only.

(3/5)

Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
REGC	–	Connecting capacitor for regulator output stabilization (4.7 μF (preliminary value))	–	6, 41	6, 49	9, 62
$\overline{\text{RESET}}$	Input	System reset input	–	10	10	13
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	P22/INTP02	–	–	7
RTCCL	Output	Real-time counter clock (original 32 kHz clock) output	P21/RTCDIV	–	–	6
RTCDIV	Output	Real-time counter clock (divided 32 kHz clock) output	P21/RTCCL	–	–	6
RTP00	Output	Real-time output port	P40/SIF0/TXDC3/SDA01	52	68	85
RTP01		RTP00, RTP01 are N-ch open-drain output selectable.	P41/SOF0/RXDC3/SCL01	53	69	86
RTP02			P42/$\overline{\text{SCKF0}}$/TIAA40/TOAA40	54	70	87
RTP03			P43	–	–	88
RTP04			P44	–	–	89
RTP05			P45TIAA41/TOAA41	–	–	90
RXDC0	Input	Serial receive data input (UARTC0 to UARTC3)	P31/SOF2/TIAA01/TOAA01	14	18	21
RXDC1			P24/SOF1/SDL00/INTP04	–	14	17
RXDC2			P37/SCL02/CRXD0[Note]	51	67	82
RXDC3			P41/SOF0/SCL01/RTP01	53	69	86
$\overline{\text{SCKF0}}$	I/O	Serial clock I/O (CSIF0 to CSIF4)	P42/TIAA40/TOAA40/RTP02	54	70	87
$\overline{\text{SCKF1}}$			P25/TIAA30/TOAA30	–	15	18
$\overline{\text{SCKF2}}$			P32/ASCKC0/TIAA10/TOAA10	15	19	22
$\overline{\text{SCKF3}}$			P915	–	–	32
$\overline{\text{SCKF4}}$			P35/TIAA21/TOAA21/TOAA1OFF /INTP06	–	–	80
SCL00	I/O	Serial clock I/O (I^2C00 to I^2C02)	P24/SOF1/RXDC1/INTP04	–	14	17
SCL01		N-ch open-drain output selectable.	P41/SOF0/RXDC3/RTP01	53	69	86
SCL02			P37/RXDC2/CRXD0[Note]	51	67	82
SDA00	I/O	Serial transmit/receive data I/O (I^2C00 to I^2C02)	P23/SIF1/TXDC1/INTP03	–	13	16
SDA01		N-ch open-drain output selectable.	P40/SIF0/TXDC3/RTP00	52	68	85
SDA02			P36/TXDC2/CTXD0[Note]	50	66	81
SIF0	Input	Serial receive data input (CSIF0 to CSIF4)	P40/TXDC3/SDA01/RTP00	52	68	85
SIF1			P23/TXDC1/SDA00/INTP03	–	13	16
SIF2			P30/TXDC0/TIAA00/TOAA00	13	17	20
SIF3			P913/INTP19	–	–	30
SIF4			P33/TIAA11/TOAA11	–	–	23
SOF0	Output	Serial transmit data output (CSIF0 to CSIF4)	P41/RXDC3/SCL01/RTP01	53	69	86
SOF1		N-ch open-drain output selectable.	P24/RXDC1/SDL00/INTP04	–	14	17
SOF2			P31/RXDC0/TIAA01/TOAA01	14	18	21
SOF3			P914/INTP20	–	–	31
SOF4			P34/TIAA20/TOAA20	–	–	24
TECR0	Input	Encoder clear input of TMT0	P96/TIT00/KR6/TOT00	–	31	40
TENC00		Encoder input/external event input/external trigger input of TMT0	P97/TIT01/KR7/TOT01	–	32	41
TENC01		Encoder input of TMT0	P98/INTP17	–	33	42

Note Available only in on-chip CAN controller products

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

(5/5)

Pin Name	I/O	Function	Alternate Function	Pin number		
				JE3-E	JF3-E	JG3-E
TOAB1B1	Output	Pulse signal output for 6-phase PWM low arm of TAB1	P91/TIAB10/KR1/TOAB10	–	58	73
TOAB1B2			P93/TRGAB1/KR3/INTP14	–	60	75
TOAB1B3			P95/EVTAB1/KR5/INTP16	–	62	77
TOAB1OFF	Input	TAB1 High-impedance output control signal input	P912/INTP18	–	63	78
TOAB1T1	Output	Pulse signal output for 6-phase PWM high arm of TAB1. N-ch open-drain output selectable.	P90/TOAB11/TIAB11/KR0/INTP12	–	57	72
TOAB1T2			P92/TOAB12/TIAB12/KR2/INTP13	–	59	74
TOAB1T3			P94/TOAB13/TIAB13/KR4/INTP15	–	61	76
TOT00	Output	Timer output of TMT0 N-ch open-drain output selectable	P96/TECR0/TIT00/KR6	–	31	40
TOT01			P97/TENC00/TIT01/KR7	–	32	41
TRGAB1	Input	External trigger input of TAB1 N-ch open-drain output selectable	P93/TOAB1B2/KR3/INTP14	–	60	75
TXDC0	Output	Serial transmit data output (UARTC0 to UARTC3) N-ch open-drain output selectable.	P30/SIF2/TIAA00/TOAA00	13	17	20
TXDC1			P23/SIF1/SDA00/INTP03	–	13	16
TXDC2			P36/SDA02/CTXD0[Note]	50	66	81
TXDC3			P40/SIF0/SDA01/RTP00	52	68	85
UDMF	I/O	USB data I/O (–) function	–	21	26	35
UDPF		USB data I/O (+) function	–	22	27	36
UV_{DD}	–	3.3 V positive power supply for USB	–	23	28	37
V_{DD}	–	Positive power supply for internal circuit	–	5	5	8
V_{SS}	–	Ground potential for internal circuit	–	7	7	10
X1	Input	Connecting resonator for main clock	–	8	8	11
X2	–		–	9	9	12
XT1	Input	Connecting resonator for subclock	–	8	11	14
XT2	–		–	9	12	15

Note Available only in on-chip CAN controller products.

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Table 1-1. Types of Pin I/O Circuits (2/3)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JE3-E	JF3-E	JG3-E
P90	TOAB1T1/TOAB11/TIAB11/KR0 /INTP12	10-D	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	–	57	72
P91	TOAB1B1/TIAB10/KR1/TOAB10			–	58	73
P92	TOAB1T2/TOAB12/TIAB12/KR2 /INTP13			–	59	74
P93	TOAB1B2/TRGAB1/KR3/INTP14			–	60	75
P94	TOAB1T3/TOAB13/TIAB13/KR4 /INTP15			–	61	76
P95	TOAB1B3/EVTB1/KR5/INTP16			–	62	77
P96	TECR0/TIT00/KR6/TOT00			–	31	40
P97	TENC00/TIT01/KR7/TOT01			–	32	41
P98	TENC01/INTP17			–	33	42
P912	TOAB1OFF/INTP18			–	63	78
P913	SIF3/INTP19			–	–	30
	INTP19			–	25	–
P914	SOF3/INTP20			–	–	31
P915	$\overline{SCKF3}$			–	–	32
PDL0 to PDL4	–	5	Input: Independently connect to EV_{DD} or V_{SS} via a resistor. Output: Leave open.	–	–	58 to 67
PDL5	FLMD1	5		49	64	79
PDL6 to PDL10	–	5		–	–	83,84, 33,34, 43
AV_{REF0}	–	–	Directly connect to V_{DD} and always supply power.	1	1	1
AV_{SS}	–	–	Directly connect to V_{SS}.	2	2	2
EV_{DD}	–	–	Directly connect to V_{DD} and always supply power.	24, 44	29, 52	38, 65
FLMD0	–	–	Connect to V_{SS} in other than flash mode.	42	50	63
P1COL	–	5	Independently connect to EV_{DD} or V_{SS} via a resistor.	46	54	69
P1CRS	–	5		45	53	68
P1MDIO	–	5		47	55	70
P1RXCLK	–	5		48	56	71
P1RXD0	–	5		39	47	57
P1RXD1	–	5		33	41	51
P1RXD2	–	5		34	42	52
P1RXD3	–	5		35	43	53
P1RXDV	–	5		36	44	54
P1RXER	–	5		37	45	55
P1TXCLK	–	5		38	46	56
P1MDC	–	5	Leave open.	32	40	50
P1TXD0	–	5		26	34	44
P1TXD1	–	5		27	35	45
P1TXD2	–	5		28	36	46
P1TXD3	–	5		29	37	47
P1TXEN	–	5		31	39	49
P1TXER	–	5		30	38	48

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

Table 1-1. Types of Pin I/O Circuits (3/3)

Pin Name	Alternate Function	I/O Circuit Type	Recommended Connection of Unused Pins	JE3-E	JF3-E	JG3-E
REGC	–	–	Connect to regulator output stabilization (4.7 μF (preliminary value)) capacitor.	6, 41	6, 49	9, 62
$\overline{\text{RESET}}$	–	2	–	10	10	13
UDMF	–	–	Leave open.	21	26	35
UDPF	–	–	Leave open.	22	27	36
UV_{DD}	–	–	Directly connect to V_{DD} and always supply power.	23	28	37
V_{DD}	–	–	–	5	5	8
V_{SS}	–	–	–	7	7	10
X1	–	–	–	8	8	11
X2	–	–	–	9	9	12
XT1	–	16-C	Connect to V_{SS} via a resistor.	8	11	14
XT2	–	16-C	Leave open.	9	12	15

Remark JE3-E: V850ES/JE3-E, JF3-E: V850ES/JF3-E, JG3-E: V850ES/JG3-E

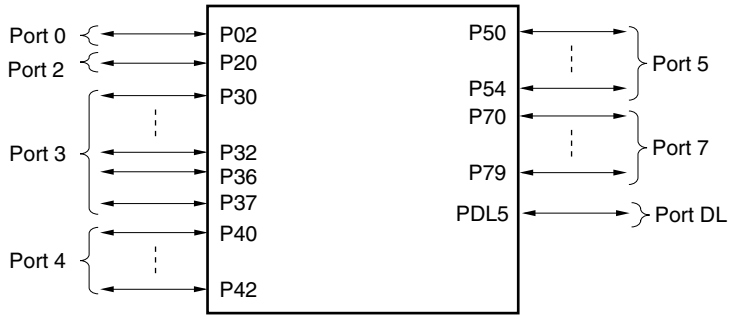
4. PORTS

The number of I/O ports of the V850ES/Jx3-E is shown below.

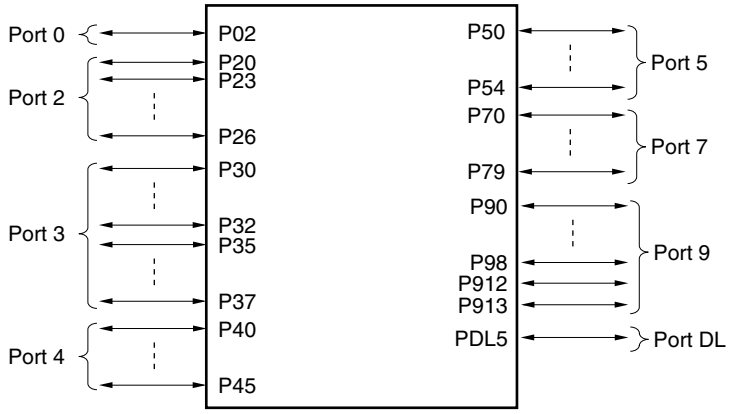
Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of ports (5 V tolerant)	26 (12)	42 (28)	62 (35)

The following figure shows the basic configurations of ports.

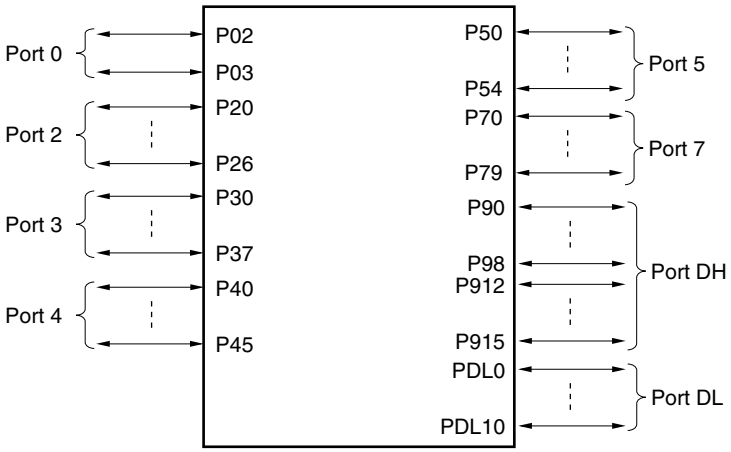
(a) V850ES/JE3-E



(b) V850ES/JF3-E



(c) V850ES/JG3-E



5. CLOCK GENERATION FUNCTION

The clock generation function has the following features.

- Main clock oscillator
  - PLL mode (×8): f_X = 3 to 6.25 MHz (f_{XX} = 24 to 50 MHz)
  - Clock through mode: f_X = 3 to 6.25 MHz (f_{XX} = 3 to 6.25 MHz)
- Subclock oscillator
  - f_{XT} = 32.768 kHz
- Internal oscillator (f_R = 220 kHz)
  - Default clock of watchdog timer
  - Sampling clock for clock monitor function of the main clock oscillator
  - Can be used as the internal system clock after the main clock is stopped
- Internal system clock generation
  - 7 levels (f_{XX}, f_{XX}/2, f_{XX}/4, f_{XX}/8, f_{XX}/16, f_{XX}/32, f_{XT})
- Peripheral clock generation
- Clock output function

6. 16-BIT TIMER/EVENT COUNTER AA (TAA)

The number of TAA of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	5 channels (TAA0 to TAA4[Note])	5 channels (TAA0 to TAA4)	5 channels (TAA0 to TAA4)
Number of timer output	4	7	10

Note TAA2 and TAA3 have Interval timer function only.

The timer/counter function has the following features.

- 16 bit timer/counter (TAAn)
- Clock selection: 8 ways
- Capture/trigger input pins (TIAA n0, TIAAn1): 2
- External event count input pin[Note]: 1
- External trigger input pin[Note]: 1
- Timer/counter: 1
- Capture/compare registers: 2
  (32-bit capture function available by using a cascade connection with timer AA.)
- Capture/compare match interrupt request signals: 2
- Timer output pins (TOAAn0, TOAAn1): 2

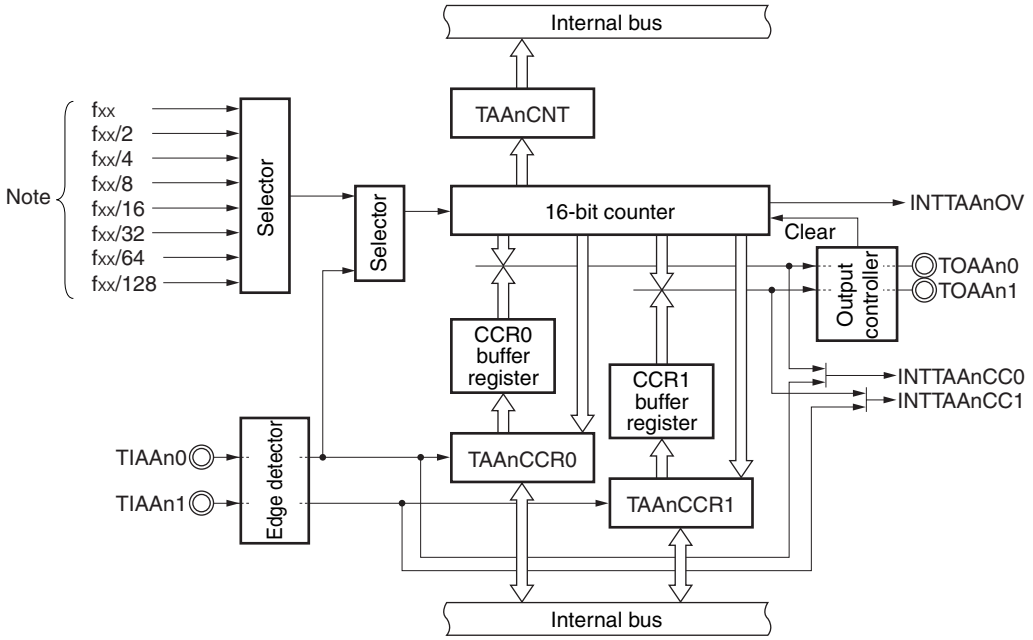
The TAAn function has the following features.

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Timer tuning function
- Simultaneous start function

Note The external event count input pin and external trigger input pin also function as the capture trigger input pin (TIAAn0).

Remark n = 0 to 4

The following figure shows the configuration of TAA.



Note fxx/2, fxx/4, fxx/8, fxx/16, fxx/64, fxx/256, fxx/512, fxx/1024 for TAA2, TAA3

Remark fxx = Main clock frequency

n = 0 to 4

7. 16-BIT TIMER/EVENT COUNTER AB (TAB)

The number of TAB of the V850ES/Jx3-E is shown below.

Product Name	V850ES/JF3-E	V850ES/JF-E	V850ES/JG3-E
Number of channel	1 channel (TAB1[Note])	1 channel (TAB1)	1 channel (TAB1)
Number of timer output	-	4	4

Note Interval timer function only.

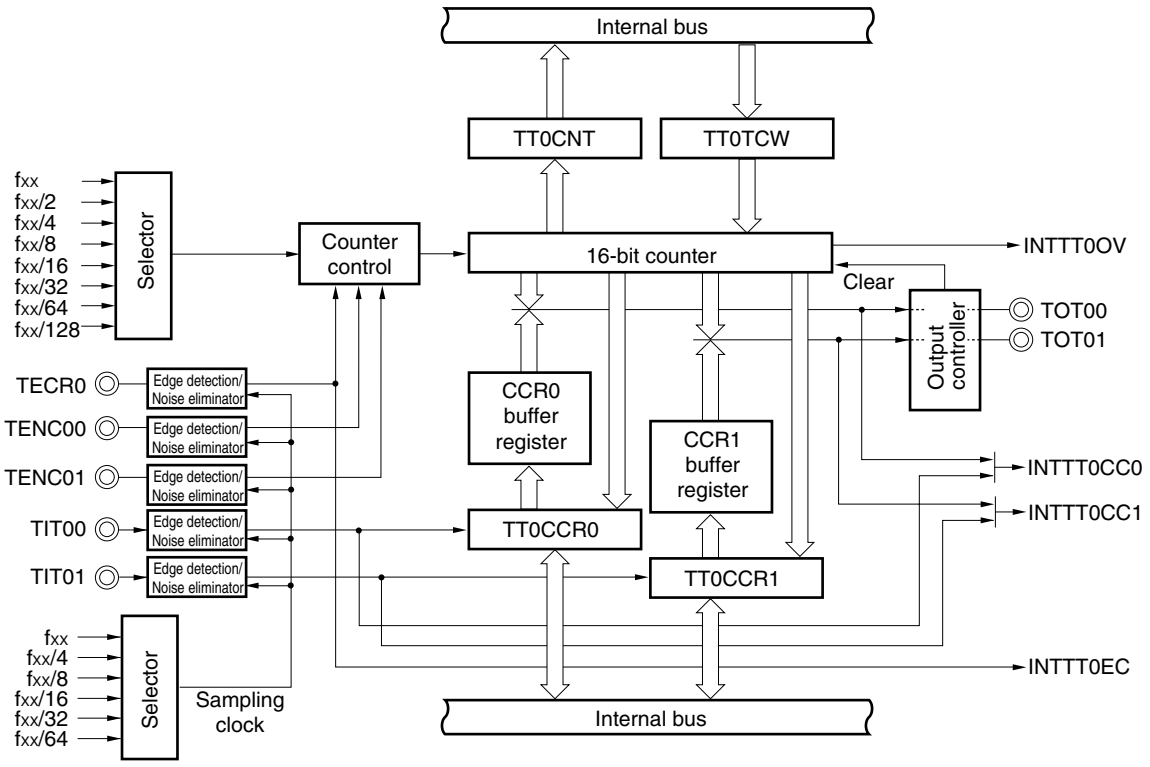
The TAB function has the following features.

- 16-bit timer/counter (TAB1)
- Clock selection: 8 ways
- Capture/trigger input pins (TIAB10 to TIAB13): 4
- External event count input pin (EVTAB1): 1
- External trigger input pin (TRGAB1): 1
- Timer/counter: 1
- Capture/compare registers: 4
- Capture/compare match interrupt request signals: 4
- Timer output pins (TOAB10 to TOAB13): 4

The TAB1 function has the following features.

- Interval timer
- External event counter
- External trigger pulse output
- One-shot pulse output
- PWM output
- Free-running timer
- Pulse width measurement
- Triangular wave PWM output
- Timer tuning function

The following figure shows the configuration of TMT.



Remark fxx: Main clock frequency

10. MOTOR CONTROL FUNCTION

In the V850ES/JF3-E and V850ES/JG3-E, one channel of motor control function is provided.

Timer AB1 (TAB) and the TAB option (TABOP) can be used as an inverter function that controls a motor.

It performs a tuning operation with timer AA4 (TAA4) and A/D conversion of the A/D converter can be started when the value of TAB matches the value of TAA4. The following operations can be performed as motor control functions.

- 6-phase PWM output function with 16-bit resolution (with dead-timer, for upper and lower arms)
- Timer tuning operation function (tunable with TAA4)
- Cycle setting function (cycle can be changed during operation of crest or valley interrupt)
- Compare register rewriting: Anytime rewrite, batch rewrite, or intermittent rewrite
  (selectable during TAB operation)
- Interrupt and transfer culling functions
- Dead-time setting function
- A/D trigger timing function of the A/D converter (four types of timing can be generated)
- 0% output and 100% output available
- 0% output and 100% output selectable by crest interrupt and valley interrupt
- Forced output stop function
  - At valid edge detection by external pin input (INTP06/TOAA1OFF, INTP18/TOAB1OFF)
  - When stoppage of the main clock oscillation is detected by clock monitor function

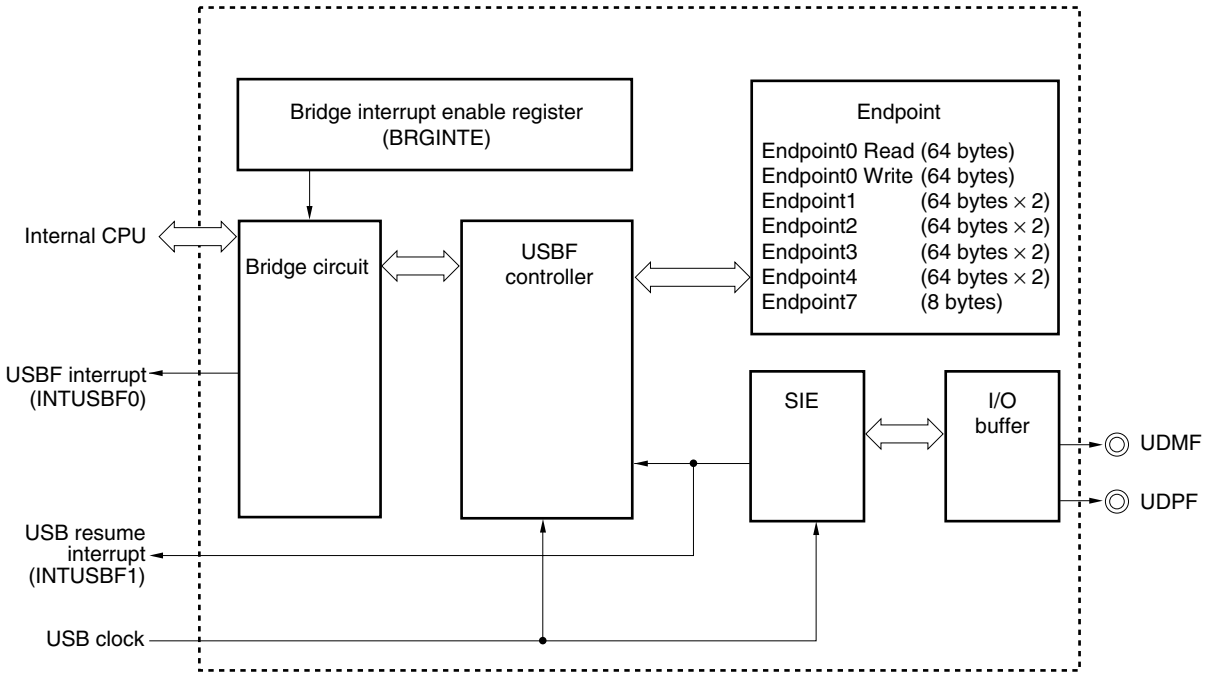
19. USB FUNCTION CONTROLLER (USBF)

In the V850ES/Jx3-E, one channel of USBF is provided.

- Conforms to the Universal Serial Bus (USB) Specification.
- USB 2.0-compatible full-speed transfer (12 Mbps) supported
- Endpoint for transfer incorporated

Endpoint Name	FIFO Size (Bytes)	Transfer Type	Remark
Endpoint0 Read	64	Control transfer	–
Endpoint0 Write	64	Control transfer	–
Endpoint1	64 × 2	Bulk 1 transfer (IN)	2-buffer configuration
Endpoint2	64 × 2	Bulk 1 transfer (OUT)	2-buffer configuration
Endpoint3	64 × 2	Bulk 2 transfer (IN)	2-buffer configuration
Endpoint4	64 × 2	Bulk 2 transfer (OUT)	2-buffer configuration
Endpoint7	8	Interrupt transfer (IN)	–

The following figure shows the configuration of USB function controller.



Remark Area enclosed with dashed line: Functions included in USB function controller

Table 22-1. Interrupt Source List (1/3)

Type	Classification	Default Priority	Name	Trigger	Generating Unit	Interrupt Control Register	JE3E	JF3E	JG3E
Reset	Interrupt	–	RESET	$\overline{\text{RESET}}$ pin input/reset input from internal source	RESET	–	√	√	√
Non-maskable	Interrupt	–	NMI	NMI pin valid edge input	Pin	–	√	√	√
		–	INTWDT2	WDT2 overflow	WDT2	–	√	√	√
Software exception	Exception	–	TRAP0n (n = 0-FH)	TRAP instruction	–	–	√	√	√
		–	TRAP1n (n = 0-FH)	TRAP instruction	–	–	√	√	√
Exception trap	Exception	–	ILGOP/DBG0	Illegal instruction code/DBTRAP instruction	–	–	√	√	√
Maskable	Interrupt	0	INTLVI	Detection of low voltage	POCLVI	LVIIC	√	√	√
		1	INTP00	Detection of external interrupt pin input edge (INTP00)	Pin	PIC0			√
		2	INTP01	Detection of external interrupt pin input edge (INTP01)	Pin	PIC1	√	√	√
		3	INTP02	Detection of external interrupt pin input edge (INTP02)	Pin	PIC2	–	–	√
		4	INTP03	Detection of external interrupt pin input edge (INTP03)	Pin	PIC3	–	√	√
		5	INTP04	Detection of external interrupt pin input edge (INTP04)	Pin	PIC4	–	√	√
		6	INTP05	Detection of external interrupt pin input edge (INTP05)	Pin	PIC5	–	√	√
		7	INTP06	Detection of external interrupt pin input edge (INTP06)	Pin	PIC6	–	√	√
		8	INTP07	Detection of external interrupt pin input edge (INTP07)	Pin	PIC7	√	√	√
		9	INTP08	Detection of external interrupt pin input edge (INTP08)	Pin	PIC8	√	√	√
		10	INTP09	Detection of external interrupt pin input edge (INTP09)	Pin	PIC9	√	√	√
		11	INTP10	Detection of external interrupt pin input edge (INTP10)	Pin	PIC10	√	√	√
		12	INTP11	Detection of external interrupt pin input edge (INTP11)	Pin	PIC11	√	√	√
		13	INTP12	Detection of external interrupt pin input edge (INTP12)	Pin	PIC12	–	√	√
		14	INTP13	Detection of external interrupt pin input edge (INTP13)	Pin	PIC13	–	√	√
		15	INTP14	Detection of external interrupt pin input edge (INTP14)	Pin	PIC14	–	√	√
		16	INTP15	Detection of external interrupt pin input edge (INTP15)	Pin	PIC15	–	√	√
		17	INTP16	Detection of external interrupt pin input edge (INTP16)	Pin	PIC16	–	√	√
		18	INTP17	Detection of external interrupt pin input edge (INTP17)	Pin	PIC17	–	√	√
		19	INTP18	Detection of external interrupt pin input edge (INTP18)	Pin	PIC18	–	√	√
		20	INTP19	Detection of external interrupt pin input edge (INTP19)	Pin	PIC19	–	√	√
		21	INTP20	Detection of external interrupt pin input edge (INTP20)	Pin	PIC20	–	–	√
		32	INTTAB1OV	TAB1 overflow	TAB1	TAB1OVIC	√	√	√
		33	INTTAB1CC0	TAB1 capture 0/compare 0 match	TAB1	TAB1CCIC0	√	√	√
		34	INTTAB1CC1	TAB1 capture 1/compare 1 match	TAB1	TAB1CCIC1	√	√	√
		35	INTTAB1CC2	TAB1 capture 2/compare 2 match	TAB1	TAB1CCIC2	√	√	√
		36	INTTAB1CC3	TAB1 capture 3/compare 3 match	TAB1	TAB1CCIC3	√	√	√
		37	INTTT0OV	TMT0 overflow	TMT0	TT0OVIC	√	√	√
		38	INTTT0CC0	TMT0 capture 0/compare 0 match	TMT0	TT0CCIC0	√	√	√
		39	INTTT0CC1	TMT0 capture 1/compare 1 match	TMT0	TT0CCIC1	√	√	√
		40	INTTT0EC	TMT0 encoder input	TMT0	TT0ECIC	–	–	√

24. STANDBY FUNCTION

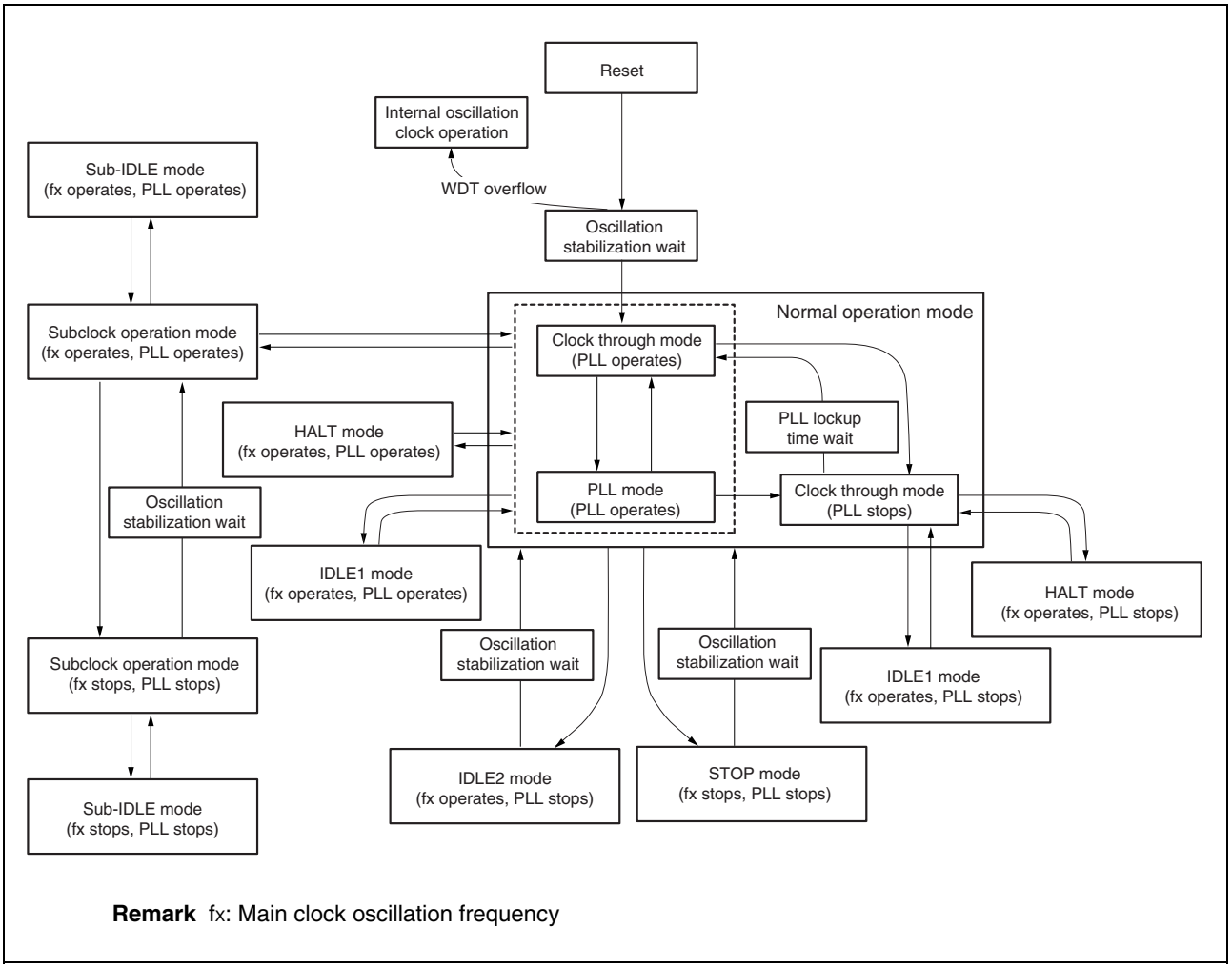
The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. The available standby modes are listed in Table 24-1.

Table 24-1. Standby Modes

Mode	Function Overview
HALT mode	Mode to stop only the operating clock of the CPU
IDLE1 mode	Mode to stop all the operations of the internal circuit except the oscillator, PLL operation[Note], and flash memory
IDLE2 mode	Mode to stop all the operations of the internal circuit except the oscillator
STOP mode	Mode to stop all the operations of the internal circuit except the subclock oscillator
Subclock operation mode	Mode to operate internal system clock by subclock
Sub-IDLE mode	Mode to stop all the operations of the internal circuit except the oscillator in subclock operation mode

Note PLL retains the previous operation status.

The following figure shows the status transitions of the standby function.



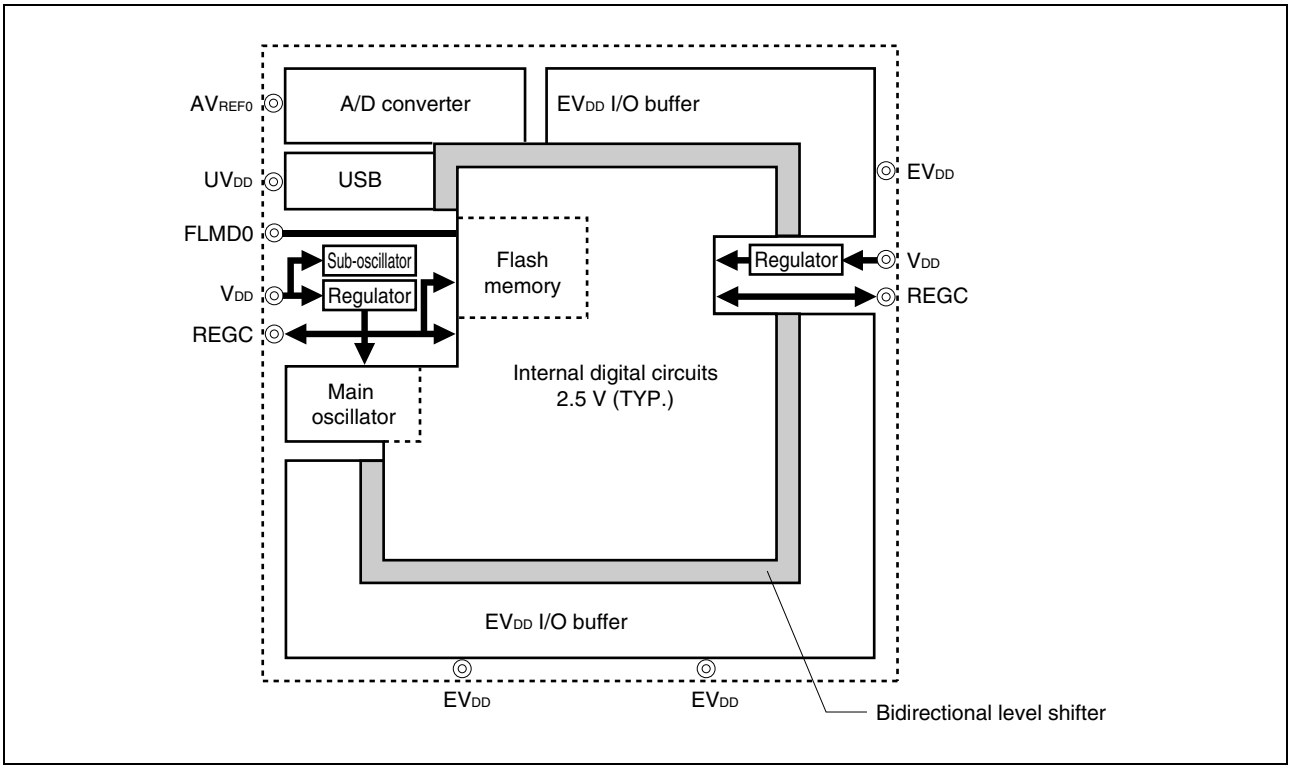
Remark fx: Main clock oscillation frequency

28. REGULATOR FUNCTION

The V850ES/Jx3-E includes a regulator to reduce power consumption and noise.

This regulator supplies a stepped-down V_{DD} power supply voltage to the oscillator block and internal logic circuits except the A/D converter and output buffers). The regulator output voltage is set to 2.5 V (TYP.).

The outline of the regulator functions is shown below.



30. ON-CHIP DEBUG FUNCTION

Debugging can be implemented with the V850ES/Jx3-E mounted on the target system.

The NEC Electronics on-chip debug emulators MINICUBE and MINICUBE2 are planned to support the V850ES/Jx3-E.

○ MINICUBE

An on-chip debug function is implemented by using the DCU (debug control unit) in the V850ES/Jx3-E, using the $\overline{\text{DRST}}$, DCK, DMS, DDI, and DDO pins as the debug interface pins.

○ MINICUBE2

An on-chip debug function is implemented by using the user resources (on-chip flash memory, internal RAM, etc.) instead of the DCU, and using the SIF0, SOF0, and $\overline{\text{SCKF0}}$ pins or the SIF3, SOF3, and $\overline{\text{SCKF3}}$ pins or the RXDC0 and TXDC0 pins as the interface pins.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.