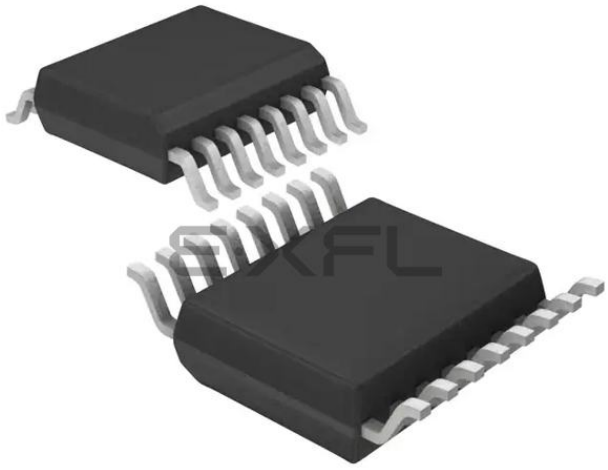

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, SPI
Peripherals	LVD, POR, PWM
Number of I/O	12
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908qc8cdte

3.3.4.4 Code Width and Quantization Error . . . 51
3.3.4.5 Linearity Errors . . . 51
3.3.4.6 Code Jitter, Non-Monotonicity and Missing Codes . . . 51
3.4 Interrupts . . . 52
3.5 Low-Power Modes . . . 52
3.5.1 Wait Mode . . . 52
3.5.2 Stop Mode . . . 52
3.6 ADC10 During Break Interrupts . . . 52
3.7 I/O Signals . . . 53
3.7.1 ADC10 Analog Power Pin (V_{DDA}) . . . 53
3.7.2 ADC10 Analog Ground Pin (V_{SSA}) . . . 53
3.7.3 ADC10 Voltage Reference High Pin (V_{REFH}) . . . 53
3.7.4 ADC10 Voltage Reference Low Pin (V_{REFL}) . . . 53
3.7.5 ADC10 Channel Pins (ADn) . . . 54
3.8 Registers . . . 54
3.8.1 ADC10 Status and Control Register . . . 54
3.8.2 ADC10 Result High Register (ADRH) . . . 56
3.8.3 ADC10 Result Low Register (ADRL) . . . 56
3.8.4 ADC10 Clock Register (ADCLK) . . . 56

Chapter 4
Configuration Registers (CONFIG1 and CONFIG2)

4.1 Introduction . . . 59
4.2 Functional Description . . . 59

Chapter 5
Computer Operating Properly (COP)

5.1 Introduction . . . 63
5.2 Functional Description . . . 63
5.3 I/O Signals . . . 64
5.3.1 BUSCLKX4 . . . 64
5.3.2 STOP Instruction . . . 64
5.3.3 COPCTL Write . . . 64
5.3.4 Power-On Reset . . . 64
5.3.5 Internal Reset . . . 64
5.3.6 COPD (COP Disable) . . . 64
5.3.7 COPRS (COP Rate Select) . . . 65
5.4 COP Control Register . . . 65
5.5 Interrupts . . . 65
5.6 Monitor Mode . . . 65
5.7 Low-Power Modes . . . 65
5.7.1 Wait Mode . . . 65
5.7.2 Stop Mode . . . 65
5.8 COP Module During Break Mode . . . 65

13.3.2.2 Character Transmission . . . 126
13.3.2.3 Break Characters . . . 127
13.3.2.4 Idle Characters . . . 128
13.3.2.5 Inversion of Transmitted Output . . . 128
13.3.3 Receiver . . . 128
13.3.3.1 Character Length . . . 128
13.3.3.2 Character Reception . . . 128
13.3.3.3 Data Sampling . . . 130
13.3.3.4 Framing Errors . . . 131
13.3.3.5 Baud Rate Tolerance . . . 131
13.3.3.6 Receiver Wakeup . . . 133
13.4 Interrupts . . . 134
13.4.1 Transmitter Interrupts . . . 134
13.4.2 Receiver Interrupts . . . 134
13.4.3 Error Interrupts . . . 134
13.5 Low-Power Modes . . . 135
13.5.1 Wait Mode . . . 135
13.5.2 Stop Mode . . . 135
13.6 ESCI During Break Interrupts . . . 135
13.7 I/O Signals . . . 135
13.7.1 ESCI Transmit Data (TxD) . . . 135
13.7.2 ESCI Receive Data (RxD) . . . 136
13.8 Registers . . . 136
13.8.1 ESCI Control Register 1 . . . 136
13.8.2 ESCI Control Register 2 . . . 138
13.8.3 ESCI Control Register 3 . . . 140
13.8.4 ESCI Status Register 1 . . . 141
13.8.5 ESCI Status Register 2 . . . 143
13.8.6 ESCI Data Register . . . 144
13.8.7 ESCI Baud Rate Register . . . 144
13.8.8 ESCI Prescaler Register . . . 145
13.9 ESCI Arbiter . . . 149
13.9.1 ESCI Arbiter Control Register . . . 149
13.9.2 ESCI Arbiter Data Register . . . 150
13.9.3 Bit Time Measurement . . . 150
13.9.4 Arbitration Mode . . . 151

Chapter 14
System Integration Module (SIM)

14.1 Introduction . . . 153
14.2 $\overline{\text{RST}}$ and $\overline{\text{IRQ}}$ Pins Initialization . . . 153
14.3 SIM Bus Clock Control and Generation . . . 153
14.3.1 Bus Timing . . . 155
14.3.2 Clock Start-Up from POR . . . 155
14.3.3 Clocks in Stop Mode and Wait Mode . . . 155
14.4 Reset and System Initialization . . . 155
14.4.1 External Pin Reset . . . 155

14.4.2 Active Resets from Internal Sources . . . 156
14.4.2.1 Power-On Reset . . . 157
14.4.2.2 Computer Operating Properly (COP) Reset . . . 157
14.4.2.3 Illegal Opcode Reset . . . 158
14.4.2.4 Illegal Address Reset . . . 158
14.4.2.5 Low-Voltage Inhibit (LVI) Reset . . . 158
14.5 SIM Counter . . . 158
14.5.1 SIM Counter During Power-On Reset . . . 158
14.5.2 SIM Counter During Stop Mode Recovery . . . 158
14.5.3 SIM Counter and Reset States . . . 159
14.6 Exception Control . . . 159
14.6.1 Interrupts . . . 159
14.6.1.1 Hardware Interrupts . . . 159
14.6.1.2 SWI Instruction . . . 162
14.6.2 Interrupt Status Registers . . . 162
14.6.2.1 Interrupt Status Register 1 . . . 163
14.6.2.2 Interrupt Status Register 2 . . . 163
14.6.2.3 Interrupt Status Register 3 . . . 163
14.6.3 Reset . . . 163
14.6.4 Break Interrupts . . . 164
14.6.5 Status Flag Protection in Break Mode . . . 164
14.7 Low-Power Modes . . . 164
14.7.1 Wait Mode . . . 164
14.7.2 Stop Mode . . . 165
14.8 SIM Registers . . . 166
14.8.1 SIM Reset Status Register . . . 167
14.8.2 Break Flag Control Register . . . 168

Chapter 15
Serial Peripheral Interface (SPI) Module

15.1 Introduction . . . 169
15.2 Features . . . 169
15.3 Functional Description . . . 169
15.3.1 Master Mode . . . 172
15.3.2 Slave Mode . . . 172
15.3.3 Transmission Formats . . . 173
15.3.3.1 Clock Phase and Polarity Controls . . . 173
15.3.3.2 Transmission Format When CPHA = 0 . . . 173
15.3.3.3 Transmission Format When CPHA = 1 . . . 174
15.3.3.4 Transmission Initiation Latency . . . 175
15.3.4 Queuing Transmission Data . . . 177
15.3.5 Resetting the SPI . . . 178
15.3.6 Error Conditions . . . 178
15.3.6.1 Overflow Error . . . 178
15.3.6.2 Mode Fault Error . . . 180
15.4 Interrupts . . . 181
15.5 Low-Power Modes . . . 182
15.5.1 Wait Mode . . . 182
15.5.2 Stop Mode . . . 182

15.6 SPI During Break Interrupts . . . 182
15.7 I/O Signals . . . 183
15.7.1 MISO (Master In/Slave Out) . . . 183
15.7.2 MOSI (Master Out/Slave In) . . . 183
15.7.3 SPSCK (Serial Clock) . . . 183
15.7.4 $\overline{SS}$ (Slave Select) . . . 183
15.8 Registers . . . 184
15.8.1 SPI Control Register . . . 184
15.8.2 SPI Status and Control Register . . . 186
15.8.3 SPI Data Register . . . 188

Chapter 16
Timer Interface Module (TIM1)

16.1 Introduction . . . 189
16.2 Features . . . 189
16.3 Functional Description . . . 189
16.3.1 TIM1 Counter Prescaler . . . 192
16.3.2 Input Capture . . . 192
16.3.3 Output Compare . . . 192
16.3.3.1 Unbuffered Output Compare . . . 192
16.3.3.2 Buffered Output Compare . . . 192
16.3.4 Pulse Width Modulation (PWM) . . . 193
16.3.4.1 Unbuffered PWM Signal Generation . . . 194
16.3.4.2 Buffered PWM Signal Generation . . . 194
16.3.4.3 PWM Initialization . . . 195
16.4 Interrupts . . . 196
16.5 Low-Power Modes . . . 196
16.5.1 Wait Mode . . . 196
16.5.2 Stop Mode . . . 196
16.6 TIM1 During Break Interrupts . . . 197
16.7 I/O Signals . . . 197
16.7.1 TIM1 Channel I/O Pins (T1CH3:T1CH0) . . . 197
16.7.2 TIM1 Clock Pin (T1CLK) . . . 197
16.8 Registers . . . 197
16.8.1 TIM1 Status and Control Register . . . 197
16.8.2 TIM1 Counter Registers . . . 199
16.8.3 TIM1 Counter Modulo Registers . . . 200
16.8.4 TIM1 Channel Status and Control Registers . . . 200
16.8.5 TIM1 Channel Registers . . . 204

Chapter 17
Timer Interface Module (TIM2)

17.1 Introduction . . . 205
17.2 Features . . . 205
17.3 Functional Description . . . 205
17.3.1 TIM2 Counter Prescaler . . . 205
17.3.2 Input Capture . . . 207

Table 1-2. Pin Functions

Pin Name	Description	Input/Output
V_{DD}	Power supply	Power
V_{SS}	Power supply ground	Power
PTA0	PTA0 — General purpose I/O port	Input/Output
	T1CH0 — Timer Channel 0 I/O	Input/Output
	AD0 — A/D channel 0 input	Input
	KBI0 — Keyboard interrupt input 0	Input
PTA1	PTA1 — General purpose I/O port	Input/Output
	T1CH1 — Timer Channel 1 I/O	Input/Output
	AD1 — A/D channel 1 input	Input
	KBI1 — Keyboard interrupt input 1	Input
PTA2[1]	PTA2 — General purpose input-only port	Input
	$\overline{IRQ}$ — External interrupt with programmable pullup and Schmitt trigger input	Input
	KBI2 — Keyboard interrupt input 2	Input
	T1CLK — TIM1 timer clock input	Input
PTA3	PTA3 — General purpose I/O port	Input/Output
	$\overline{RST}$ — Reset input, active low with internal pullup and Schmitt trigger	Input
	KBI3 — Keyboard interrupt input 3	Input
PTA4	PTA4 — General purpose I/O port	Input/Output
	OSC2 —XTAL oscillator output (XTAL option only) RC or internal oscillator output (OSC2EN = 1 in PTAPUE register)	Output Output
	AD2 — A/D channel 2 input	Input
	KBI4 — Keyboard interrupt input 4	Input
PTA5	PTA5 — General purpose I/O port	Input/Output
	OSC1 — XTAL, RC, or external oscillator input	Input
	AD3 — A/D channel 3 input	Input
	KBI5 — Keyboard interrupt input 5	Input
PTB0	PTB0 — General-purpose I/O port	Input/Output
	SPSCK— SPI serial clock	Input/Output
	AD4 — A/D channel 4 input	Input
PTB1	PTB1 — General-purpose I/O port	Input/Output
	MOSI — SPI data transmitted	Input/Output
	T2CH1[2] — TIM2 channel 1	Input/Output
	AD5 — A/D channel 5 input	Input

— Continued on next page

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0019	ESCI Arbiter Data Register (SCIADAT) See page 150.	Read:	ARD7	ARD6	ARD5	ARD4	ARD3	ARD2	ARD1	ARD0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001A	Keyboard Status and Control Register (KBSCR) See page 90.	Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
		Write:						ACKK		
		Reset:	0	0	0	0	0	0	0	0
$001B	Keyboard Interrupt Enable Register (KBIER) See page 90.	Read:	0	R	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001C	Keyboard Interrupt Polarity Register (KBIPR) See page 91.	Read:	0	0	KBIP5	KBIP4	KBIP3	KBIP2	KBIP1	KBIP0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001D	IRQ Status and Control Register (INTSCR) See page 83.	Read:	0	0	0	0	IRQF	0	IMASK	MODE
		Write:						ACK		
		Reset:	0	0	0	0	0	0	0	0
$001E	Configuration Register 2 (CONFIG2)(1) See page 59.	Read:	IRQPUD	IRQEN	0	0	TIM2POS	ESCIBDSRC	OSCENIN-STOP	RSTEN
		Write:								
		Reset:	0	0	0	0	0	0	0	0(2)

1. One-time writable register after each reset.
2. RSTEN reset to 0 by a power-on reset (POR) only.

$001F	Configuration Register 1 (CONFIG1)(1) See page 60.	Read:	COPRS	LVISTOP	LVIRSTD	LVIPWRD	LVITRIP	SSREC	STOP	COPD
		Write:								
		Reset:	0	0	0	0	0(2)	0	0	0

1. One-time writable register after each reset.
2. LVI5OR3 reset to 0 by a power-on reset (POR) only.

$0020	TIM1 Status and Control Register (T1SC) See page 198.	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
$0021	TIM1 Counter Register High (T1CNTH) See page 199.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0022	TIM1 Counter Register Low (T1CNTL) See page 199.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0023	TIM1 Counter Modulo Register High (T1MODH) See page 200.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1

= Unimplemented R = Reserved U = Unaffected

Figure 2-2. Control, Status, and Data Registers (Sheet 3 of 8)

Table 6-1. Instruction Set Summary (Sheet 3 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
CLR *opr* CLRA CLRX CLRH CLR *opr*,X CLR ,X CLR *opr*,SP	Clear	M ← $00 A ← $00 X ← $00 H ← $00 M ← $00 M ← $00 M ← $00	0	–	–	0	1	–	DIR INH INH INH IX1 IX SP1	3F 4F 5F 8C 6F 7F 9E6F	dd ff ff	3 1 1 1 3 2 4
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X CMP *opr*,SP CMP *opr*,SP	Compare A with M	(A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A1 B1 C1 D1 E1 F1 9EE1 9ED1	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
COM *opr* COMA COMX COM *opr*,X COM ,X COM *opr*,SP	Complement (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (M) X ← ($\overline{X}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	0	–	–	↕	↕	1	DIR INH INH IX1 IX SP1	33 43 53 63 73 9E63	dd ff ff	4 1 1 4 3 5
CPHX #*opr* CPHX *opr*	Compare H:X with M	(H:X) – (M:M + 1)	↕	–	–	↕	↕	↕	IMM DIR	65 75	ii ii+1 dd	3 4
CPX #*opr* CPX *opr* CPX *opr* CPX ,X CPX *opr*,X CPX *opr*,X CPX *opr*,SP CPX *opr*,SP	Compare X with M	(X) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A3 B3 C3 D3 E3 F3 9EE3 9ED3	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
DAA	Decimal Adjust A	$(A)_{10}$	U	–	–	↕	↕	↕	INH	72		2
DBNZ *opr,rel* DBNZA *rel* DBNZX *rel* DBNZ *opr*,X,*rel* DBNZ X,*rel* DBNZ *opr*,SP,*rel*	Decrement and Branch if Not Zero	A ← (A) – 1 or M ← (M) – 1 or X ← (X) – 1 PC ← (PC) + 3 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 3 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 4 + *rel* ? (result) ≠ 0	–	–	–	–	–	–	DIR INH INH IX1 IX SP1	3B 4B 5B 6B 7B 9E6B	dd rr rr rr ff rr rr ff rr	5 3 3 5 4 6
DEC *opr* DECA DECX DEC *opr*,X DEC ,X DEC *opr*,SP	Decrement	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1 M ← (M) – 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3A 4A 5A 6A 7A 9E6A	dd ff ff	4 1 1 4 3 5
DIV	Divide	A ← (H:A)/(X) H ← Remainder	–	–	–	–	↕	↕	INH	52		7
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X EOR *opr*,SP EOR *opr*,SP	Exclusive OR M with A	A ← (A ⊕ M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A8 B8 C8 D8 E8 F8 9EE8 9ED8	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
INC *opr* INCA INCX INC *opr*,X INC ,X INC *opr*,SP	Increment	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1 M ← (M) + 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3C 4C 5C 6C 7C 9E6C	dd ff ff	4 1 1 4 3 5

Chapter 10
Oscillator Mode (OSC)

10.1 Introduction

The oscillator (OSC) module is used to provide a stable clock source for the MCU system and bus.

The OSC shares its pins with general-purpose input/output (I/O) port pins. See Figure 10-1 for port location of these shared pins. The OSC2EN bit is located in the port A pull enable register (PTAPUEN) on this MCU. See Chapter 11 Input/Output Ports (PORTS) for information on PTAPUEN register.

10.2 Features

The bus clock frequency is one fourth of any of these clock source options:

1. Internal oscillator: An internally generated, fixed frequency clock, trimmable to ± 0.4%. There are four choices for the internal oscillator, 25.6 MHz, 12.8 MHz, 8 MHz, or 4 MHz. The 4-MHz internal oscillator is the default option out of reset.
2. External oscillator: An external clock that can be driven directly into OSC1.
3. External RC: A built-in oscillator module (RC oscillator) that requires an external R connection only. The capacitor is internal to the chip.
4. External crystal: A built-in XTAL oscillator that requires an external crystal or ceramic-resonator. There are three crystal frequency ranges supported, 8–32 MHz, 1–8 MHz, and 32–100 kHz.

10.3 Functional Description

The oscillator contains these major subsystems:

- Internal oscillator circuit
- Internal or external clock switch control
- External clock circuit
- External crystal circuit
- External RC clock circuit

10.3.1 Internal Signal Definitions

The following signals and clocks are used in the functional description and figures of the OSC module.

10.3.1.1 Oscillator Enable Signal (SIMOSCEN)

The SIMOSCEN signal comes from the system integration module (SIM) and disables the XTAL oscillator circuit, the RC oscillator, or the internal oscillator in stop mode. OSCENINSTOP in the configuration register can be used to override this signal.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	OSCOPT1	OSCOPT0	ICFS1	ICFS0	ECFS1	ECFS0	ECGON	ECGST
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-4. Oscillator Status and Control Register (OSCSC)

OSCOPT1:OSCOPT0 — OSC Option Bits

These read/write bits allow the user to change the clock source for the MCU. The default reset condition has the bus clock being derived from the internal oscillator. See 10.3.2.2 Internal to External Clock Switching for information on changing clock sources.

OSCOPT1	OSCOPT0	Oscillator Modes
0	0	Internal oscillator (frequency selected using ICFSx bits)
0	1	External oscillator clock
1	0	External RC
1	1	External crystal (range selected using ECFSx bits)

ICFS1:ICFS0 — Internal Clock Frequency Select Bits

These read/write bits enable the frequency to be increased for applications requiring a faster bus clock when running off the internal oscillator. The WAIT instruction has no effect on the oscillator logic. BUSCLKX2 and BUSCLKX4 continue to drive to the SIM module.

ICFS1	ICFS0	Internal Clock Frequency
0	0	4.0 MHz — default reset condition
0	1	8.0 MHz
1	0	12.8 MHz
1	1	25.6 MHz

ECFS1:ECFS0 — External Crystal Frequency Select Bits

These read/write bits enable the specific amplifier for the crystal frequency range. Refer to oscillator characteristics table in the Electricals section for information on maximum external clock frequency versus supply voltage.

ECFS1	ECFS0	External Crystal Frequency
0	0	8 MHz – 32 MHz
0	1	1 MHz – 8 MHz
1	0	32 kHz – 100 kHz
1	1	Reserved

ECGON — External Clock Generator On Bit

This read/write bit enables the OSC1 pin as the clock input to the MCU, so that the switching process can be initiated. This bit is cleared by reset. This bit is ignored in monitor mode with the internal oscillator bypassed.

1 = External clock enabled
0 = External clock disabled

11.5.3 Port C Input Pullup Enable Register

The port C input pullup enable register (PTCPUE) contains a software configurable pullup device for each of the four port C pins. Each bit is individually configurable and requires the corresponding data direction register, DDRCx, be configured as input. Each pullup device is automatically and dynamically disabled when its corresponding DDRCx bit is configured as output.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	PTCPUE3	PTCPUE2	PTCPUE1	PTCPUE0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-12. Port C Input Pullup Enable Register (PTCPUE)

PTCPUE[3:0] — Port C Input Pullup Enable Bits

These read/write bits are software programmable to enable pullup devices on port C pins

1 = Corresponding port C pin configured to have internal pull if its DDRC bit is set to 0

0 = Pullup device is disconnected on the corresponding port C pin regardless of the state of its DDRC bit.

Table 11-3 summarizes the operation of the port C pins.

Table 11-3. Port C Pin Functions

PTCPUE Bit	DDRC Bit	PTC Bit	I/O Pin Mode	Accesses to DDRC	Accesses to PTC	
				Read/Write	Read	Write
1	0	X(1)	Input, V_{DD}(2)	DDRC2–DDRC0	Pin	PTC3–PTC0(3)
0	0	X	Input, Hi-Z(4)	DDRC2–DDRC0	Pin	PTC3–PTC0(3)
X	1	X	Output	DDRC2–DDRC0	PTC3–PTC0	PTC3–PTC0

1. X = don't care
2. I/O pin pulled to V_{DD} by internal pullup.
3. Writing affects data register, but does not affect input.
4. Hi-Z = high impedance

11.6 Port D

Port D is an 8-bit general purpose I/O port. Each port D pin can be configured to have an internal pullup when used as an input port pin.

11.6.1 Port D Data Register

The port D data register (PTD) contains a data latch for each of the eight port D pins.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0
Write:								
Reset:	Unaffected by reset							

Figure 11-13. Port D Data Register (PTD)

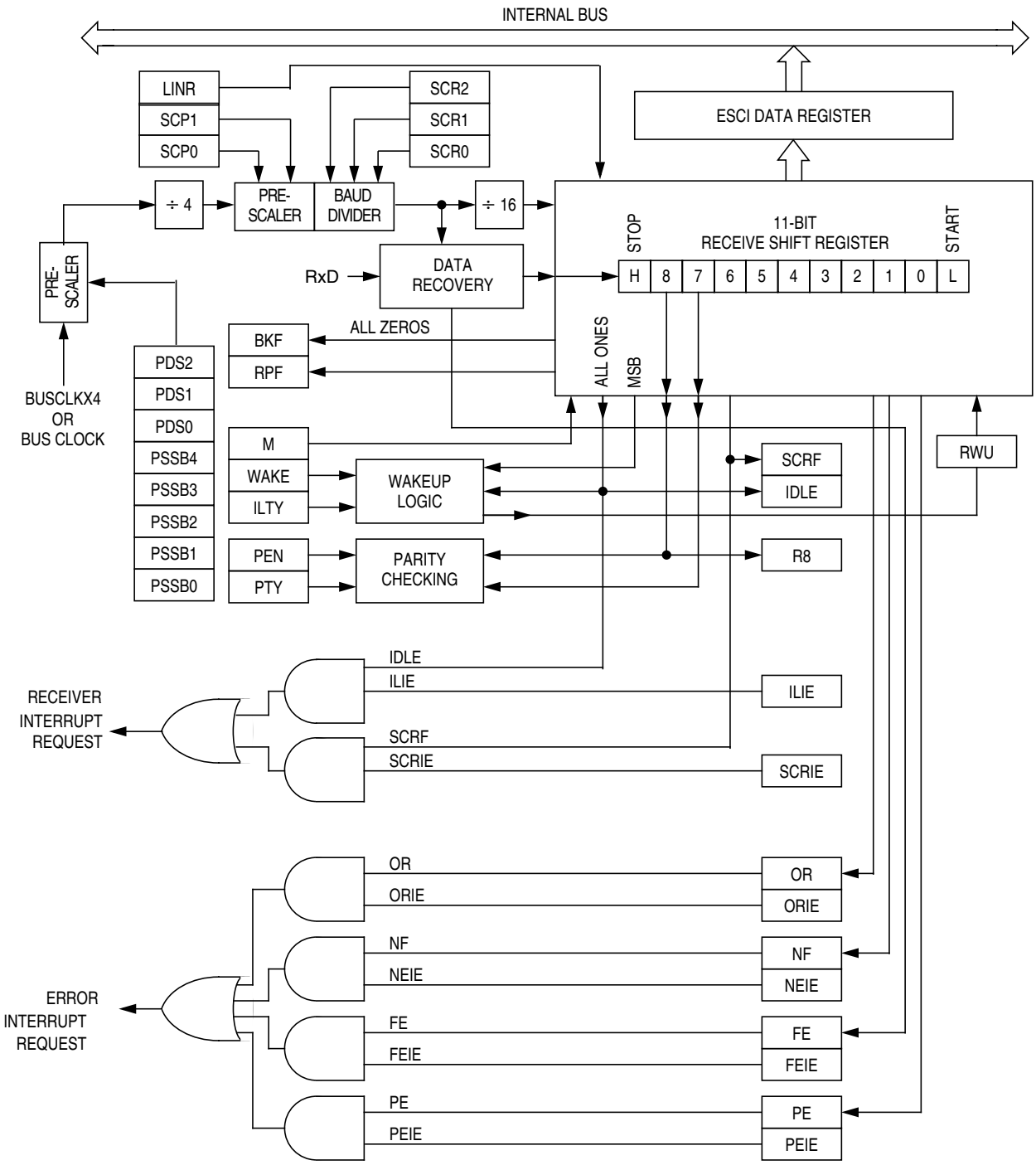

Figure 13-5. ESCI Receiver Block Diagram

NF — Receiver Noise Flag Bit

This clearable, read-only bit is set when the ESCI detects noise on the RxD pin. NF generates an NF interrupt request if the NEIE bit in SCC3 is also set. Clear the NF bit by reading SCS1 and then reading the SCDR.

1 = Noise detected
0 = No noise detected

FE — Receiver Framing Error Bit

This clearable, read-only bit is set when a 0 is accepted as the stop bit. FE generates an ESCI error interrupt request if the FEIE bit in SCC3 also is set. Clear the FE bit by reading SCS1 with FE set and then reading the SCDR.

1 = Framing error detected
0 = No framing error detected

PE — Receiver Parity Error Bit

This clearable, read-only bit is set when the ESCI detects a parity error in incoming data. PE generates a PE interrupt request if the PEIE bit in SCC3 is also set. Clear the PE bit by reading SCS1 with PE set and then reading the SCDR.

1 = Parity error detected
0 = No parity error detected

13.8.5 ESCI Status Register 2

ESCI status register 2 (SCS2) contains flags to signal these conditions:

- Break character detected
- Reception in progress

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	BKF	RPF
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-14. ESCI Status Register 2 (SCS2)

BKF — Break Flag Bit

This clearable, read-only bit is set when the ESCI detects a break character on the RxD pin. In SCS1, the FE and SCRF bits are also set. In 9-bit character transmissions, the R8 bit in SCC3 is cleared. BKF does not generate a interrupt request. Clear BKF by reading SCS2 with BKF set and then reading the SCDR. Once cleared, BKF can become set again only after 1s again appear on the RxD pin followed by another break character.

1 = Break character detected
0 = No break character detected

RPF — Reception in Progress Flag Bit

This read-only bit is set when the receiver detects a 0 during the RT1 time period of the start bit search. RPF does not generate an interrupt request. RPF is reset after the receiver detects false start bits (usually from noise or a baud rate mismatch), or when the receiver detects an idle character. Polling RPF before disabling the ESCI module or entering stop mode can show whether a reception is in progress.

1 = Reception in progress
0 = No reception in progress

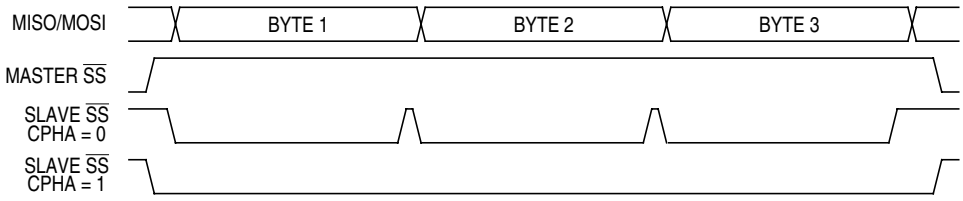

Figure 15-12. CPHA/SS Timing

NOTE

A high on the SS pin of a slave SPI puts the MISO pin in a high-impedance state. The slave SPI ignores all incoming SPSCK clocks, even if it was already in the middle of a transmission.

When an SPI is configured as a master, the SS input can be used in conjunction with the MODF flag to prevent multiple masters from driving MOSI and SPSCK. (See 15.3.6.2 Mode Fault Error.) For the state of the SS pin to set the MODF flag, the MODFEN bit in the SPSCK register must be set. If the MODFEN bit is 0 for an SPI master, the SS pin can be used as a general-purpose I/O under the control of the data direction register of the shared I/O port. When MODFEN is 1, it is an input-only pin to the SPI regardless of the state of the data direction register of the shared I/O port.

User software can read the state of the SS pin by configuring the appropriate pin as an input and reading the port data register. See Table 15-2.

Table 15-2. SPI Configuration

SPE	SPMSTR	MODFEN	SPI Configuration	Function of SS Pin
0	X[1]	X	Not enabled	General-purpose I/O; SS ignored by SPI
1	0	X	Slave	Input-only to SPI
1	1	0	Master without MODF	General-purpose I/O; SS ignored by SPI
1	1	1	Master with MODF	Input-only to SPI

1. X = Don't care

15.8 Registers

The following registers allow the user to control and monitor SPI operation:

- SPI control register (SPCR)
- SPI status and control register (SPSCR)
- SPI data register (SPDR)

15.8.1 SPI Control Register

The SPI control register:

- Enables SPI module interrupt requests
- Configures the SPI module as master or slave
- Selects serial clock polarity and phase
- Configures the SPSCK, MOSI, and MISO pins as open-drain outputs
- Enables the SPI module

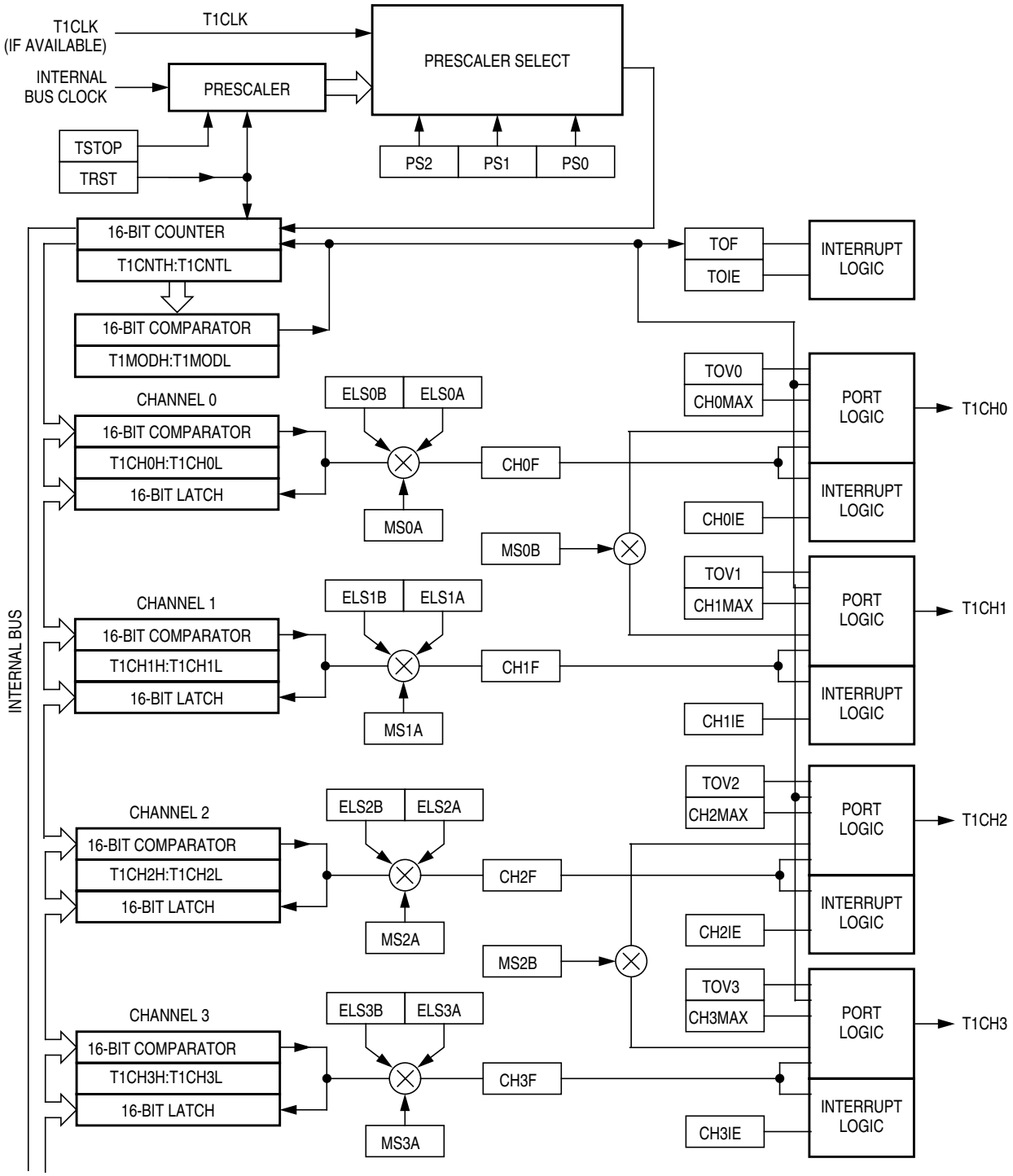

Figure 16-2. TIM1 Block Diagram

PS[2:0] — Prescaler Select Bits

These read/write bits select one of the seven prescaler outputs as the input to the counter as Table 16-1 shows.

Table 16-1. Prescaler Selection

PS2	PS1	PS0	TIM1 Clock Source
0	0	0	Internal bus clock ÷ 1
0	0	1	Internal bus clock ÷ 2
0	1	0	Internal bus clock ÷ 4
0	1	1	Internal bus clock ÷ 8
1	0	0	Internal bus clock ÷ 16
1	0	1	Internal bus clock ÷ 32
1	1	0	Internal bus clock ÷ 64
1	1	1	T1CLK (if available)

16.8.2 TIM1 Counter Registers

The two read-only TIM1 counter registers contain the high and low bytes of the value in the counter. Reading the high byte (T1CNTH) latches the contents of the low byte (T1CNTL) into a buffer. Subsequent reads of T1CNTH do not affect the latched T1CNTL value until T1CNTL is read. Reset clears the TIM1 counter registers. Setting the TIM1 reset bit (TRST) also clears the TIM1 counter registers.

NOTE

If you read T1CNTH during a break interrupt, be sure to unlatch T1CNTL by reading T1CNTL before exiting the break interrupt. Otherwise, T1CNTL retains the value latched during the break.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 16-5. TIM1 Counter High Register (T1CNTH)

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 16-6. TIM1 Counter Low Register (T1CNTL)

18.2.2 Break Module Registers

These registers control and monitor operation of the break module:

- Break status and control register (BRKSCR)
- Break address register high (BRKH)
- Break address register low (BRKL)
- Break status register (BSR)
- Break flag control register (BFCR)

18.2.2.1 Break Status and Control Register

The break status and control register (BRKSCR) contains break module enable and status bits.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BRKE	BRKA	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 18-3. Break Status and Control Register (BRKSCR)

BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a 0 to bit 7. Reset clears the BRKE bit.

1 = Breaks enabled on 16-bit address match
0 = Breaks disabled

BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a 1 to BRKA generates a break interrupt. Clear BRKA by writing a 0 to it before exiting the break routine. Reset clears the BRKA bit.

1 = Break address match
0 = No break address match

18.2.2.2 Break Address Registers

The break address registers (BRKH and BRKL) contain the high and low bytes of the desired breakpoint address. Reset clears the break address registers.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 18-4. Break Address Register High (BRKH)

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 18-5. Break Address Register Low (BRKL)

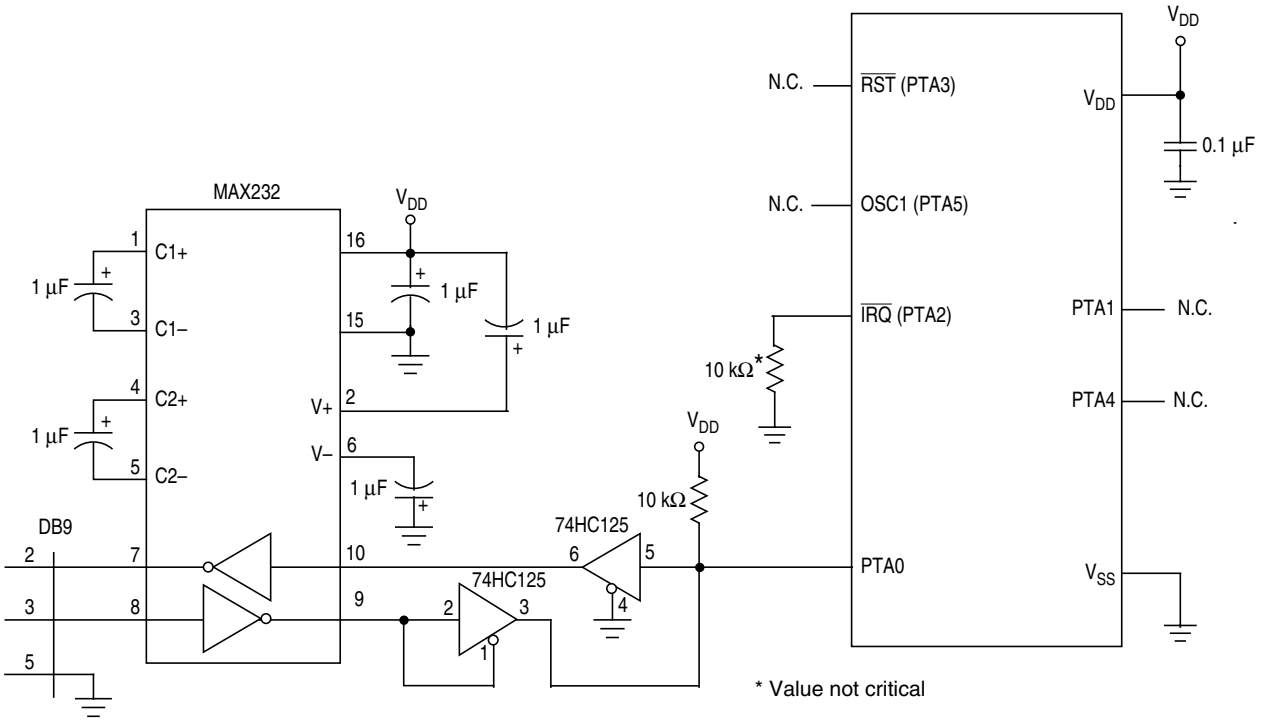

Figure 18-12. Monitor Mode Circuit (Internal Clock, No High Voltage)

Simple monitor commands can access any memory address. In monitor mode, the MCU can execute code downloaded into RAM by a host computer while most MCU pins retain normal operating mode functions. All communication between the host computer and the MCU is through the PTA0 pin. A level-shifting and multiplexing interface is required between PTA0 and the host computer. PTA0 is used in a wired-OR configuration and requires a pullup resistor.

The monitor code has been updated from previous versions of the monitor code to allow enabling the internal oscillator to generate the internal clock. This addition, which is enabled when $\overline{IRQ}$ is held low out of reset, is intended to support serial communication/programming at 9600 baud in monitor mode by using the internal oscillator, and the internal oscillator user trim value OSCTRIM (FLASH location $FFC0, if programmed) to generate the desired internal frequency (3.2 MHz). Since this feature is enabled only when $\overline{IRQ}$ is held low out of reset, it cannot be used when the reset vector is programmed (i.e., the value is not $FFFF) because entry into monitor mode in this case requires V_{TST} on $\overline{IRQ}$. The $\overline{IRQ}$ pin must remain low during this monitor session in order to maintain communication.

Table 18-1 shows the pin conditions for entering monitor mode. As specified in the table, monitor mode may be entered after a power-on reset (POR) and will allow communication at 9600 baud provided one of the following sets of conditions is met:

- If $FFFE and $FFFF do not contain $FF (programmed state):
  - The external clock is 9.8304 MHz
  - $\overline{IRQ}$ = V_{TST}
- If $FFFE and $FFFF contain $FF (erased state):
  - The external clock is 9.8304 MHz
  - $\overline{IRQ}$ = V_{DD} (this can be implemented through the internal $\overline{IRQ}$ pullup)
- If $FFFE and $FFFF contain $FF (erased state):
  - $\overline{IRQ}$ = V_{SS} (internal oscillator is selected, no external clock required)

Characteristic	Symbol	Min	Typ	Max	Unit
RC oscillator external resistor V_{DD} = 5 V V_{DD} = 3.3 V	R_{EXT}		See Figure 19-7 See Figure 19-8		—
Crystal frequency, XTALCLK (1) (7) (8) ECFS1:ECFS0 = 00 ($V_{DD} \geq$ 4.5 V) ECFS1:ECFS0 = 00 ECFS1:ECFS0 = 01 ECFS1:ECFS0 = 10	$f_{OSCXCLK}$	 8 8 1 30	 — — — —	 32 16 8 100	 MHz MHz MHz kHz
ECFS1:ECFS0 = 00(9) ($f_{OSCXCLK}$: 8–32 MHz) Feedback bias resistor Crystal load capacitance(10) Crystal capacitors(10)	 R_B C_L C_1, C_2	 — — —	 1 20 (2 x C_L) – 5pF	 — — —	 MΩ pF pF
ECFS1:ECFS0 = 01(9) ($f_{OSCXCLK}$: 1–8 MHz) Crystal series damping resistor $f_{OSCXCLK}$ = 1 MHz $f_{OSCXCLK}$ = 4 MHz $f_{OXCSCLK}$ = 8 MHz Feedback bias resistor Crystal load capacitance(10) Crystal capacitors(10)	 R_S R_B C_L C_1, C_2	 — — — — — —	 20 10 0 5 18 (2 x C_L) –10pF	 — — — — — —	 kΩ kΩ kΩ MΩ pF pF
ECFS1:ECFS0 = 10(9) ($f_{OSCXCLK}$: 30–100 kHz) Feedback bias resistor Crystal load capacitance(10) Crystal capacitors(10)	 R_B C_L C_1, C_2	 — — —	 10 12.5 (2 x C_L) –10	 — — —	 MΩ pF pF
PWU module Internal RC oscillator frequency	f_{INTRC}	—	32	—	kHz

1. Bus frequency, f_{OP}, is oscillator frequency divided by 4.
2. Factory trimmed to provided 12.8MHz accuracy requirement (± 5%, @ 25 C and V_{DD} = 5.0 V) for forced monitor mode communication. User should trim in-circuit to obtain the most accurate internal oscillator frequency for his application.
3. Values are based on characterization results, not tested in production.
4. Deviation values assumes trimming in target application @25 C and midpoint of voltage range, for example 5.0 V for 5 V ± 10% operation.
5. No more than 10% duty cycle deviation from 50%.
6. When external oscillator clock is greater than 1 MHz, ECFS1:ECFS0 must be 00 or 01.
7. Use fundamental mode only, do **not** use overtone crystals or overtone ceramic resonators.
8. Due to variations in electrical properties of external components such as, ESR and Load Capacitance, operation above 16 MHz is not guaranteed for all crystals or ceramic resonators. Operation above 16 MHz requires that a Negative Resistance Margin (NRM) characterization and component optimization be performed by the crystal or ceramic resonator vendor for every different type of crystal or ceramic resonator which will be used. This characterization and optimization must be performed at the extremes of voltage and temperature which will be applied to the microcontroller in the application. The NRM must meet or exceed 10x the maximum ESR of the crystal or ceramic resonator for acceptable performance.
9. Do not use damping resistor when ECFS1:ECFS0 = 00 or 10.
10. Consult crystal vendor data sheet.

19.17 Memory Characteristics

Characteristic	Symbol	Min	Typ(1)	Max	Unit
RAM data retention voltage (2)	V_{RDR}	1.3	—	—	V
FLASH program bus clock frequency	—	1	—	—	MHz
FLASH PGM/ERASE supply voltage (V_{DD})	$V_{PGM/ERASE}$	2.7	—	5.5	V
FLASH read bus clock frequency	f_{Read}(3)	0	—	8 M	Hz
FLASH page erase time	t_{Erase}	3.6	4	5.5	ms
FLASH mass erase time	t_{MErase}	4	—	—	ms
FLASH PGM/ERASE to HVEN setup time	t_{NVS}	10	—	—	µs
FLASH high-voltage hold time	t_{NVH}	5	—	—	µs
FLASH high-voltage hold time (mass erase)	t_{NVHL}	100	—	—	µs
FLASH program hold time	t_{PGS}	5	—	—	µs
FLASH program time	t_{PROG}	30	—	40	µs
FLASH return to read time	t_{RCV}(4)	1	—	—	µs
FLASH cumulative program HV period	t_{HV}(5)	—	—	4	ms
FLASH endurance(6)	—	10 k	100 k	—	Cycles
FLASH data retention time(7)	—	15	100	—	Years

1. Typical values are for reference only and are not tested in production.
2. Values are based on characterization results, not tested in production.
3. f_{Read} is defined as the frequency range for which the FLASH memory can be read.
4. t_{RCV} is defined as the time it needs before the FLASH can be read after turning off the high voltage charge pump, by clearing HVEN to 0.
5. t_{HV} is defined as the cumulative high voltage programming time to the same row before next erase. t_{HV} must satisfy this condition: $t_{NVS} + t_{NVH} + t_{PGS} + (t_{PROG} \times 32) \leq t_{HV}$ maximum.
6. Typical endurance was evaluated for this product family. For additional information on how Freescale defines *Typical Endurance*, please refer to Engineering Bulletin EB619.
7. Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 C using the Arrhenius equation. For additional information on how Freescale defines *Typical Data Retention*, please refer to Engineering Bulletin EB618.