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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347epmc-gs-614e1

Contents

3. Pin Description

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
1 to 4	99 to 2	P24 to P27	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Trigger input pins for input captures.
5	3	P30	G	General purpose I/O pin.The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Trigger input pin for input capture.
6	4	P31	G	General purpose I/O pin.The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		$\overline{RD}$		External read strobe output pin. This function is enabled when the external bus is enabled.
		IN5		Trigger input pin for input capture.
7	5	P32	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the WR/WRL pin output is disabled.
		$\overline{WR}$ / $\overline{WRL}$		Write strobe output pin for the external data bus. This function is enabled when both the external bus and the WR/WRL pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
		INT10R		External interrupt request input pin.
8	6	P33	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or when the WRH pin output is disabled.
		$\overline{WRH}$		Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101)
		X0A, X1A	B	Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102)
15	13	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
16	14	V_{SS}	—	GND pin
17	15	C	K	This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 µF.
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture.
		RX1		RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only)
		INT9R		External interrupt request input pin

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter
35	33	AV_{SS}	K	Analog GND pin for the A/D Converter
36 to 43	34 to 41	P60 to P67	I	General purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
44	42	V_{SS}	—	GND pin
45 to 50	43 to 48	P70 to P75	I	General purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT0 to INT5		External interrupt request input pins
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	$\overline{RST}$	E	Reset input pin
55, 56	53, 54	P76, P77	I	General purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT6, INT7		External interrupt request input pins
57	55	P80	F	General purpose I/O pin.
		TIN0		Event input pin for the reload timer
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin
58	56	P81	F	General purpose I/O pin.
		TOT0		Output pin for the reload timer
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin
59	57	P82	M	General purpose I/O pin.
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer
		INT14R		External interrupt request input pin
60	58	P83	F	General purpose I/O pin.
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
96	94	P17	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
97 to 100	95 to 98	P20 to P23	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9,PPGB,PPGD,PPGF		Output pins for PPGs

1 : FPT-100P-M06

2 : FPT-100P-M20

3 : For I/O circuit type, refer to “I/O Circuit Type”.

Address	Register	Abbreviation	Access	Resource name	Initial value
$0000A5_H$	Automatic Ready Function Select Register	ARSR	W	External Memory Access	$0011XX00_B$
$0000A6_H$	External Address Output Control Register	HACR	W		00000000_B
$0000A7_H$	Bus Control Signal Selection Register	ECSR	W		$0000000X_B$
$0000A8_H$	Watchdog Control Register	WDTC	R,W	Watchdog Timer	$XXXXX111_B$
$0000A9_H$	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	$1XX00100_B$
$0000AA_H$	Watch Timer Control Register	WTC	R,R/W	Watch Timer	$1X001000_B$
$0000AB_H$	Reserved				
$0000AC_H$	DMA Enable L Register	DERL	R/W	DMA	00000000_B
$0000AD_H$	DMA Enable H Register	DERH	R/W		00000000_B
$0000AE_H$	Flash Control Status Register (Flash memory devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	$000X0000_B$
$0000AF_H$	Reserved				
$0000B0_H$	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111_B
$0000B1_H$	Interrupt Control Register 01	ICR01	W,R/W		00000111_B
$0000B2_H$	Interrupt Control Register 02	ICR02	W,R/W		00000111_B
$0000B3_H$	Interrupt Control Register 03	ICR03	W,R/W		00000111_B
$0000B4_H$	Interrupt Control Register 04	ICR04	W,R/W		00000111_B
$0000B5_H$	Interrupt Control Register 05	ICR05	W,R/W		00000111_B
$0000B6_H$	Interrupt Control Register 06	ICR06	W,R/W		00000111_B
$0000B7_H$	Interrupt Control Register 07	ICR07	W,R/W		00000111_B
$0000B8_H$	Interrupt Control Register 08	ICR08	W,R/W		00000111_B
$0000B9_H$	Interrupt Control Register 09	ICR09	W,R/W		00000111_B
$0000BA_H$	Interrupt Control Register 10	ICR10	W,R/W		00000111_B
$0000BB_H$	Interrupt Control Register 11	ICR11	W,R/W		00000111_B
$0000BC_H$	Interrupt Control Register 12	ICR12	W,R/W		00000111_B
$0000BD_H$	Interrupt Control Register 13	ICR13	W,R/W		00000111_B
$0000BE_H$	Interrupt Control Register 14	ICR14	W,R/W		00000111_B
$0000BF_H$	Interrupt Control Register 15	ICR15	W,R/W		00000111_B
$0000C0_H$	D/A Converter Data 0	DAT0	R/W	D/A Converter	$XXXXXXXX_B$
$0000C1_H$	D/A Converter Data 1	DAT1	R/W		$XXXXXXXX_B$
$0000C2_H$	D/A Control 0	DACR0	R/W		$XXXXXXX0_B$
$0000C3_H$	D/A Control 1	DACR1	R/W		$XXXXXXX0_B$

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Address	Register	Abbreviation	Access	Resource name	Initial value
007970_H	I^2C Bus Status Register 0	IBSR0	R	I^2C Interface 0	00000000_B
007971_H	I^2C Bus Control Register 0	IBCR0	W,R/W		00000000_B
007972_H	I^2C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000_B
007973_H		ITBAH0	R/W		00000000_B
007974_H	I^2C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111_B
007975_H		ITMKH0	R/W		00111111_B
007976_H	I^2C 7-bit Slave Address Register 0	ISBA0	R/W		00000000_B
007977_H	I^2C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111_B
007978_H	I^2C Data Register 0	IDAR0	R/W		00000000_B
007979_H, $00797A_H$	Reserved				
$00797B_H$	I^2C Clock Control Register 0	ICCR0	R/W	I^2C Interface 0	00011111_B
$00797C_H$ to $00797F_H$	Reserved				
007980_H	I^2C Bus Status Register 1	IBSR1	R	I^2C Interface 1	00000000_B
007981_H	I^2C Bus Control Register 1	IBCR1	W,R/W		00000000_B
007982_H	I^2C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000_B
007983_H		ITBAH1	R/W		00000000_B
007984_H	I^2C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111_B
007985_H		ITMKH1	R/W		00111111_B
007986_H	I^2C 7-bit Slave Address Register 1	ISBA1	R/W		00000000_B
007987_H	I^2C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111_B
007988_H	I^2C Data Register 1	IDAR1	R/W		00000000_B
007989_H, $00798A_H$	Reserved				
$00798B_H$	I^2C Clock Control Register 1	ICCR1	R/W	I^2C Interface 1	00011111_B
$00798C_H$ to $0079C1_H$	Reserved				
$0079C2_H$	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	$0001X000_B$
$0079C3_H$ to $0079DF_H$	Reserved				

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List of Control Registers (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007B00_H$	$007D00_H$	Control Status Register	CSR	R/W, W R/W, R	$0XXXX0X1_B$ $00XXX000_B$
$007B01_H$	$007D01_H$				
$007B02_H$	$007D02_H$	Last Event Indicator Register	LEIR	R/W	$000X0000_B$ $XXXXXXXX_B$
$007B03_H$	$007D03_H$				
$007B04_H$	$007D04_H$	Receive And Transmit Error Counter	RTEC	R	00000000_B 00000000_B
$007B05_H$	$007D05_H$				
$007B06_H$	$007D06_H$	Bit Timing Register	BTR	R/W	11111111_B $X1111111_B$
$007B07_H$	$007D07_H$				
$007B08_H$	$007D08_H$	IDE Register	IDER	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B09_H$	$007D09_H$				
$007B0A_H$	$007D0A_H$	Transmit RTR Register	TRTRR	R/W	00000000_B 00000000_B
$007B0B_H$	$007D0B_H$				
$007B0C_H$	$007D0C_H$	Remote Frame Receive Waiting Register	RFWTR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B0D_H$	$007D0D_H$				
$007B0E_H$	$007D0E_H$	Transmit Interrupt Enable Register	TIER	R/W	00000000_B 00000000_B
$007B0F_H$	$007D0F_H$				
$007B10_H$	$007D10_H$	Acceptance Mask Select Register	AMSR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B11_H$	$007D11_H$				
$007B12_H$	$007D12_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B13_H$	$007D13_H$				
$007B14_H$	$007D14_H$	Acceptance Mask Register 0	AMR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B15_H$	$007D15_H$				
$007B16_H$	$007D16_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B17_H$	$007D17_H$				
$007B18_H$	$007D18_H$	Acceptance Mask Register 1	AMR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B19_H$	$007D19_H$				
$007B1A_H$	$007D1A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B1B_H$	$007D1B_H$				

List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A40_H$	$007C40_H$	ID Register 8	IDR8	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A41_H$	$007C41_H$				
$007A42_H$	$007C42_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A43_H$	$007C43_H$				
$007A44_H$	$007C44_H$	ID Register 9	IDR9	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A45_H$	$007C45_H$				
$007A46_H$	$007C46_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A47_H$	$007C47_H$				
$007A48_H$	$007C48_H$	ID Register 10	IDR10	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A49_H$	$007C49_H$				
$007A4A_H$	$007C4A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4B_H$	$007C4B_H$				
$007A4C_H$	$007C4C_H$	ID Register 11	IDR11	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4D_H$	$007C4D_H$				
$007A4E_H$	$007C4E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4F_H$	$007C4F_H$				
$007A50_H$	$007C50_H$	ID Register 12	IDR12	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A51_H$	$007C51_H$				
$007A52_H$	$007C52_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A53_H$	$007C53_H$				
$007A54_H$	$007C54_H$	ID Register 13	IDR13	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A55_H$	$007C55_H$				
$007A56_H$	$007C56_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A57_H$	$007C57_H$				
$007A58_H$	$007C58_H$	ID Register 14	IDR14	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A59_H$	$007C59_H$				
$007A5A_H$	$007C5A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5B_H$	$007C5B_H$				
$007A5C_H$	$007C5C_H$	ID Register 15	IDR15	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5D_H$	$007C5D_H$				
$007A5E_H$	$007C5E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5F_H$	$007C5F_H$				

10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI^{2}OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC$_H$	—	—
INT9 instruction	N	—	#09	FFFFD8$_H$	—	—
Exception	N	—	#10	FFFFD4$_H$	—	—
CAN 0 RX	N	—	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N	—	#12	FFFFCC$_H$		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4$_H$		
CAN 2 RX / I^{2}C0	N	—	#15	FFFFC0$_H$	ICR02	0000B2$_H$
CAN 2 TX/NS	N	—	#16	FFFFBC$_H$		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8$_H$	ICR03	0000B3$_H$
16-bit Reload Timer 1	Y1	1	#18	FFFFB4$_H$		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit Reload Timer 3	Y1	—	#20	FFFFAC$_H$		
PPG 0/1/4/5	N	—	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG 2/3/6/7	N	—	#22	FFFFA4$_H$		
PPG 8/9/C/D	N	—	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG A/B/E/F	N	—	#24	FFFF9C$_H$		
Time Base Timer	N	—	#25	FFFF98$_H$	ICR07	0000B7$_H$
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94$_H$		
Watch Timer	N	—	#27	FFFF90$_H$	ICR08	0000B8$_H$
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C$_H$		
A/D Converter	Y1	5	#29	FFFF88$_H$	ICR09	0000B9$_H$
Free-run Timer 0 / Free-run Timer 1	N	—	#30	FFFF84$_H$		
Input Capture 4/5 / I^{2}C1	Y1	6	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C$_H$		
Input Capture 0 to 3	Y1	8	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output Compare 2/3/6/7	Y1	9	#34	FFFF74$_H$		
UART 0 RX	Y2	10	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART 0 TX	Y1	11	#36	FFFF6C$_H$		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64$_H$		

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Interrupt cause	EI^{2}OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX / UART 4 RX	Y2	14	#39	$FFFF60_H$	ICR14	$0000BE_H$
UART 2 TX / UART 4 TX	Y1	15	#40	$FFFF5C_H$		
Flash Memory	N	——	#41	$FFFF58_H$	ICR15	$0000BF_H$
Delayed Interrupt	N	——	#42	$FFFF54_H$		

Y1 : Usable
Y2 : Usable, with EI^{2}OS stop function
N : Unusable

Note:
- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
- When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

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(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	−1	—	+1	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Except Flash memory devices
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	55	70	mA	
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At writing Flash memory.	—	70	85	mA	Flash memory devices
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At erasing Flash memory.	—	75	90	mA	Flash memory devices
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 24 MHz, In Sleep mode.	—	25	35	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, In Main Timer mode	—	0.3	0.8	mA	
	$I_{CTSPLL6}$		V_{CC} = 5.0 V, Internal frequency : 24 MHz, In PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		V_{CC} = 5.0 V Internal frequency : 8 kHz, In sub operation T_A = +25°C	—	70	140	µA	
	I_{CCLS}		V_{CC} = 5.0 V Internal frequency : 8 kHz, In sub sleep T_A = +25°C	—	20	50	µA	
	I_{CCT}		V_{CC} = 5.0 V Internal frequency : 8 kHz, In watch mode T_A = +25°C	—	10	35	µA	
	I_{CCH}		V_{CC} = 5.0 V, In Stop mode, T_A = +25°C	—	7	25	µA	
Input capacitance	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}	—	—	5	15	pF	

* : The power supply current is measured with an external clock.

11.4 AC Characteristics

11.4.1 Clock Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP}≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

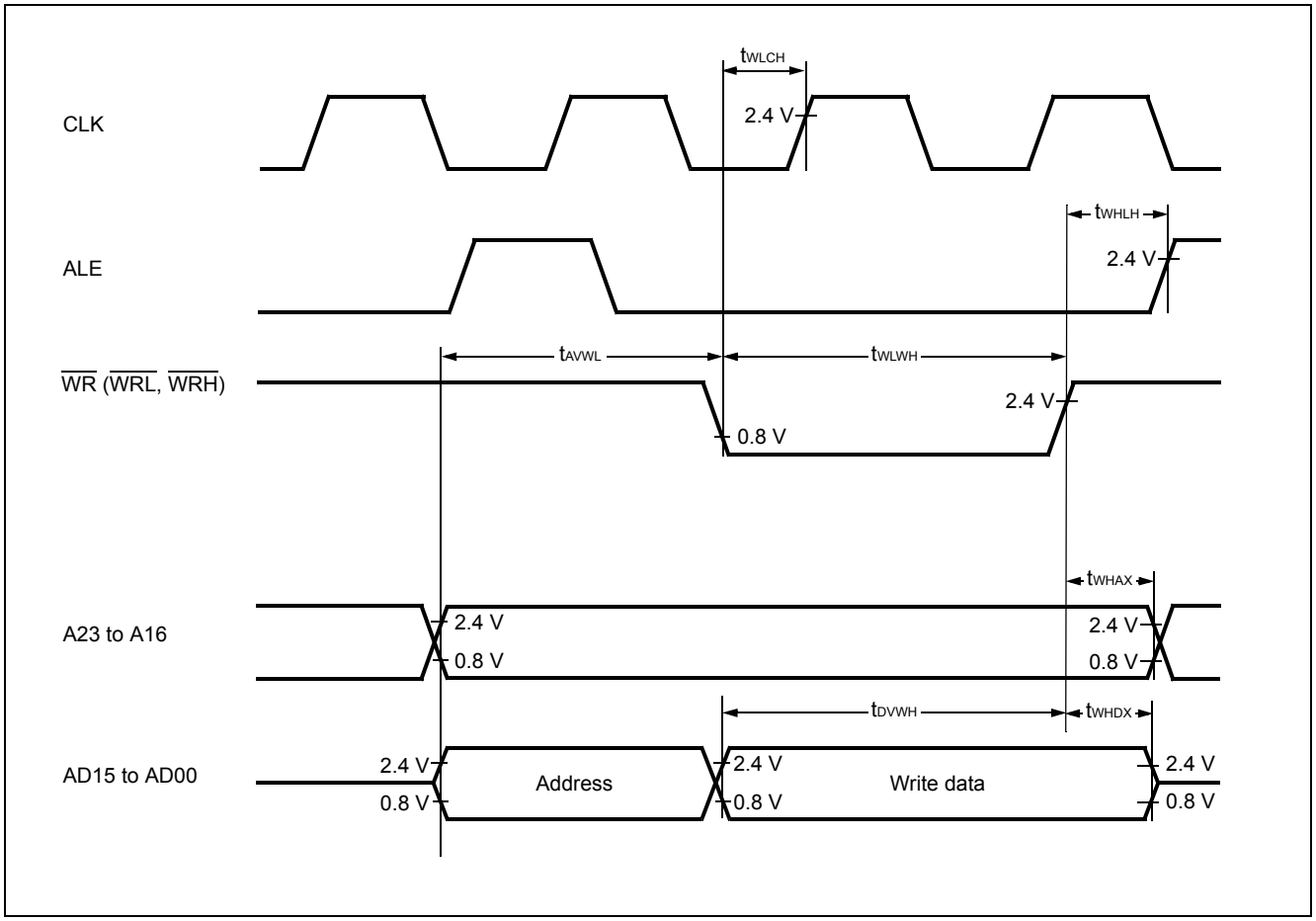
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	When using an oscillation circuit
			4	—	16	MHz	PLL multiplied by 1 When using an oscillation circuit
			4	—	12	MHz	PLL multiplied by 2 When using an oscillation circuit
			4	—	8	MHz	PLL multiplied by 3 When using an oscillation circuit
			4	—	6	MHz	PLL multiplied by 4 When using an oscillation circuit
			—	—	4	MHz	PLL multiplied by 6 When using an oscillation circuit
			3	—	24	MHz	When using an external clock*
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	µs	When using sub clock

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in “Relation between the external clock frequency and machine clock frequency”.

11.4.6 Bus Timing (Write)

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{WR}$	—	t_{CP}−15	—	ns
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		3 t_{CP}/2 − 20	—	ns
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		3 t_{CP}/2 − 20	—	ns
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	—	ns
$\overline{WR}$ ↑ → Address valid time	t_{WHAX}	A23 to A16, $\overline{WR}$		t_{CP}/2 − 10	—	ns
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 − 15	—	ns
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 − 15	—	ns



11.4.9 LIN-UART0/1/2/3

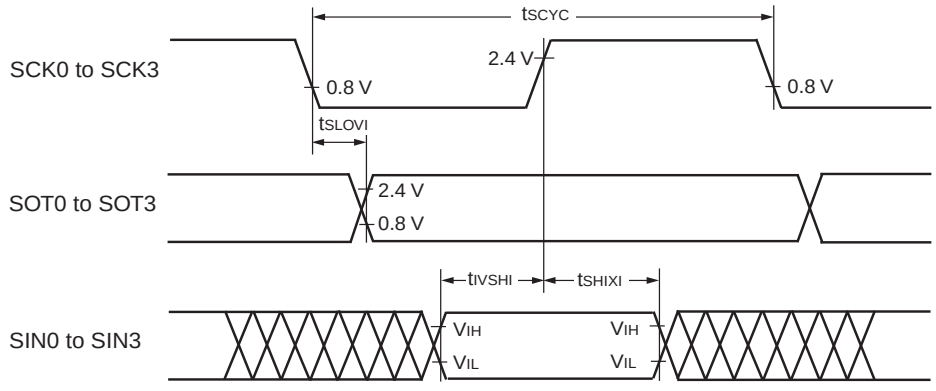
■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0**

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		−50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock “L” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “H” pulse width	t_{SLSH}	SCK0 to SCK3		t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SIN0 to SIN3		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

Note:
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

- Internal Shift Clock Mode

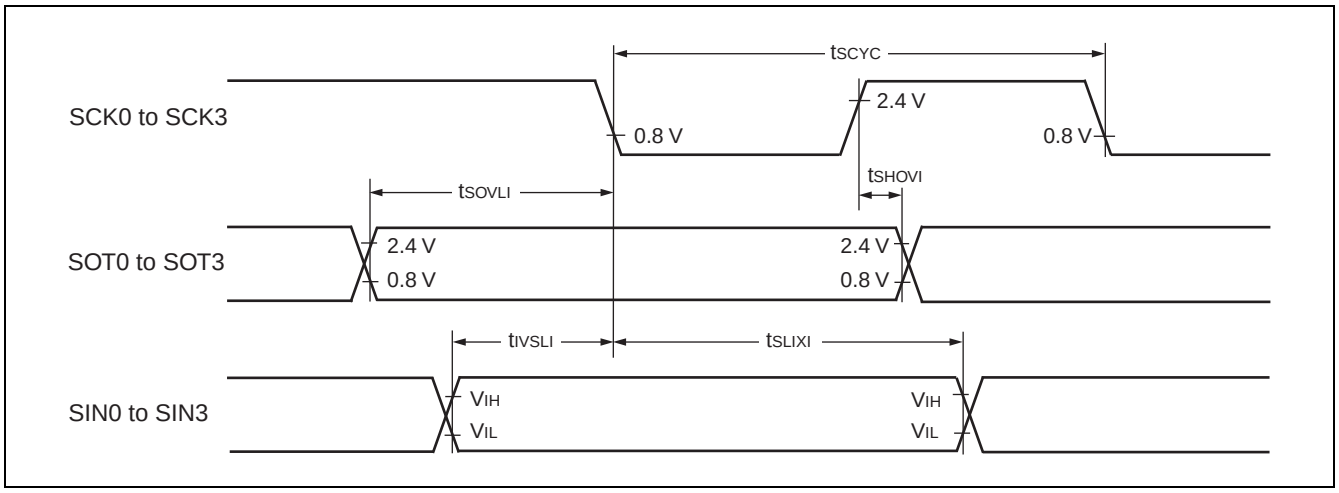


■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1**

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

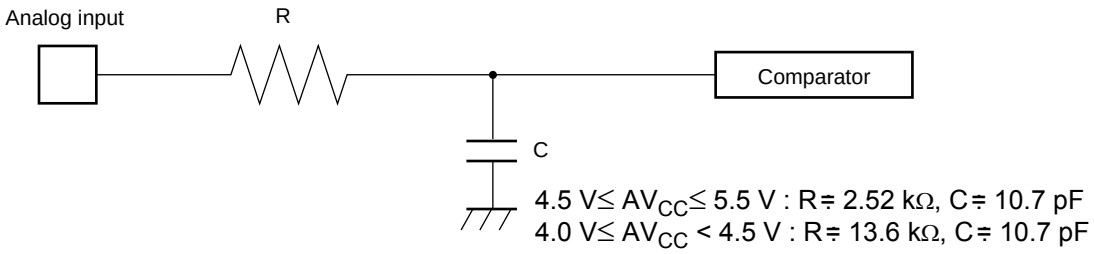
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		−50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} − 70	—	ns

Note:
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".



If the output impedance of the external circuit is too high, a sampling period for an analog voltage may be insufficient.

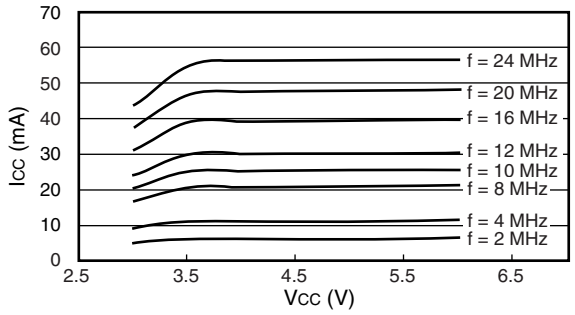
- Analog input circuit model



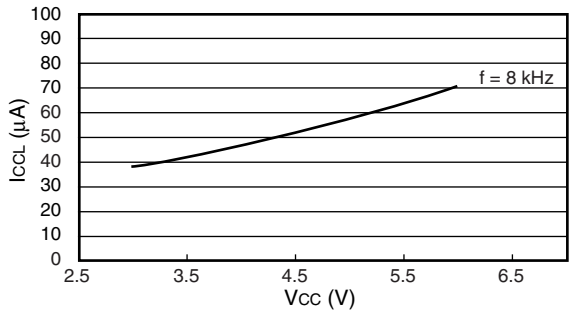
Note: : Use the values in the figure only as a guideline.

■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

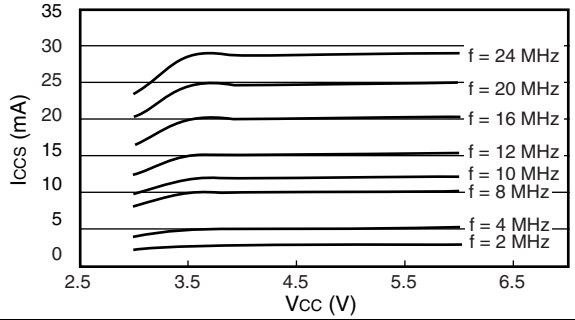
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



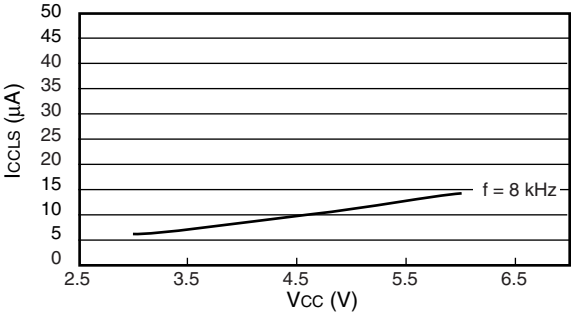
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



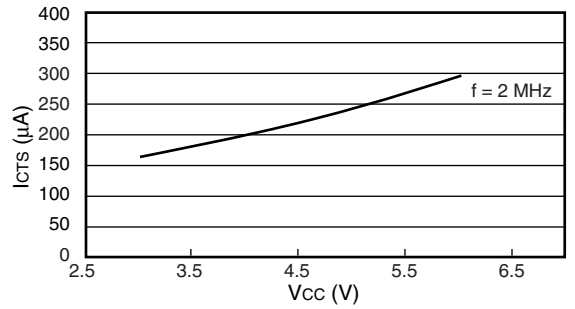
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



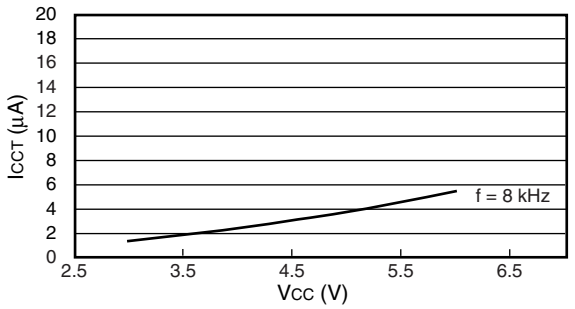
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



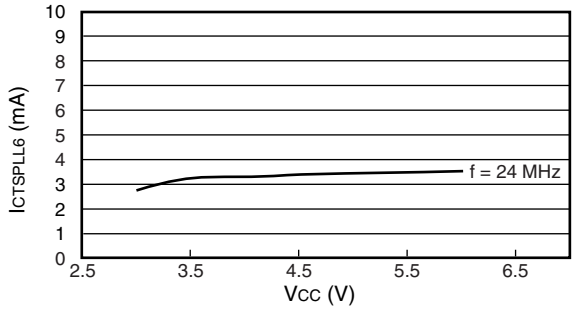
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



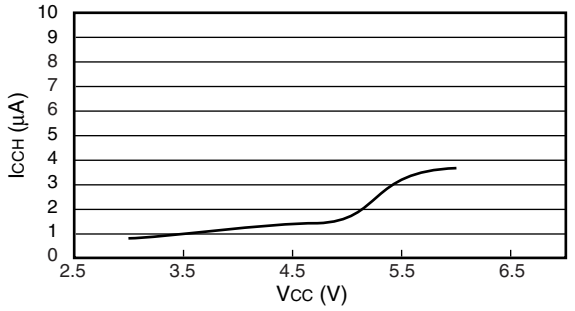
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency

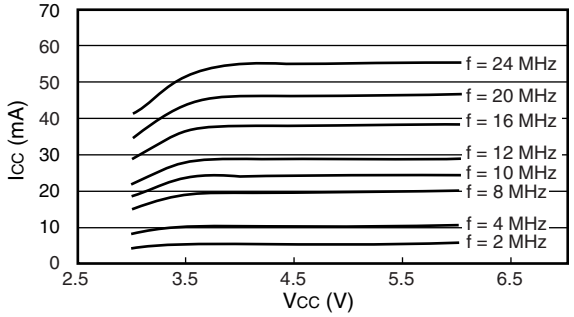


$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

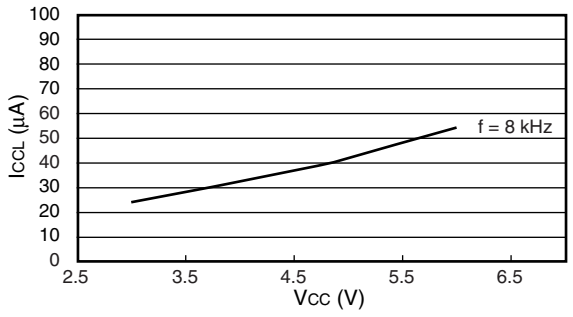


■ MB90347E, MB90347ES, MB90347CE, MB90347CES

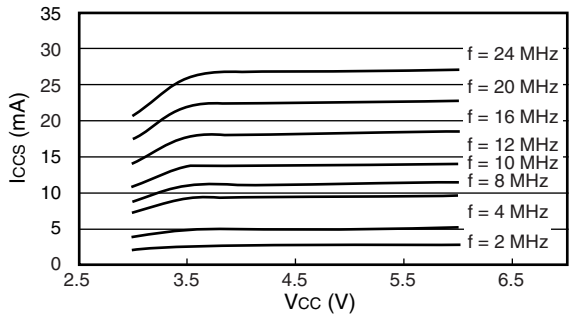
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



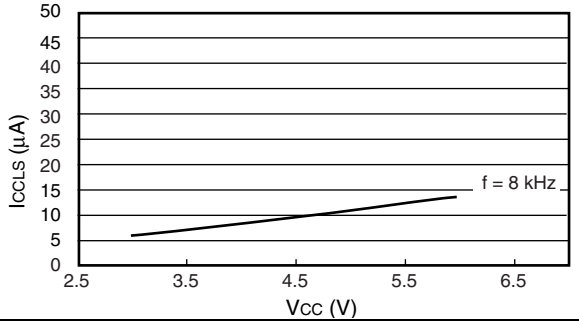
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



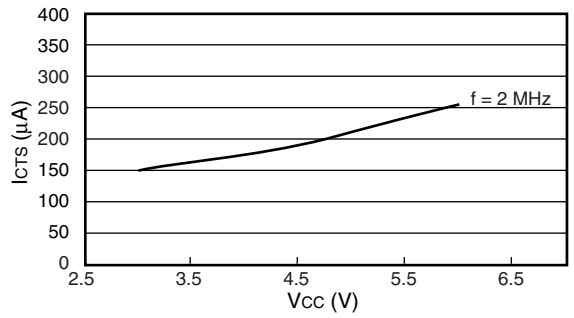
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



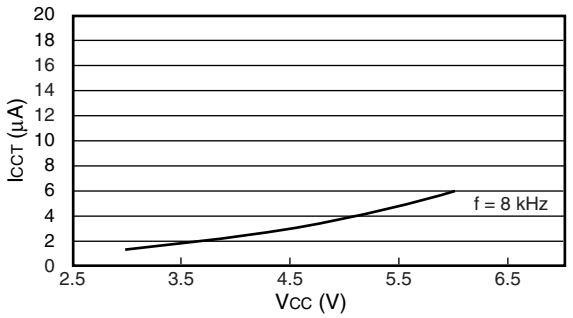
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



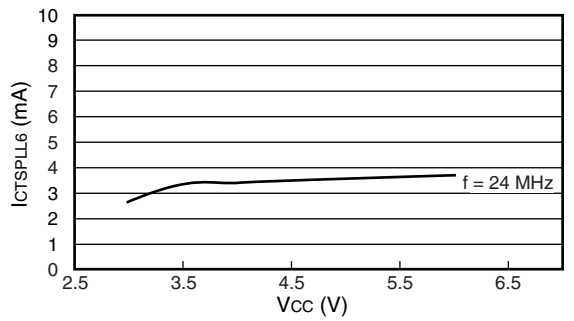
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



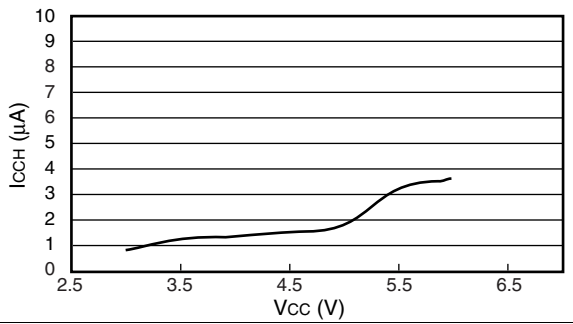
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped



(Continued)

Part number	Package	Remarks
MB90346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90346ESPF		
MB90346CEPF		
MB90346CESPF		
MB90346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90346ESPMC		
MB90346CEPMC		
MB90346CESPMC		
MB90347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90347ESPF		
MB90347CEPF		
MB90347CESPF		
MB90347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90347ESPMC		
MB90347CEPMC		
MB90347CESPMC		
MB90348EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90348ESPF		
MB90348CEPF		
MB90348CESPF		
MB90348EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90348ESPMC		
MB90348CEPMC		
MB90348CESPMC		
MB90349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90349ESPF		
MB90349CEPF		
MB90349CESPF		
MB90349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90349ESPMC		
MB90349CEPMC		
MB90349CESPMC		
MB90V340E-101CR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation
MB90V340E-102CR		