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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

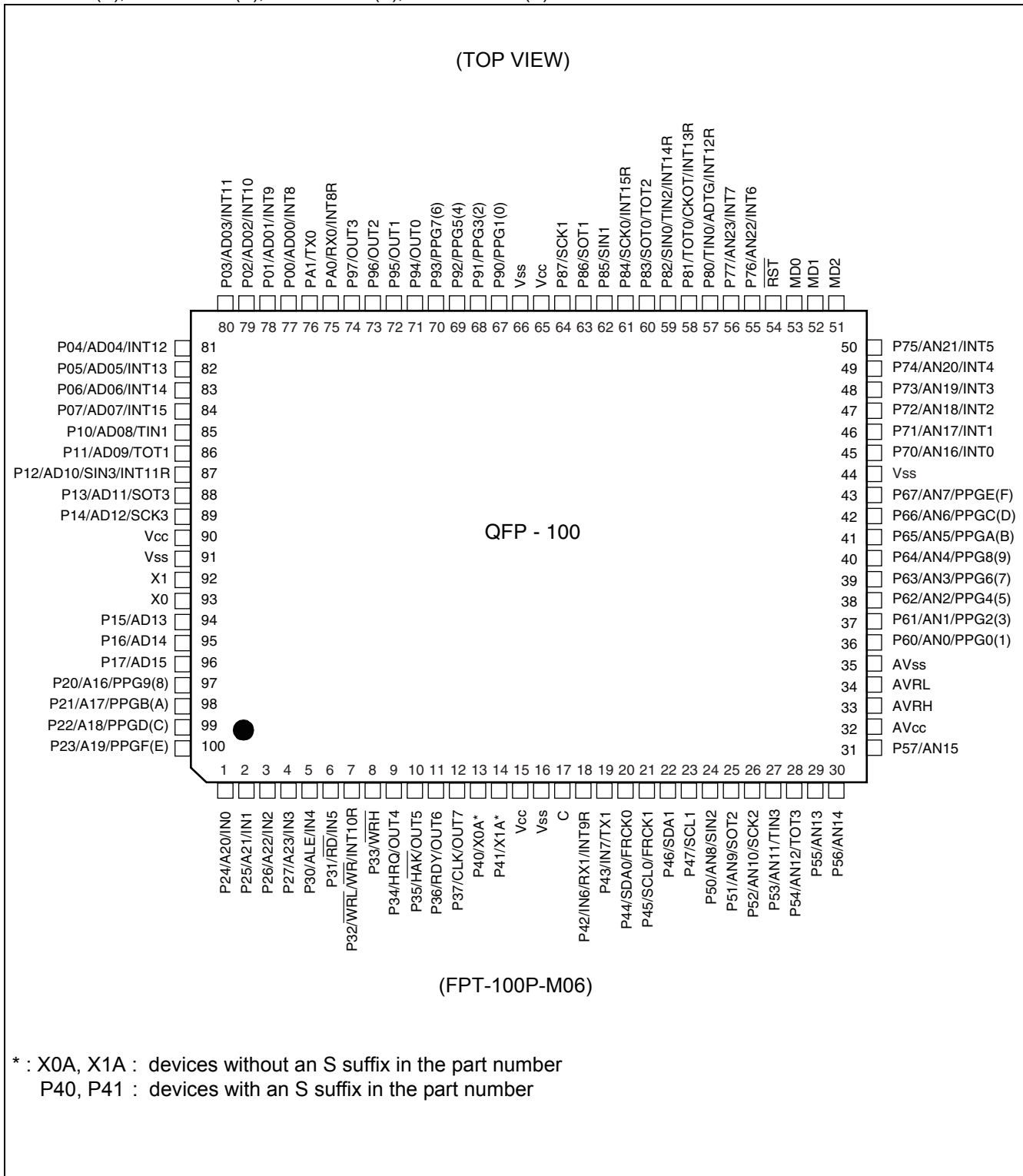
Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-248e1

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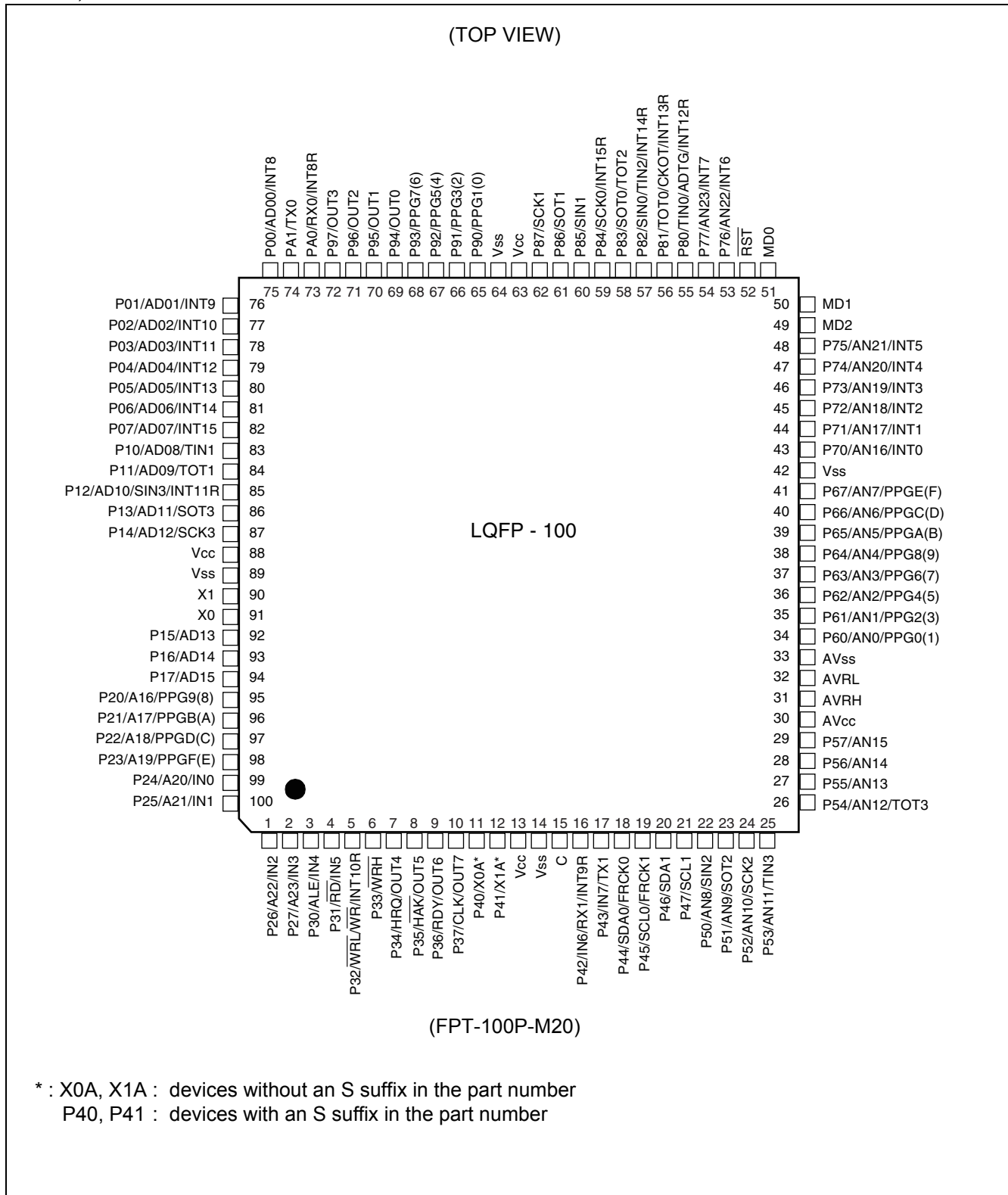
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■ MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)



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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV _{CC}	K	Analog power input pin for the A/D Converter

(Continued)

5. Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , $AVRH$, $AVRL$) and analog inputs ($AN0$ to $AN23$) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed $AVRH$ or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

6. Connection of Unused A/D Converter Pins when the A/D Converter is Used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

7. Crystal Oscillator Circuit

The X0, X1 pins and X0A, X1A pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

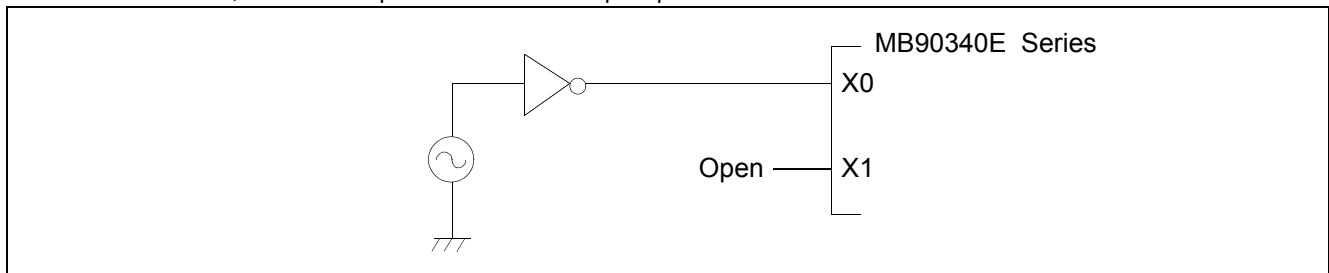
For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

8. Pull-up/down resistors

The MB90340E Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

9. Using external clock

To use an external clock, drive the X0 pin and leave the X1 pin open.



10. Precautions when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

11. Notes on operation in PLL clock mode

If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

12. Notes on Power-On

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50 μ s or more (0.2 V to 2.7 V)

MB90342E(S)/342CE(S)
MB90F342E(S)/F342CE(S)
MB90349E(S)/349CE(S)
MB90F349E(S)/F349CE(S)

MB90341E(S)/341CE(S)
MB90348E(S)/348CE(S)

MB90347E(S)/347CE(S)
MB90F347E(S)/F347CE(S)

MB90346E(S)/346CE(S)
MB90F346E(S)/F346CE(S)

000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral
	External access area		External access area		External access area		External access area
000100H		000100H		000100H	RAM 6 Kbytes	000100H	RAM 2 Kbytes
	RAM 16 Kbytes		RAM 16 Kbytes	0018FFH		0008FFH	
003FFFH		003FFFH					
007900H		007900H		007900H		007900H	
007FFFH	Peripheral	007FFFH	Peripheral	007FFFH	Peripheral	007FFFH	Peripheral
008000H		008000H		008000H		008000H	
00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)
	External access area		External access area		External access area		External access area
FC0000H							
FCFFFFH	ROM (FC bank)						
FD0000H							
FDFFFFH	ROM (FD bank)						
FE0000H		FE0000H		FE0000H		FE0000H	
FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	
FF0000H		FF0000H		FF0000H		FF0000H	
FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)

 : Not accessible

Note: :An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.

For example, when the address 00C000_H is accessed, the data at FFC000_H in ROM is actually accessed.

The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.

As a result, the image between FF8000_H and FFFFFFF_H is visible in bank 00, while the image between FF0000_H and FF7FFF_H is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
007924 _H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
007925 _H	Input Capture 2	IPCP2	R		XXXXXXXX _B
007926 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007927 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007928 _H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
007929 _H	Input Capture 4	IPCP4	R		XXXXXXXX _B
00792A _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
00792B _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
00792C _H	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
00792D _H	Input Capture 6	IPCP6	R		XXXXXXXX _B
00792E _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
00792F _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
007930 _H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
007931 _H	Output Compare 0	OCCP0	R/W		XXXXXXXX _B
007932 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007933 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007934 _H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
007935 _H	Output Compare 2	OCCP2	R/W		XXXXXXXX _B
007936 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007937 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007938 _H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX _B
007939 _H	Output Compare 4	OCCP4	R/W		XXXXXXXX _B
00793A _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793B _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793C _H	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX _B
00793D _H	Output Compare 6	OCCP6	R/W		XXXXXXXX _B
00793E _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
00793F _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
007940 _H	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000 _B
007941 _H	Timer Data 0	TCDT0	R/W		00000000 _B
007942 _H	Timer Control Status 0	TCCSL0	R/W		00000000 _B
007943 _H	Timer Control Status 0	TCCSH0	R/W		0XXXXXXXX _B
007944 _H	Timer Data 1	TCDT1	R/W	Free-run Timer 1	00000000 _B
007945 _H	Timer Data 1	TCDT1	R/W		00000000 _B
007946 _H	Timer Control Status 1	TCCSL1	R/W		00000000 _B
007947 _H	Timer Control Status 1	TCCSH1	R/W		0XXXXXXXX _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007970 _H	I ² C Bus Status Register 0	IBSR0	R	I ² C Interface 0	00000000 _B
007971 _H	I ² C Bus Control Register 0	IBCR0	W,R/W		00000000 _B
007972 _H	I ² C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000 _B
007973 _H		ITBAH0	R/W		00000000 _B
007974 _H	I ² C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111 _B
007975 _H		ITMKH0	R/W		00111111 _B
007976 _H	I ² C 7-bit Slave Address Register 0	ISBA0	R/W		00000000 _B
007977 _H	I ² C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111 _B
007978 _H	I ² C Data Register 0	IDAR0	R/W		00000000 _B
007979 _H , 00797A _H	Reserved				
00797B _H	I ² C Clock Control Register 0	ICCR0	R/W	I ² C Interface 0	00011111 _B
00797C _H to 00797F _H	Reserved				
007980 _H	I ² C Bus Status Register 1	IBSR1	R	I ² C Interface 1	00000000 _B
007981 _H	I ² C Bus Control Register 1	IBCR1	W,R/W		00000000 _B
007982 _H	I ² C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000 _B
007983 _H		ITBAH1	R/W		00000000 _B
007984 _H	I ² C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111 _B
007985 _H		ITMKH1	R/W		00111111 _B
007986 _H	I ² C 7-bit Slave Address Register 1	ISBA1	R/W		00000000 _B
007987 _H	I ² C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111 _B
007988 _H	I ² C Data Register 1	IDAR1	R/W		00000000 _B
007989 _H , 00798A _H	Reserved				
00798B _H	I ² C Clock Control Register 1	ICCR1	R/W	I ² C Interface 1	00011111 _B
00798C _H to 0079C1 _H	Reserved				
0079C2 _H	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	0001X000 _B
0079C3 _H to 0079DF _H	Reserved				

(Continued)

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Address	Register	Abbreviation	Access	Resource name	Initial value
0079E0 _H	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXX _B
0079E1 _H	Detect Address Setting 0	PADR0	R/W		XXXXXXXX _B
0079E2 _H	Detect Address Setting 0	PADR0	R/W		XXXXXXXX _B
0079E3 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E4 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E5 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E6 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E7 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E8 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E9 _H to 0079EF _H	Reserved				
0079F0 _H	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXX _B
0079F1 _H	Detect Address Setting 3	PADR3	R/W		XXXXXXXX _B
0079F2 _H	Detect Address Setting 3	PADR3	R/W		XXXXXXXX _B
0079F3 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F4 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F5 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F6 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F7 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F8 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F9 _H to 0079FF _H	Reserved				
007A00 _H to 007AFF _H	Reserved for CAN Controller 0. Refer to “CAN Controllers				
007B00 _H to 007BFF _H	Reserved for CAN Controller 0. Refer to “CAN Controllers”				
007C00 _H to 007CFF _H	Reserved for CAN Controller 1. Refer to “CAN Controllers”				
007D00 _H to 007DFF _H	Reserved for CAN Controller 1. Refer to “CAN Controllers”				
007E00 _H to 007FFF _H	Reserved				

Note:

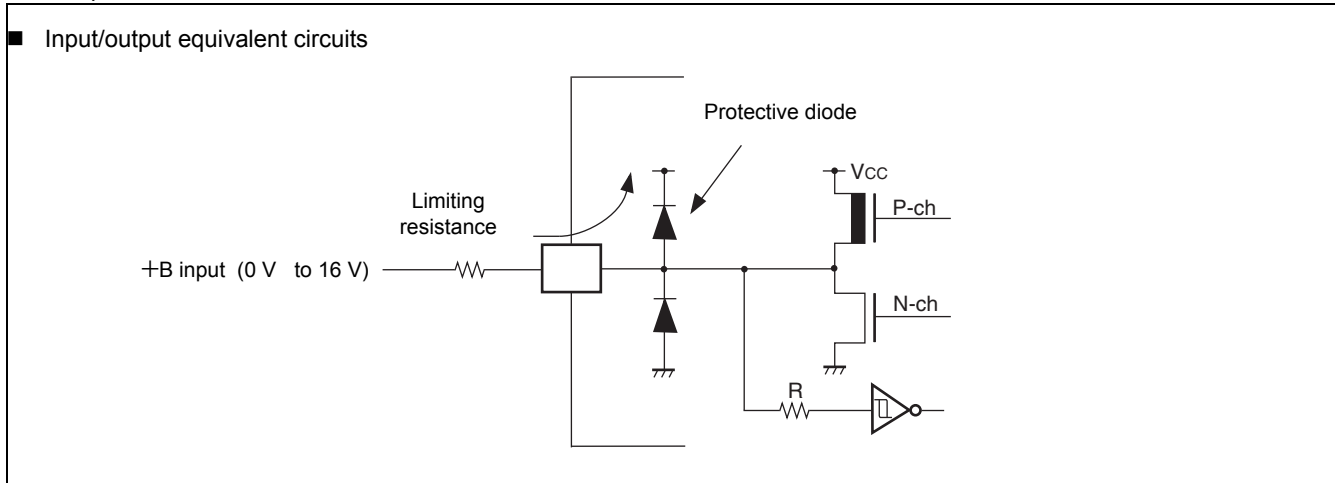
- Initial value of “X” represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A60 _H	007C60 _H	DLC Register 0	DLCR0	R/W	XXXXXXXX _B
007A61 _H	007C61 _H				
007A62 _H	007C62 _H				
007A63 _H	007C63 _H	DLC Register 1	DLCR1	R/W	XXXXXXXX _B
007A64 _H	007C64 _H				
007A65 _H	007C65 _H	DLC Register 2	DLCR2	R/W	XXXXXXXX _B
007A66 _H	007C66 _H				
007A67 _H	007C67 _H	DLC Register 3	DLCR3	R/W	XXXXXXXX _B
007A68 _H	007C68 _H				
007A69 _H	007C69 _H	DLC Register 4	DLCR4	R/W	XXXXXXXX _B
007A6A _H	007C6A _H				
007A6B _H	007C6B _H	DLC Register 5	DLCR5	R/W	XXXXXXXX _B
007A6C _H	007C6C _H				
007A6D _H	007C6D _H	DLC Register 6	DLCR6	R/W	XXXXXXXX _B
007A6E _H	007C6E _H				
007A6F _H	007C6F _H	DLC Register 7	DLCR7	R/W	XXXXXXXX _B
007A70 _H	007C70 _H				
007A71 _H	007C71 _H	DLC Register 8	DLCR8	R/W	XXXXXXXX _B
007A72 _H	007C72 _H				
007A73 _H	007C73 _H	DLC Register 9	DLCR9	R/W	XXXXXXXX _B
007A74 _H	007C74 _H				
007A75 _H	007C75 _H	DLC Register 10	DLCR10	R/W	XXXXXXXX _B
007A76 _H	007C76 _H				
007A77 _H	007C77 _H	DLC Register 11	DLCR11	R/W	XXXXXXXX _B
007A78 _H	007C78 _H				
007A79 _H	007C79 _H	DLC Register 12	DLCR12	R/W	XXXXXXXX _B
007A7A _H	007C7A _H				
007A7B _H	007C7B _H	DLC Register 13	DLCR13	R/W	XXXXXXXX _B
007A7C _H	007C7C _H				
007A7D _H	007C7D _H	DLC Register 14	DLCR14	R/W	XXXXXXXX _B
007A7E _H	007C7E _H				
007A7F _H	007C7F _H	DLC Register 15	DLCR15	R/W	XXXXXXXX _B

(Continued)

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:



*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

11.4 AC Characteristics

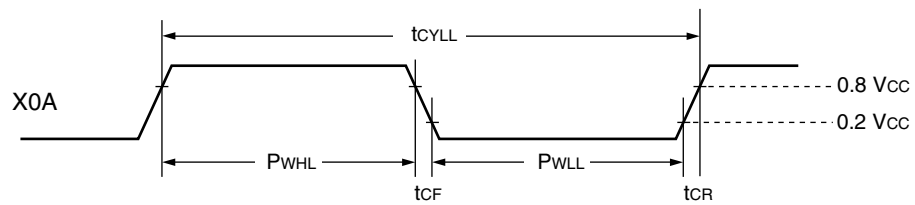
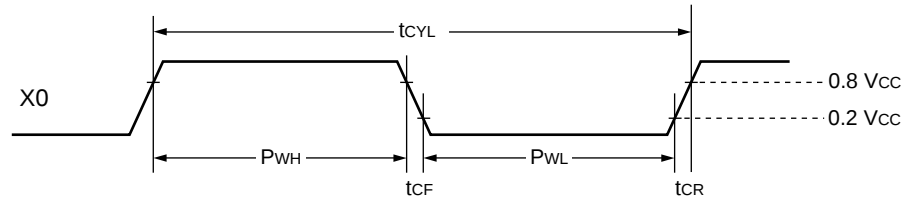
11.4.1 Clock Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	When using an oscillation circuit
			4	—	16	MHz	PLL multiplied by 1 When using an oscillation circuit
			4	—	12	MHz	PLL multiplied by 2 When using an oscillation circuit
			4	—	8	MHz	PLL multiplied by 3 When using an oscillation circuit
			4	—	6	MHz	PLL multiplied by 4 When using an oscillation circuit
			—	—	4	MHz	PLL multiplied by 6 When using an oscillation circuit
			3	—	24	MHz	When using an external clock*
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	μs	When using sub clock

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in "Relation between the external clock frequency and machine clock frequency".

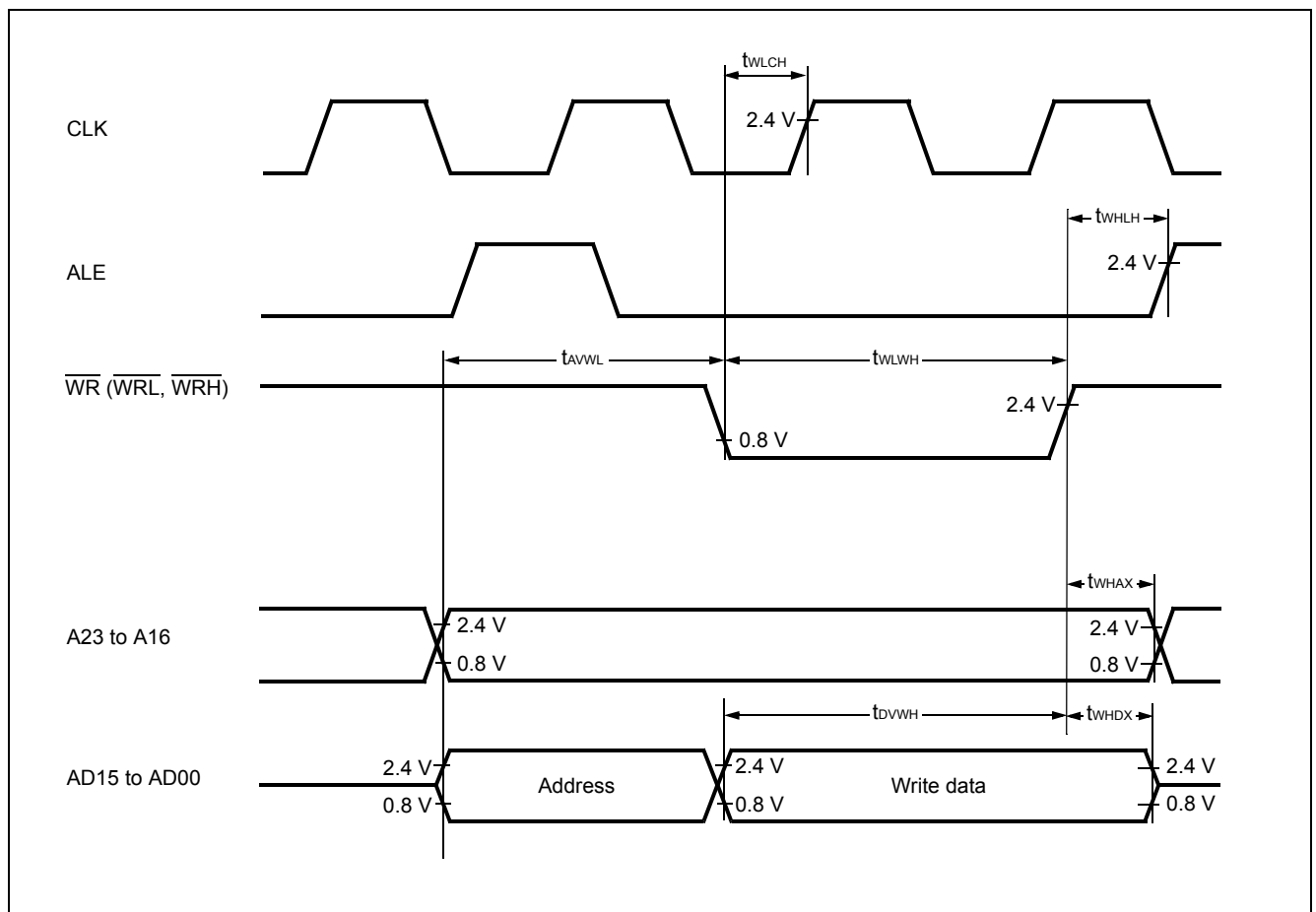
Clock Timing



11.4.6 Bus Timing (Write)

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address $\rightarrow \overline{\text{WR}} \downarrow$ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{\text{WR}}$	—	$t_{CP} - 15$	—	ns
$\overline{\text{WR}}$ pulse width	t_{WLWH}	$\overline{\text{WR}}$		$3 t_{CP}/2 - 20$	—	ns
Valid data output $\rightarrow \overline{\text{WR}} \uparrow$ time	t_{DVWH}	AD15 to AD00, $\overline{\text{WR}}$		$3 t_{CP}/2 - 20$	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ Data hold time	t_{WHDX}	AD15 to AD00, $\overline{\text{WR}}$		15	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ Address valid time	t_{WHAX}	A23 to A16, $\overline{\text{WR}}$		$t_{CP}/2 - 10$	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ ALE $\uparrow$ time	t_{WHLH}	$\overline{\text{WR}}$, ALE		$t_{CP}/2 - 15$	—	ns
$\overline{\text{WR}} \downarrow \rightarrow$ CLK $\uparrow$ time	t_{WLCH}	$\overline{\text{WR}}$, CLK		$t_{CP}/2 - 15$	—	ns



11.4.9 LIN-UART0/1/2/3

■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

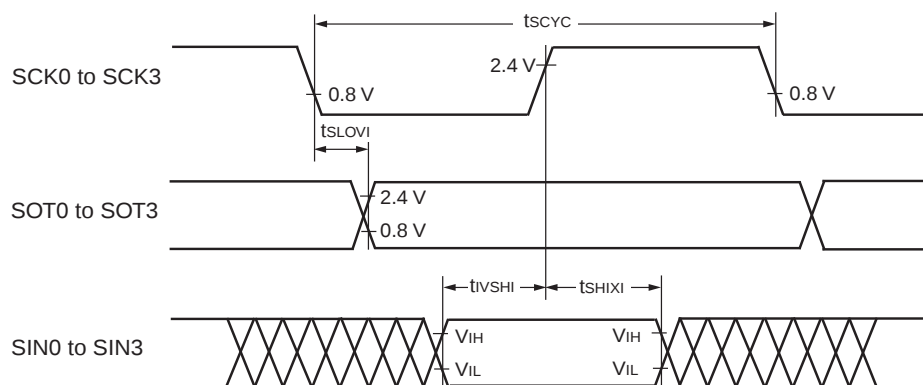
($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock "L" pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$3 t_{CP} - t_R$	—	ns
Serial clock "H" pulse width	t_{SLSH}	SCK0 to SCK3		$t_{CP} + 10$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	$2 t_{CP} + 60$	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SIN0 to SIN3		$t_{CP} + 30$	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

Note:

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “(1) Clock Timing”.

• Internal Shift Clock Mode



11.4.13 I²C Timing

(T_A = -40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V)

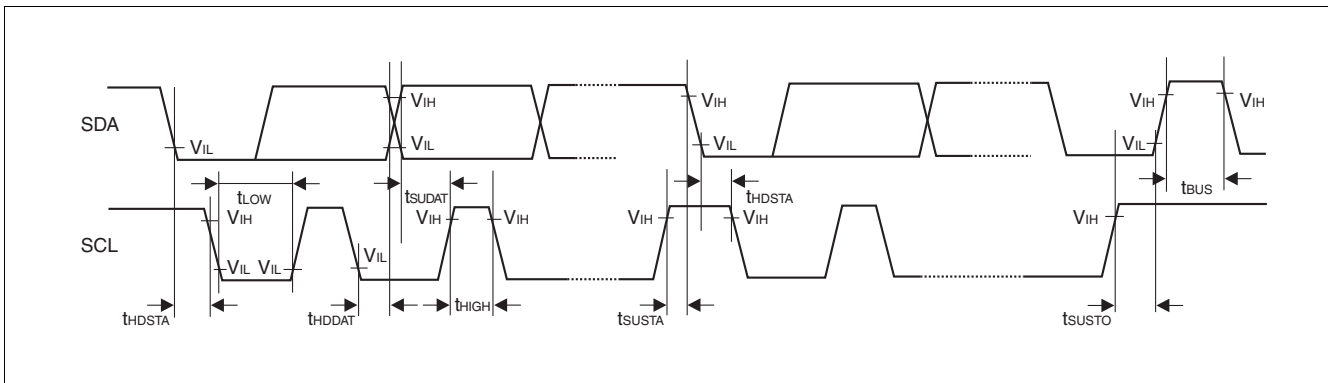
Parameter	Symbol	Condition	Standard-mode		Fast-mode* ¹		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	R = 1.7 kΩ ₂ C = 50 pF* ²	0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t _{HDSTA}		4.0	—	0.6	—	μs
"L" width of the SCL clock	t _{LOW}		4.7	—	1.3	—	μs
"H" width of the SCL clock	t _{HIGH}		4.0	—	0.6	—	μs
Set-up time (repeated) START condition SCL ↑ → SDA ↓	t _{SUSTA}		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}		0	3.45* ³	0	0.9* ⁴	μs
Data set-up time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t _{SUSTO}		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t _{BUS}		4.7	—	1.3	—	μs

*1: For use at over 100 kHz, set the machine clock to at least 6 MHz.

*2: R, C: Pull-up resistor and load capacitor of the SCL and SDA lines.

*3: The maximum t_{HDDAT} meets the requirement that it does not extend the "L" width (t_{LOW}) of the SCL signal.

*4: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.



11.5 A/D Converter

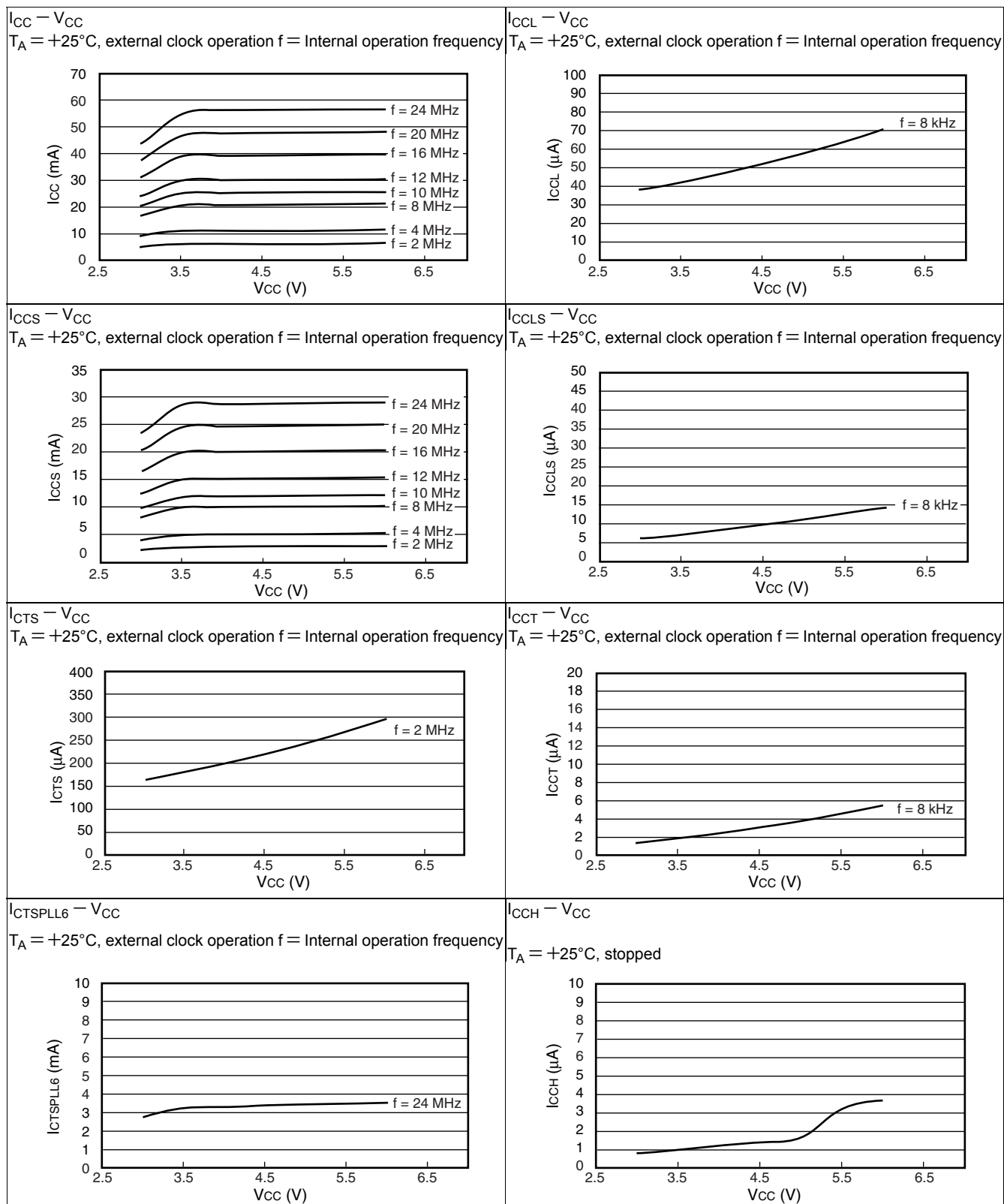
($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$, $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = \text{AV}_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential nonlinearity error	—	—	—	—	± 1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	$\text{AVRL} - 1.5 \times \text{LSB}$	$\text{AVRL} + 0.5 \times \text{LSB}$	$\text{AVRL} + 2.5 \times \text{LSB}$	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	$\text{AVRH} - 3.5 \times \text{LSB}$	$\text{AVRH} - 1.5 \times \text{LSB}$	$\text{AVRH} + 0.5 \times \text{LSB}$	V	
Compare time	—	—	1.0	—	16500	μs	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			2.0				$4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Sampling time	—	—	0.5	—	∞	μs	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			1.2				$4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Analog port input current	I_{AIN}	AN0 to AN23	-0.3	—	+0.3	μA	
Analog input voltage range	V_{AIN}	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$\text{AVRL} + 2.7$	—	AV_{CC}	V	
	—	AVRL	0	—	$\text{AVRH} - 2.7$	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage current	I_R	AVRH	—	600	900	μA	
	I_{RH}	AVRH	—	—	5	μA	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

*: If the A/D convertor is not operating, a current when CPU is stopped is applicable ($V_{CC} = \text{AV}_{CC} = \text{AVRH} = 5.0\text{ V}$).

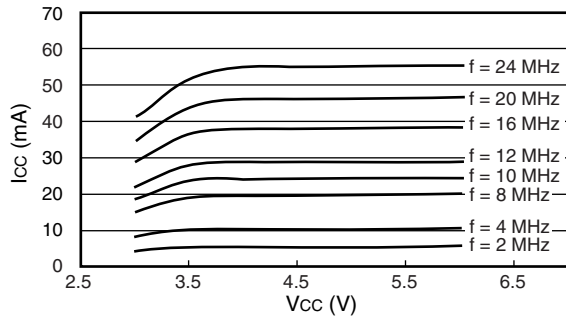
Note: : The accuracy gets worse as $|\text{AVRH} - \text{AVRL}|$ becomes smaller.

■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

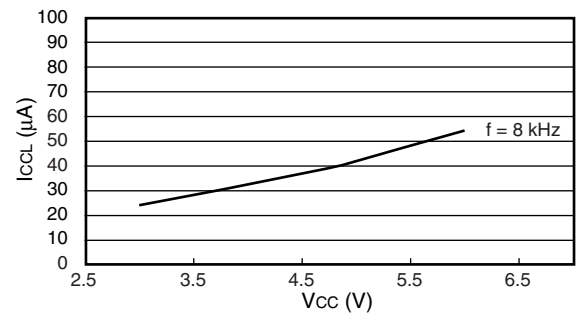


■ MB90346E, MB90346ES, MB90346CE, MB90346CES

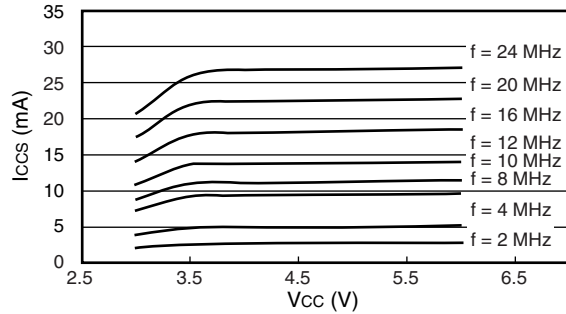
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



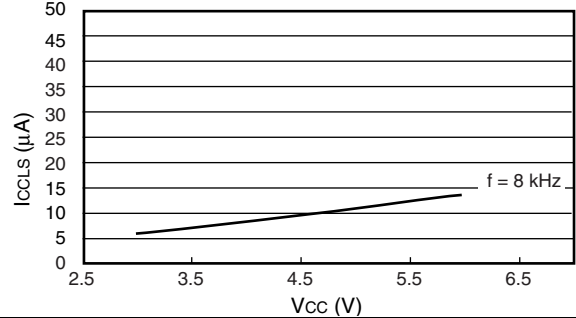
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



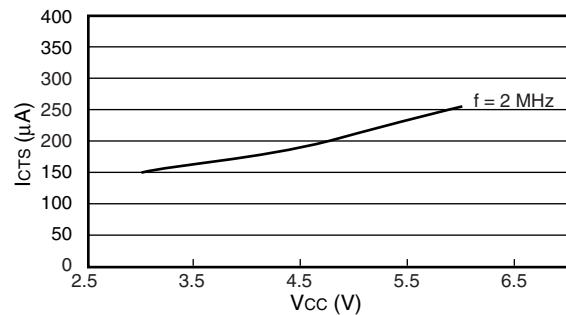
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



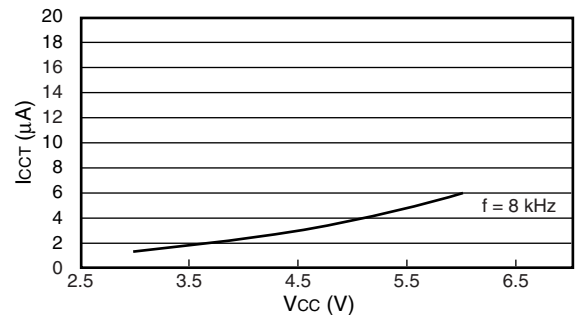
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



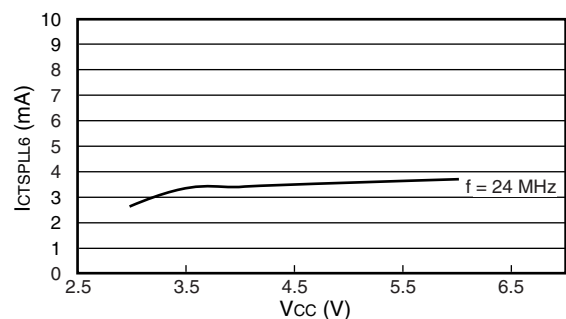
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



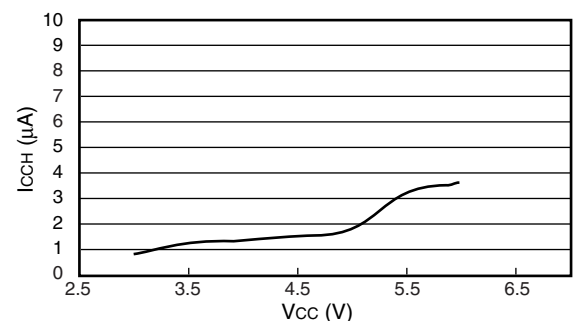
$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped



13. Ordering Information

Part number	Package	Remarks
MB90F342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F342ESPF		
MB90F342CEPF		
MB90F342CESPF		
MB90F342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F342ESPMC		
MB90F342CEPMC		
MB90F342CESPMC		
MB90F345EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F345ESPF		
MB90F345CEPF		
MB90F345CESPF		
MB90F345EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F345ESPMC		
MB90F345CEPMC		
MB90F345CESPMC		
MB90F346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F346ESPF		
MB90F346CEPF		
MB90F346CESPF		
MB90F346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F346ESPMC		
MB90F346CEPMC		
MB90F346CESPMC		

(Continued)