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What is "[Embedded - Microcontrollers](#)"?

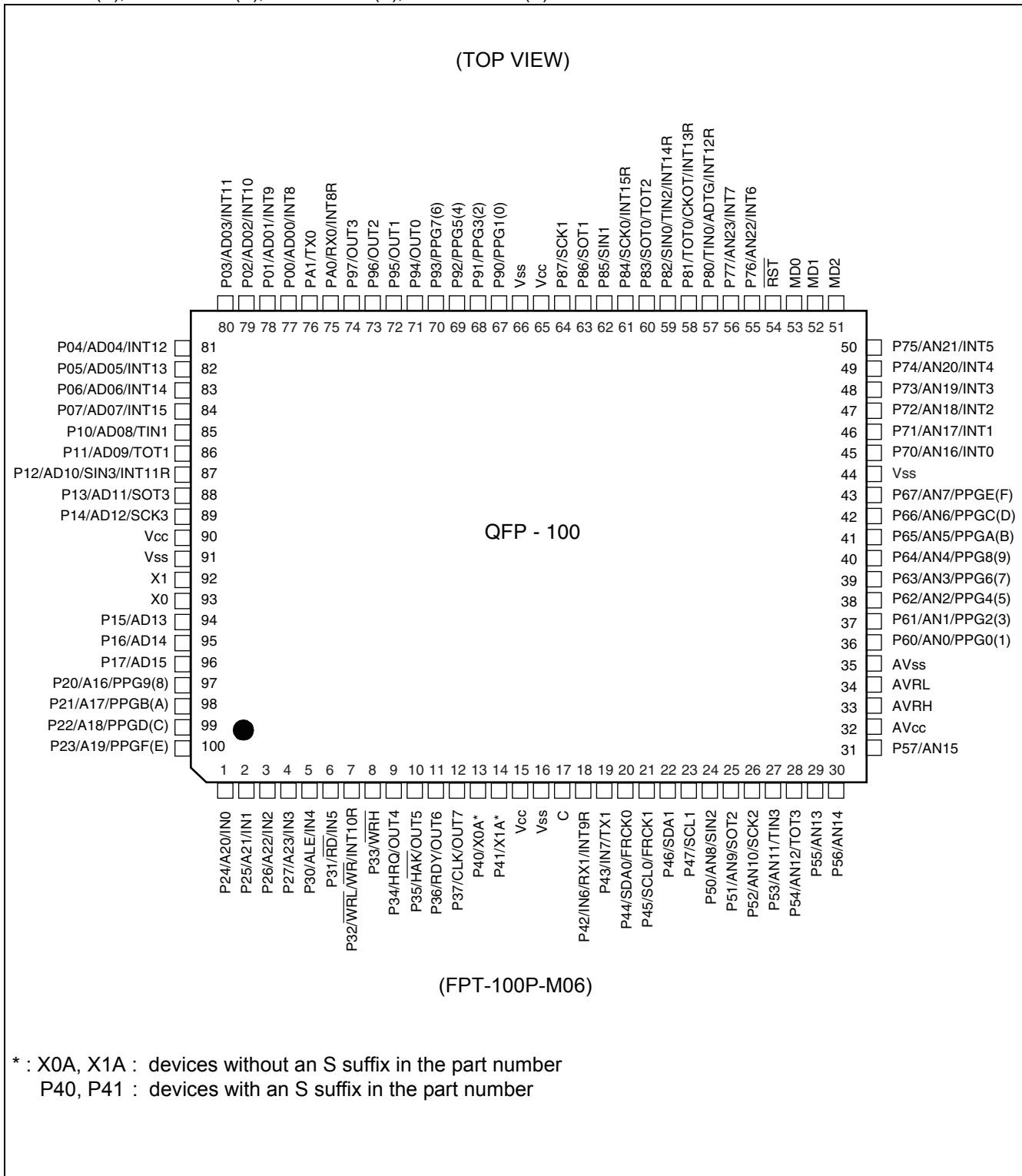
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

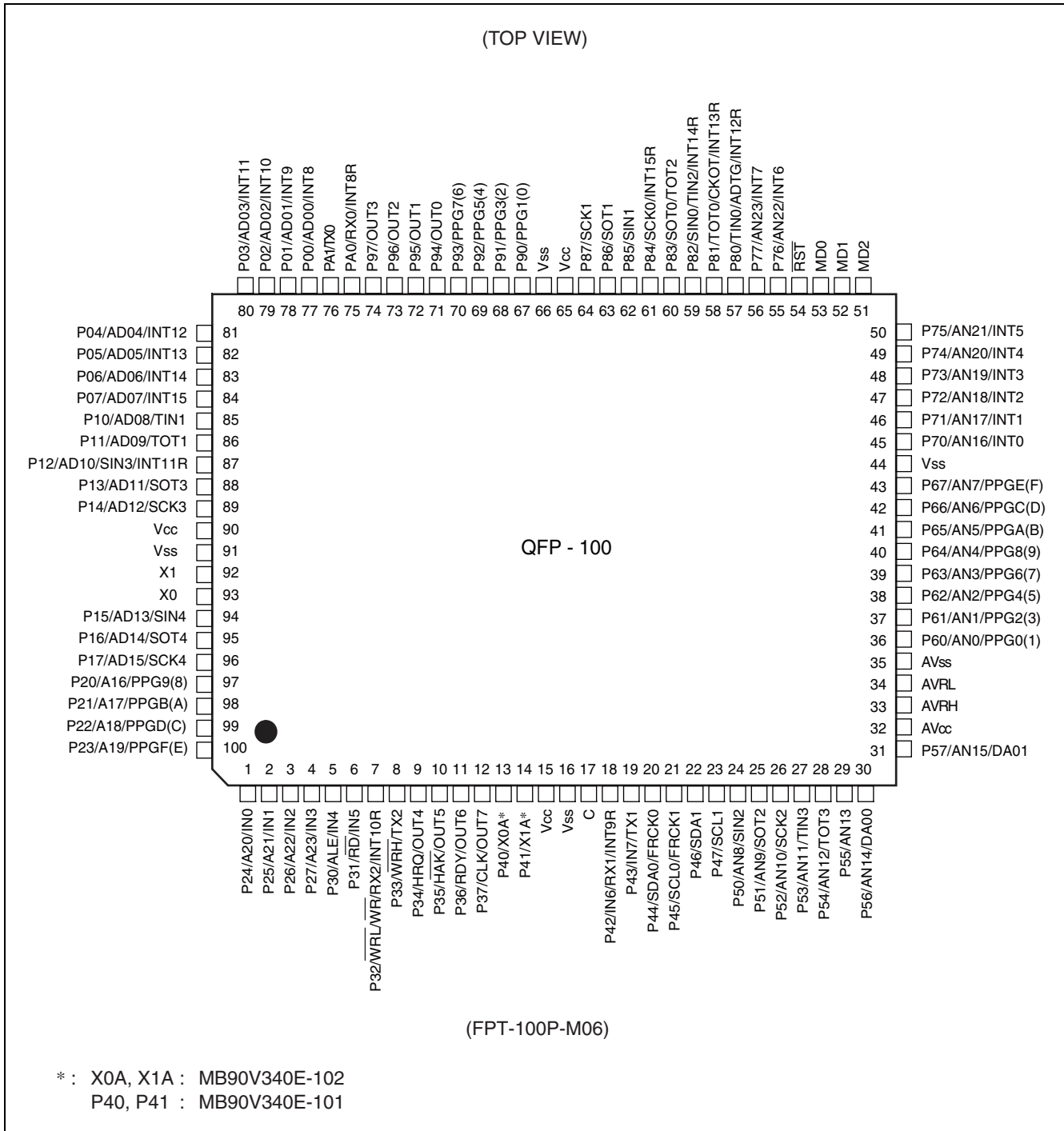
Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-277e1

■ MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)



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■ MB90V340E-101/MB90V340E-102



This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV _{CC} .
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter
35	33	AV _{SS}	K	Analog GND pin for the A/D Converter
36 to 43	34 to 41	P60 to P67	I	General purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
44	42	V _{SS}	—	GND pin
45 to 50	43 to 48	P70 to P75	I	General purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT0 to INT5		External interrupt request input pins
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	RST	E	Reset input pin
55, 56	53, 54	P76, P77	I	General purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT6, INT7		External interrupt request input pins
57	55	P80	F	General purpose I/O pin.
		TIN0		Event input pin for the reload timer
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin
58	56	P81	F	General purpose I/O pin.
		TOT0		Output pin for the reload timer
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin
59	57	P82	M	General purpose I/O pin.
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer
		INT14R		External interrupt request input pin
60	58	P83	F	General purpose I/O pin.
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
66	64	V _{SS}	—	GND pin
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pins
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pins
		OUT0 to OUT3		Waveform output pins for output compares. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin
76	74	PA1	F	General purpose I/O pin.
		TX0		TX Output pin for CAN0
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer

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MB90342E(S)/342CE(S)
MB90F342E(S)/F342CE(S)
MB90349E(S)/349CE(S)
MB90F349E(S)/F349CE(S)

MB90341E(S)/341CE(S)
MB90348E(S)/348CE(S)

MB90347E(S)/347CE(S)
MB90F347E(S)/F347CE(S)

MB90346E(S)/346CE(S)
MB90F346E(S)/F346CE(S)

000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral
	External access area		External access area		External access area		External access area
000100H		000100H		000100H	RAM 6 Kbytes	000100H	RAM 2 Kbytes
	RAM 16 Kbytes		RAM 16 Kbytes	0018FFH		0008FFH	
003FFFH		003FFFH					
007900H		007900H		007900H		007900H	
007FFFH	Peripheral	007FFFH	Peripheral	007FFFH	Peripheral	007FFFH	Peripheral
008000H		008000H		008000H		008000H	
00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)
	External access area		External access area		External access area		External access area
FC0000H							
FCFFFFH	ROM (FC bank)						
FD0000H							
FDFFFFH	ROM (FD bank)						
FE0000H		FE0000H		FE0000H		FE0000H	
FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	
FF0000H		FF0000H		FF0000H		FF0000H	
FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)

 : Not accessible

Note: :An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.

For example, when the address 00C000_H is accessed, the data at FFC000_H in ROM is actually accessed.

The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.

As a result, the image between FF8000_H and FFFFFFF_H is visible in bank 00, while the image between FF0000_H and FF7FFF_H is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
000020 _H	Serial Mode Register 0	SMR0	W,R/W	UART0	00000000 _B
000021 _H	Serial Control Register 0	SCR0	W,R/W		00000000 _B
000022 _H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000 _B
000023 _H	Serial Status Register 0	SSR0	R,R/W		00001000 _B
000024 _H	Extended Communication Control Register 0	ECCR0	R,W, R/W		000000XX _B
000025 _H	Extended Status/Control Register 0	ESCR0	R/W		00000100 _B
000026 _H	Baud Rate Generator Register 00	BGR00	R/W		00000000 _B
000027 _H	Baud Rate Generator Register 01	BGR01	R/W		00000000 _B
000028 _H	Serial Mode Register 1	SMR1	W,R/W	UART1	00000000 _B
000029 _H	Serial Control Register 1	SCR1	W,R/W		00000000 _B
00002A _H	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000 _B
00002B _H	Serial Status Register 1	SSR1	R,R/W		00001000 _B
00002C _H	Extended Communication Control Register 1	ECCR1	R,W, R/W		000000XX _B
00002D _H	Extended Status/Control Register 1	ESCR1	R/W		00000100 _B
00002E _H	Baud Rate Generator Register 10	BGR10	R/W		00000000 _B
00002F _H	Baud Rate Generator Register 11	BGR11	R/W		00000000 _B
000030 _H	PPG 0 Operation Mode Control Register	PPGC0	W,R/W	16-bit PPG 0/1	0X000XX1 _B
000031 _H	PPG 1 Operation Mode Control Register	PPGC1	W,R/W		0X000001 _B
000032 _H	PPG 0/PPG 1 Count Clock Select Register	PPG01	R/W		000000X0 _B
000033 _H	Reserved				
000034 _H	PPG 2 Operation Mode Control Register	PPGC2	W,R/W	16-bit PPG 2/3	0X000XX1 _B
000035 _H	PPG 3 Operation Mode Control Register	PPGC3	W,R/W		0X000001 _B
000036 _H	PPG 2/PPG 3 Count Clock Select Register	PPG23	R/W		000000X0 _B
000037 _H	Reserved				
000038 _H	PPG 4 Operation Mode Control Register	PPGC4	W,R/W	16-bit PPG 4/5	0X000XX1 _B
000039 _H	PPG 5 Operation Mode Control Register	PPGC5	W,R/W		0X000001 _B
00003A _H	PPG 4/PPG 5 Clock Select Register	PPG45	R/W		000000X0 _B
00003B _H	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000 _B
00003C _H	PPG 6 Operation Mode Control Register	PPGC6	W,R/W	16-bit PPG 6/7	0X000XX1 _B
00003D _H	PPG 7 Operation Mode Control Register	PPGC7	W,R/W		0X000001 _B
00003E _H	PPG 6/PPG 7 Count Clock Control Register	PPG67	R/W		000000X0 _B
00003F _H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0000A5 _H	Automatic Ready Function Select Register	ARSR	W	External Memory Access	0011XX00 _B
0000A6 _H	External Address Output Control Register	HACR	W		00000000 _B
0000A7 _H	Bus Control Signal Selection Register	ECSR	W		0000000X _B
0000A8 _H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXXX11 _B
0000A9 _H	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	1XX00100 _B
0000AA _H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 _B
0000AB _H	Reserved				
0000AC _H	DMA Enable L Register	DERL	R/W	DMA	00000000 _B
0000AD _H	DMA Enable H Register	DERH	R/W		00000000 _B
0000AE _H	Flash Control Status Register (Flash memory devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000 _B
0000AF _H	Reserved				
0000B0 _H	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111 _B
0000B1 _H	Interrupt Control Register 01	ICR01	W,R/W		00000111 _B
0000B2 _H	Interrupt Control Register 02	ICR02	W,R/W		00000111 _B
0000B3 _H	Interrupt Control Register 03	ICR03	W,R/W		00000111 _B
0000B4 _H	Interrupt Control Register 04	ICR04	W,R/W		00000111 _B
0000B5 _H	Interrupt Control Register 05	ICR05	W,R/W		00000111 _B
0000B6 _H	Interrupt Control Register 06	ICR06	W,R/W		00000111 _B
0000B7 _H	Interrupt Control Register 07	ICR07	W,R/W		00000111 _B
0000B8 _H	Interrupt Control Register 08	ICR08	W,R/W		00000111 _B
0000B9 _H	Interrupt Control Register 09	ICR09	W,R/W		00000111 _B
0000BA _H	Interrupt Control Register 10	ICR10	W,R/W		00000111 _B
0000BB _H	Interrupt Control Register 11	ICR11	W,R/W		00000111 _B
0000BC _H	Interrupt Control Register 12	ICR12	W,R/W		00000111 _B
0000BD _H	Interrupt Control Register 13	ICR13	W,R/W		00000111 _B
0000BE _H	Interrupt Control Register 14	ICR14	W,R/W		00000111 _B
0000BF _H	Interrupt Control Register 15	ICR15	W,R/W		00000111 _B
0000C0 _H	D/A Converter Data 0	DAT0	R/W	D/A Converter	XXXXXXXX _B
0000C1 _H	D/A Converter Data 1	DAT1	R/W		XXXXXXXX _B
0000C2 _H	D/A Control 0	DACR0	R/W		XXXXXXXX0 _B
0000C3 _H	D/A Control 1	DACR1	R/W		XXXXXXXX0 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007970 _H	I ² C Bus Status Register 0	IBSR0	R	I ² C Interface 0	00000000 _B
007971 _H	I ² C Bus Control Register 0	IBCR0	W,R/W		00000000 _B
007972 _H	I ² C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000 _B
007973 _H		ITBAH0	R/W		00000000 _B
007974 _H	I ² C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111 _B
007975 _H		ITMKH0	R/W		00111111 _B
007976 _H	I ² C 7-bit Slave Address Register 0	ISBA0	R/W		00000000 _B
007977 _H	I ² C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111 _B
007978 _H	I ² C Data Register 0	IDAR0	R/W		00000000 _B
007979 _H , 00797A _H	Reserved				
00797B _H	I ² C Clock Control Register 0	ICCR0	R/W	I ² C Interface 0	00011111 _B
00797C _H to 00797F _H	Reserved				
007980 _H	I ² C Bus Status Register 1	IBSR1	R	I ² C Interface 1	00000000 _B
007981 _H	I ² C Bus Control Register 1	IBCR1	W,R/W		00000000 _B
007982 _H	I ² C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000 _B
007983 _H		ITBAH1	R/W		00000000 _B
007984 _H	I ² C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111 _B
007985 _H		ITMKH1	R/W		00111111 _B
007986 _H	I ² C 7-bit Slave Address Register 1	ISBA1	R/W		00000000 _B
007987 _H	I ² C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111 _B
007988 _H	I ² C Data Register 1	IDAR1	R/W		00000000 _B
007989 _H , 00798A _H	Reserved				
00798B _H	I ² C Clock Control Register 1	ICCR1	R/W	I ² C Interface 1	00011111 _B
00798C _H to 0079C1 _H	Reserved				
0079C2 _H	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	0001X000 _B
0079C3 _H to 0079DF _H	Reserved				

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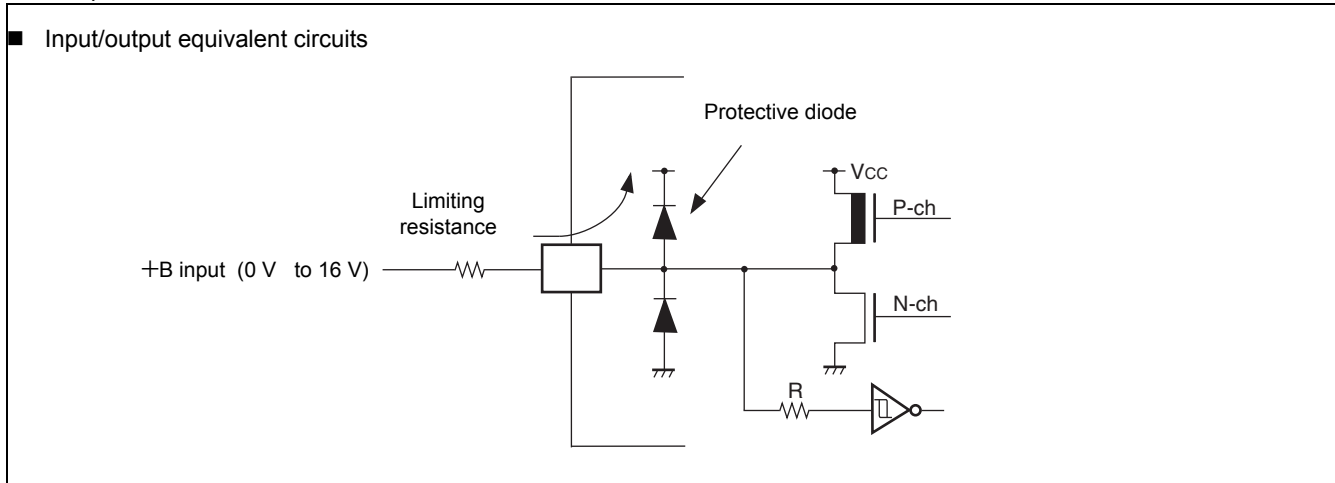
10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI ² OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC _H	—	—
INT9 instruction	N	—	#09	FFFFD8 _H	—	—
Exception	N	—	#10	FFFFD4 _H	—	—
CAN 0 RX	N	—	#11	FFFFD0 _H	ICR00	0000B0 _H
CAN 0 TX/NS	N	—	#12	FFFFCC _H		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4 _H		
CAN 2 RX / I ² C0	N	—	#15	FFFFC0 _H	ICR02	0000B2 _H
CAN 2 TX/NS	N	—	#16	FFFFBC _H		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8 _H	ICR03	0000B3 _H
16-bit Reload Timer 1	Y1	1	#18	FFFFB4 _H		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0 _H	ICR04	0000B4 _H
16-bit Reload Timer 3	Y1	—	#20	FFFFAC _H		
PPG 0/1/4/5	N	—	#21	FFFFA8 _H	ICR05	0000B5 _H
PPG 2/3/6/7	N	—	#22	FFFFA4 _H		
PPG 8/9/C/D	N	—	#23	FFFFA0 _H	ICR06	0000B6 _H
PPG A/B/E/F	N	—	#24	FFFF9C _H		
Time Base Timer	N	—	#25	FFFF98 _H	ICR07	0000B7 _H
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94 _H		
Watch Timer	N	—	#27	FFFF90 _H	ICR08	0000B8 _H
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C _H		
A/D Converter	Y1	5	#29	FFFF88 _H	ICR09	0000B9 _H
Free-run Timer 0 / Free-run Timer 1	N	—	#30	FFFF84 _H		
Input Capture 4/5 / I ² C1	Y1	6	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C _H		
Input Capture 0 to 3	Y1	8	#33	FFFF78 _H	ICR11	0000BB _H
Output Compare 2/3/6/7	Y1	9	#34	FFFF74 _H		
UART 0 RX	Y2	10	#35	FFFF70 _H	ICR12	0000BC _H
UART 0 TX	Y1	11	#36	FFFF6C _H		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68 _H	ICR13	0000BD _H
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64 _H		

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- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:



*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

11.3 DC Characteristics

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

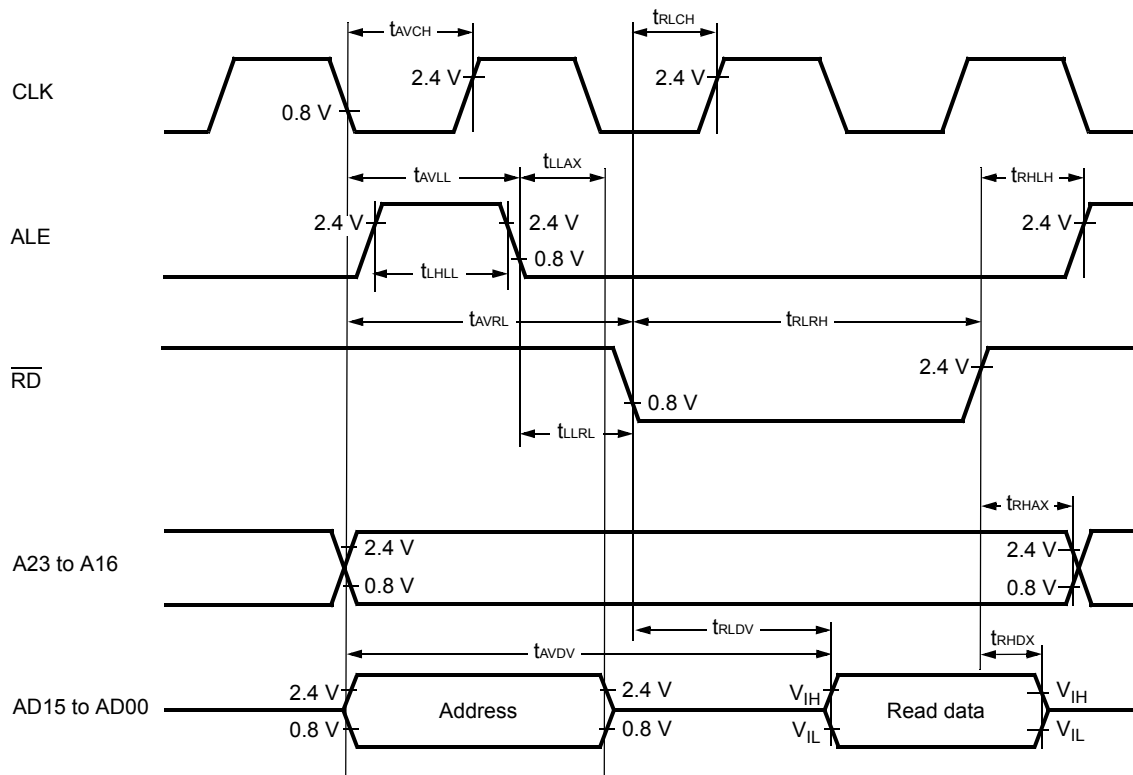
Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{IHS}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{IHA}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected
	V_{IHS}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHI}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{ILA}	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if Automotive input levels are selected
	V_{ILT}	—	—	$V_{SS} - 0.3$	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILI}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	V_{OHI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	V_{OL}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Output L voltage	V_{OLI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 3.0\text{ mA}$	—	—	0.4	V	

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11.4.5 Bus Timing (Read)

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 10$	—	ns
Valid address $\rightarrow$ ALE $\downarrow$ time	t_{AVLL}	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns
ALE $\downarrow \rightarrow$ Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns
Valid address $\rightarrow$ RD $\downarrow$ time	t_{AVRL}	A23 to A16, AD15 to AD00, $\overline{\text{RD}}$		$t_{CP} - 15$	—	ns
Valid address $\rightarrow$ Valid data input	t_{AVDV}	A23 to A16, AD15 to AD00		—	$5 t_{CP}/2 - 60$	ns
$\overline{\text{RD}}$ pulse width	t_{RLRH}	$\overline{\text{RD}}$		$3 t_{CP}/2 - 20$	—	ns
$\overline{\text{RD}} \downarrow \rightarrow$ Valid data input	t_{RLDV}	$\overline{\text{RD}}$, AD15 to AD00		—	$3 t_{CP}/2 - 50$	ns
$\overline{\text{RD}} \uparrow \rightarrow$ Data hold time	t_{RHDX}	$\overline{\text{RD}}$, AD15 to AD00		0	—	ns
$\overline{\text{RD}} \uparrow \rightarrow$ ALE $\uparrow$ time	t_{RHLH}	$\overline{\text{RD}}$, ALE		$t_{CP}/2 - 15$	—	ns
$\overline{\text{RD}} \uparrow \rightarrow$ Address valid time	t_{RHAX}	$\overline{\text{RD}}$, A23 to A16		$t_{CP}/2 - 10$	—	ns
Valid address $\rightarrow$ CLK $\uparrow$ time	t_{AVCH}	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns
$\overline{\text{RD}} \downarrow \rightarrow$ CLK $\uparrow$ time	t_{RLCH}	$\overline{\text{RD}}$, CLK		$t_{CP}/2 - 15$	—	ns
ALE $\downarrow \rightarrow$ $\overline{\text{RD}} \downarrow$ time	t_{LLRL}	ALE, $\overline{\text{RD}}$		$t_{CP}/2 - 15$	—	ns



11.4.9 LIN-UART0/1/2/3

■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

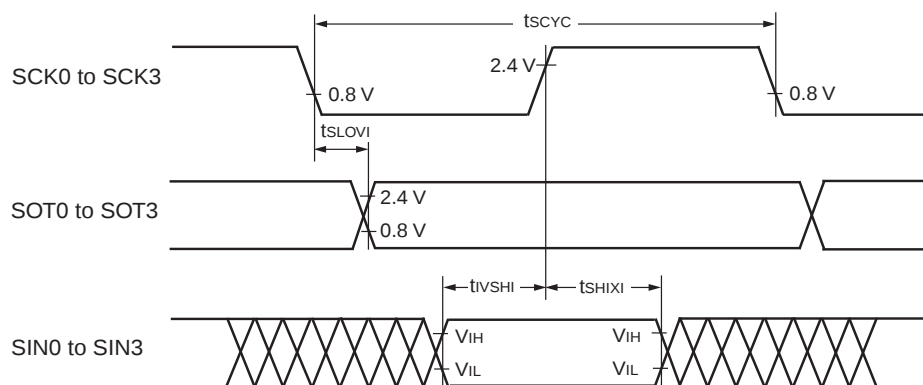
($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock "L" pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$3 t_{CP} - t_R$	—	ns
Serial clock "H" pulse width	t_{SLSH}	SCK0 to SCK3		$t_{CP} + 10$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	$2 t_{CP} + 60$	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SIN0 to SIN3		$t_{CP} + 30$	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

Note:

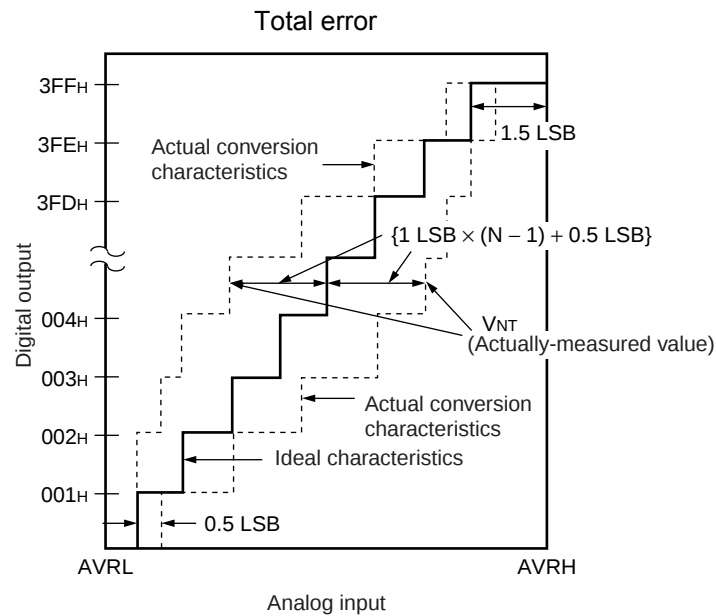
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “(1) Clock Timing”.

• Internal Shift Clock Mode



11.6 Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by the A/D converter.
- Non linearity error : The deviation between the actual conversion characteristics and a line that joins the zero-transition line ("00 0000 0000" $\leftrightarrow$ "00 0000 0001") to the full-scale transition line ("11 1111 1110" $\leftrightarrow$ "11 1111 1111").
- Differential linearity error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$1 \text{ LSB (Ideal value)} = \frac{AVRH - AVRL}{1024} \text{ [V]}$$

N : Value of the digital output from the A/D converter

V_{OT} (Ideal value) = $AVRL + 0.5 \text{ LSB}$ [V]

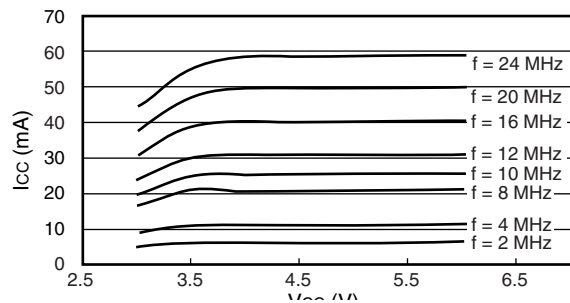
V_{FST} (Ideal value) = $AVRH - 1.5 \text{ LSB}$ [V]

V_{NT} : A voltage at which the digital output transitions from $(N - 1)_H$ to N_H .

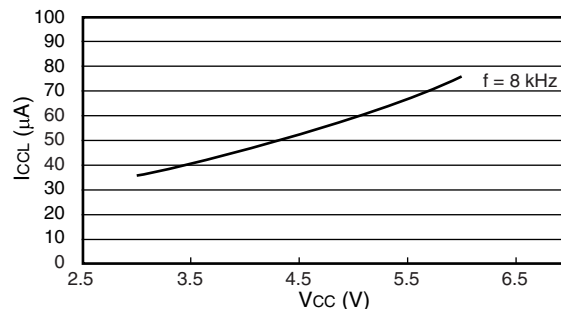
(Continued)

■ MB90F345E, MB90F345ES, MB90F345CE, MB90F345CES

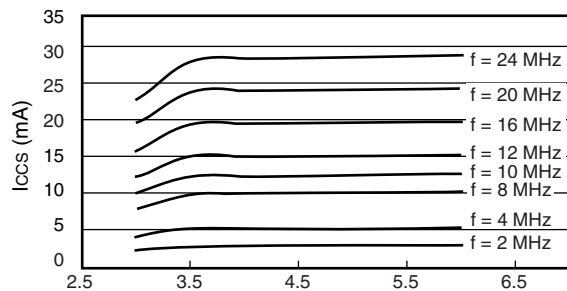
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



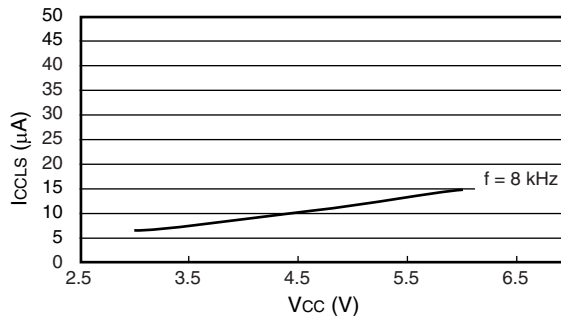
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



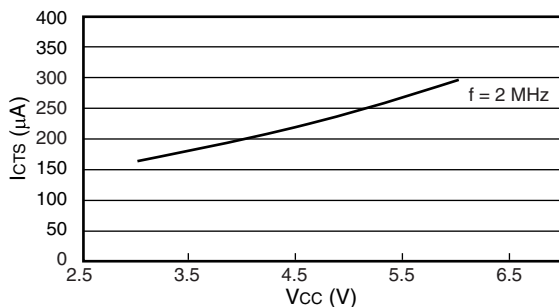
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



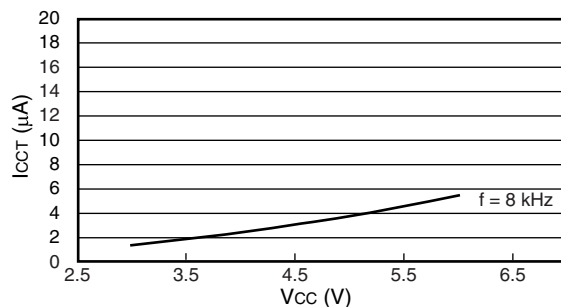
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



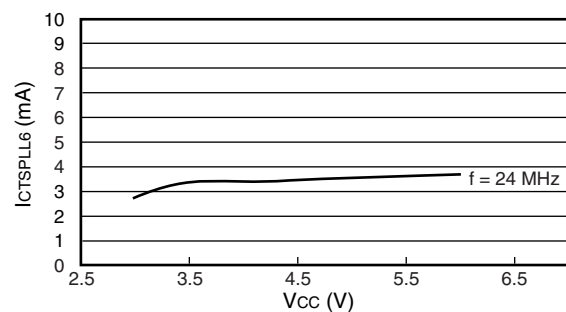
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



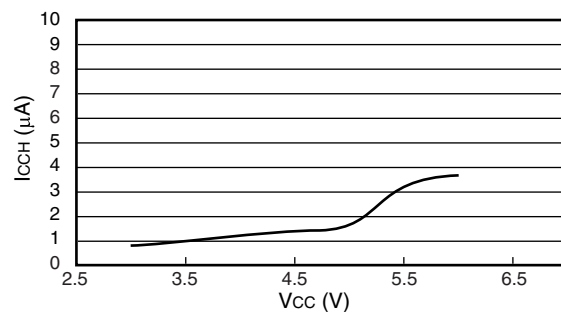
$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency

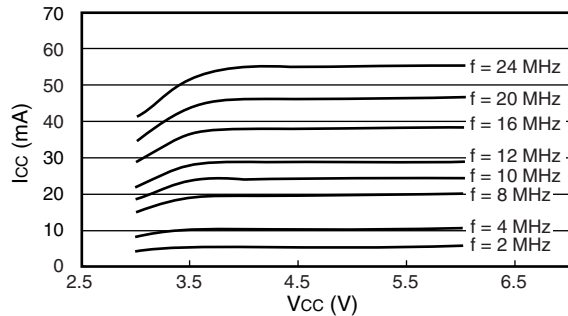


$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped

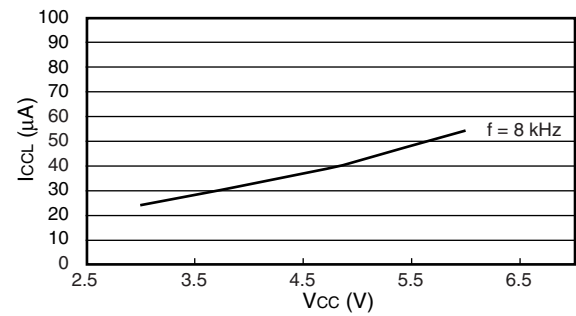


■ MB90347E, MB90347ES, MB90347CE, MB90347CES

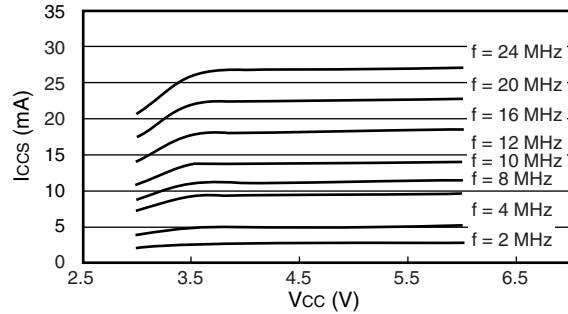
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



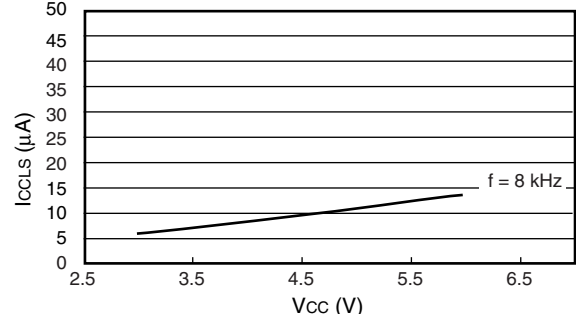
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



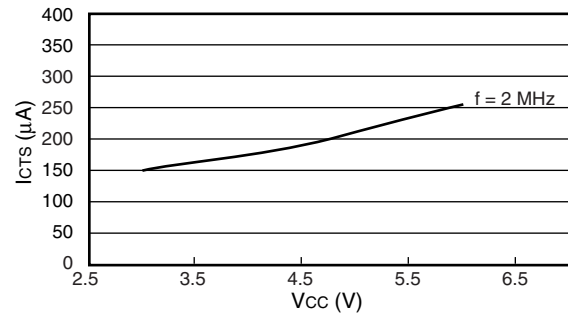
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



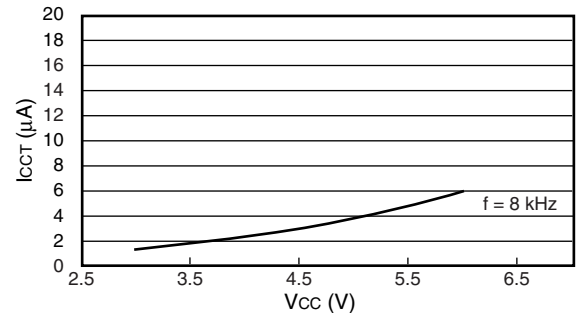
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



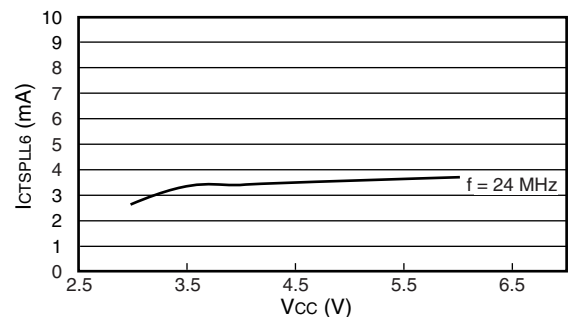
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



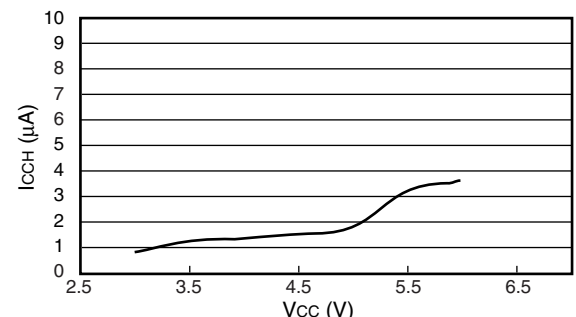
$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped



13. Ordering Information

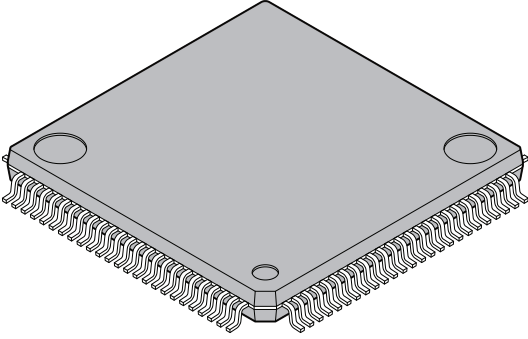
Part number	Package	Remarks
MB90F342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F342ESPF		
MB90F342CEPF		
MB90F342CESPF		
MB90F342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F342ESPMC		
MB90F342CEPMC		
MB90F342CESPMC		
MB90F345EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F345ESPF		
MB90F345CEPF		
MB90F345CESPF		
MB90F345EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F345ESPMC		
MB90F345CEPMC		
MB90F345CESPMC		
MB90F346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F346ESPF		
MB90F346CEPF		
MB90F346CESPF		
MB90F346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F346ESPMC		
MB90F346CEPMC		
MB90F346CESPMC		

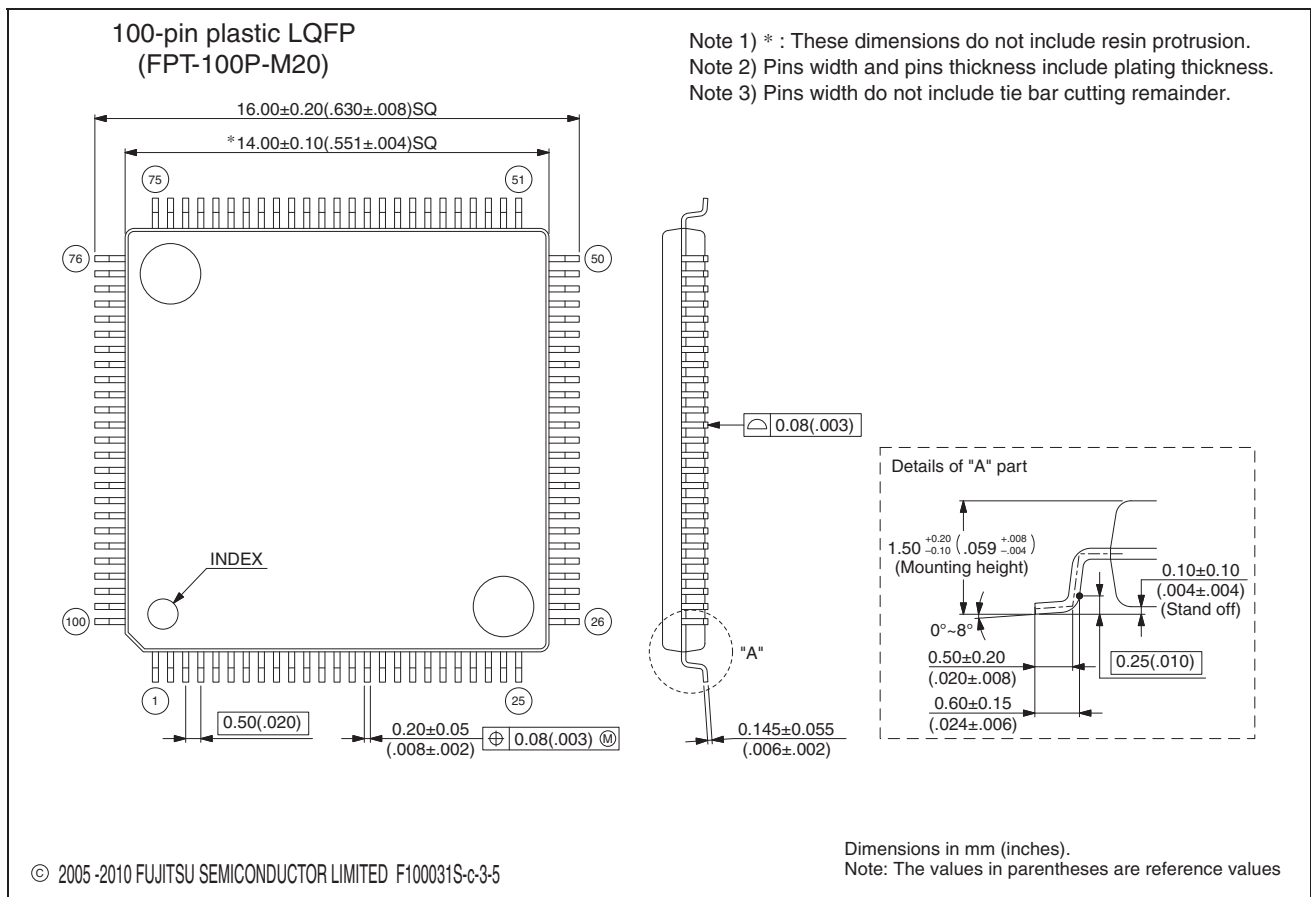
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Part number	Package	Remarks
MB90F347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F347ESPF		
MB90F347CEPF		
MB90F347CESPF		
MB90F347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F347ESPMC		
MB90F347CEPMC		
MB90F347CESPMC		
MB90F349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F349ESPF		
MB90F349CEPF		
MB90F349CESPF		
MB90F349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F349ESPMC		
MB90F349CEPMC		
MB90F349CESPMC		
MB90341EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90341ESPF		
MB90341CEPF		
MB90341CESPF		
MB90341EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90341ESPMC		
MB90341CEPMC		
MB90341CESPMC		
MB90342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90342ESPF		
MB90342CEPF		
MB90342CESPF		
MB90342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90342ESPMC		
MB90342CEPMC		
MB90342CESPMC		

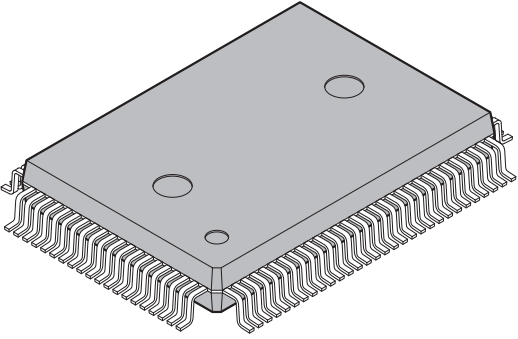
(Continued)

14. Package Dimensions

 100-pin plastic LQFP (FPT-100P-M20)	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14×14-0.50



(Continued)

100-pin plastic QFP  (FPT-100P-M06)	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65

