# Infineon Technologies - MB90347ESPMC-GS-280E1 Datasheet

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

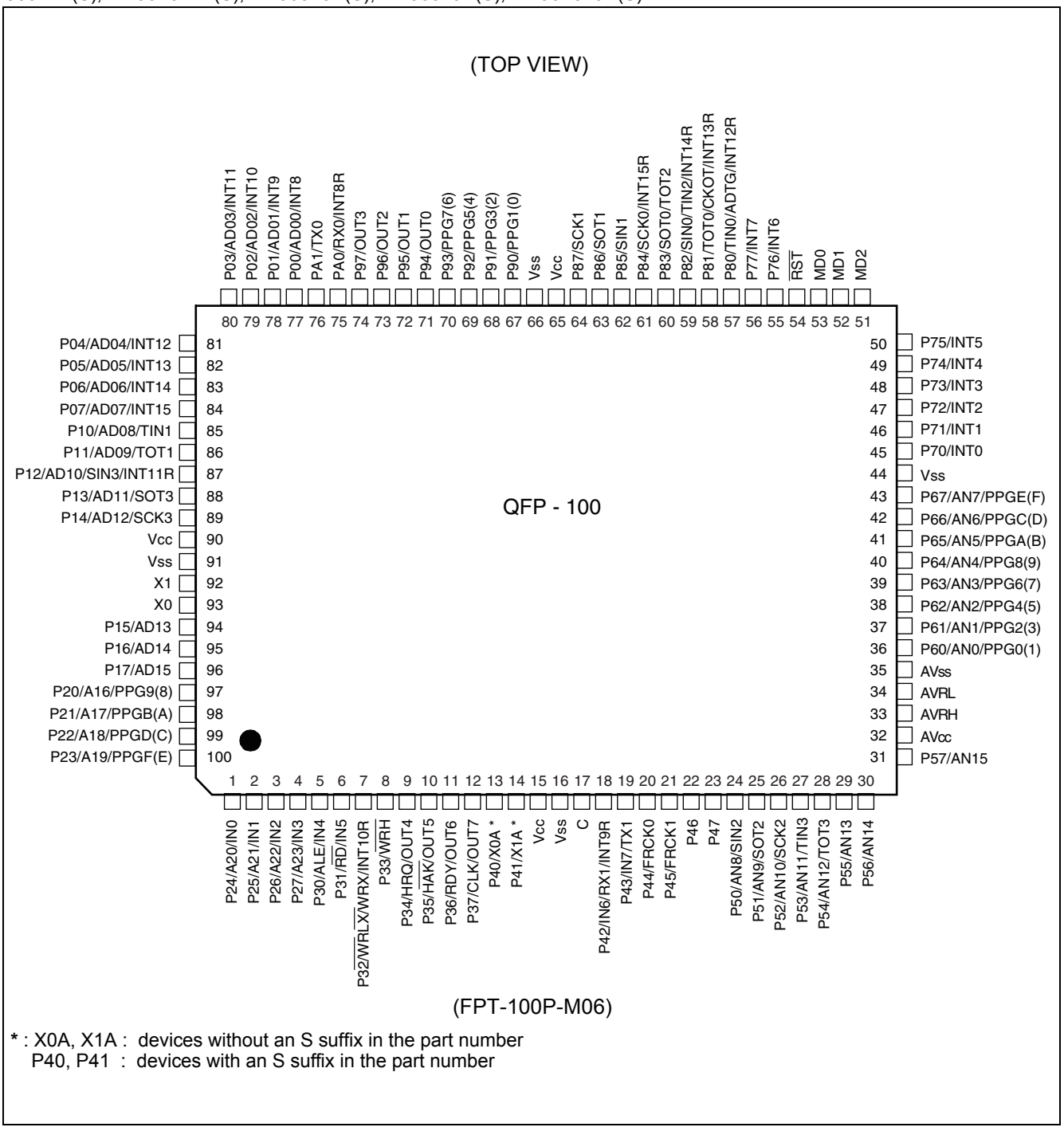
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CANbus, EBI/EMI, LINbus, SCI, UART/USART |
| Peripherals | DMA, POR, WDT |
| Number of I/O | 82 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | Mask ROM |
| EEPROM Size | - |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 5.5V |
| Data Converters | A/D 16x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-280e1 |

## 2. Pin Assignments

■ MB90341E(S), MB90342E(S), MB90F342E(S), MB90F345E(S), MB90346E(S), MB90F346E(S), MB90347E(S), MB90F347E(S), MB90348E(S), MB90349E(S), MB90F349E(S)




(FPT-100P-M06)

***** : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

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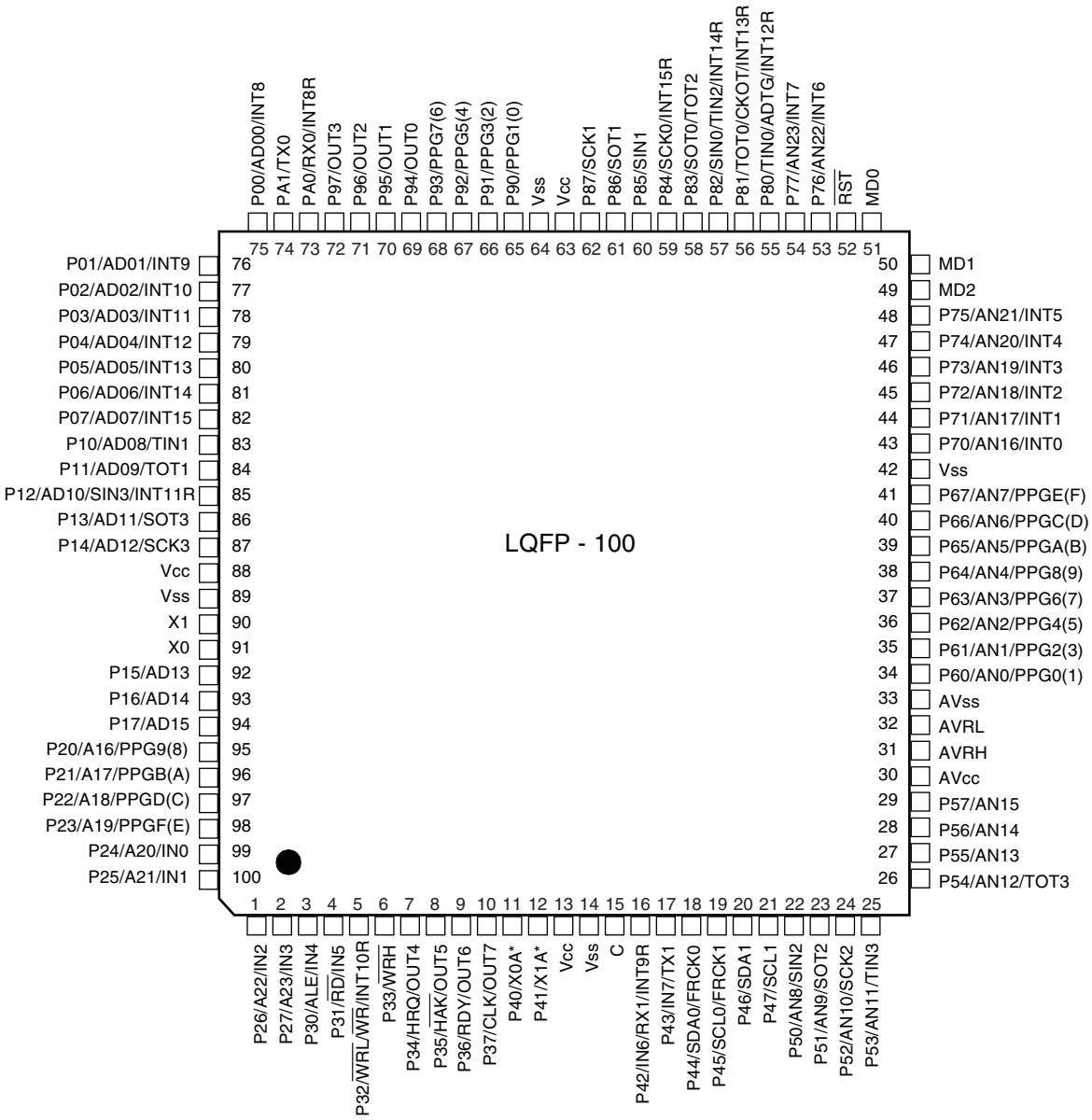
(TOP VIEW)




(FPT-100P-M20)

* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 33 | 31 | AVRH | L | Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to $AV_{CC}$. |
| 34 | 32 | AVRL | K | Lower reference voltage input pin for the A/D Converter |
| 35 | 33 | $AV_{SS}$ | K | Analog GND pin for the A/D Converter |
| 36 to 43 | 34 to 41 | P60 to P67 | I | General purpose I/O pins. |
| | | AN0 to AN7 | | Analog input pins for the A/D converter |
| | | PPG0, 2, 4, 6, 8, A, C, E | | Output pins for PPGs |
| 44 | 42 | $V_{SS}$ | — | GND pin |
| 45 to 50 | 43 to 48 | P70 to P75 | I | General purpose I/O pins. |
| | | AN16 to AN21 | | Analog input pins for the A/D converter (devices with a C suffix in the part number) |
| | | INT0 to INT5 | | External interrupt request input pins |
| 51 | 49 | MD2 | D | Input pin for specifying the operating mode. |
| 52, 53 | 50, 51 | MD1, MD0 | C | Input pins for specifying the operating mode. |
| 54 | 52 | $\overline{RST}$ | E | Reset input pin |
| 55, 56 | 53, 54 | P76, P77 | I | General purpose I/O pins. |
| | | AN22, AN23 | | Analog input pins for the A/D converter (devices with a C suffix in the part number) |
| | | INT6, INT7 | | External interrupt request input pins |
| 57 | 55 | P80 | F | General purpose I/O pin. |
| | | TIN0 | | Event input pin for the reload timer |
| | | ADTG | | Trigger input pin for the A/D converter |
| | | INT12R | | External interrupt request input pin |
| 58 | 56 | P81 | F | General purpose I/O pin. |
| | | TOT0 | | Output pin for the reload timer |
| | | CKOT | | Output pin for the clock monitor |
| | | INT13R | | External interrupt request input pin |
| 59 | 57 | P82 | M | General purpose I/O pin. |
| | | SIN0 | | Serial data input pin for UART0 |
| | | TIN2 | | Event input pin for the reload timer |
| | | INT14R | | External interrupt request input pin |
| 60 | 58 | P83 | F | General purpose I/O pin. |
| | | SOT0 | | Serial data output pin for UART0 |
| | | TOT2 | | Output pin for the reload timer |

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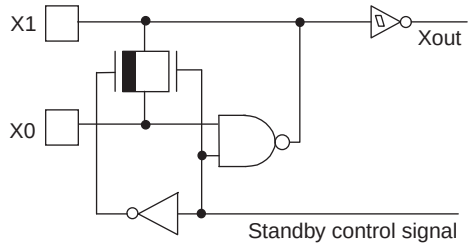
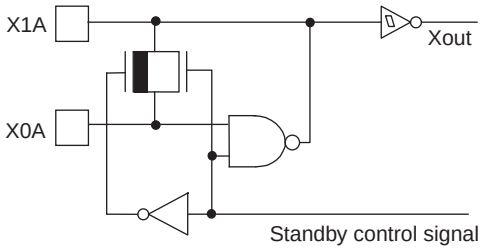
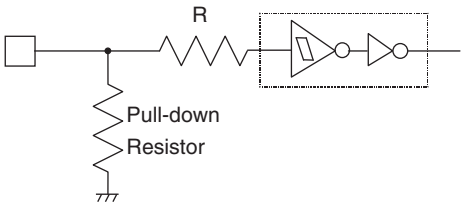
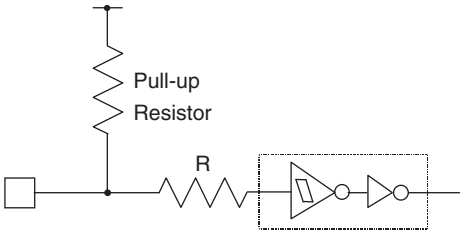
## 4. I/O Circuit Type

| Type | Circuit | Remarks |
|---|---|---|
| A |  | Oscillation circuit<br>High-speed oscillation feedback resistor = approx. 1 MΩ |
| B |  | Oscillation circuit<br>Low-speed oscillation feedback resistor = approx. 10 MΩ |
| C |  | ■ MASK ROM and evaluation products: CMOS hysteresis input pin<br>■ Flash memory products: CMOS input pin |
| D |  | MASK ROM and evaluation products:<br>■ CMOS hysteresis input pin<br>■ Pull-down resistor value: approx. 50 kΩ<br>Flash memory products:<br>■ CMOS input pin<br>■ No pull-down |
| E |  | CMOS hysteresis input pin<br>Pull-up resistor value: approx. 50 kΩ |

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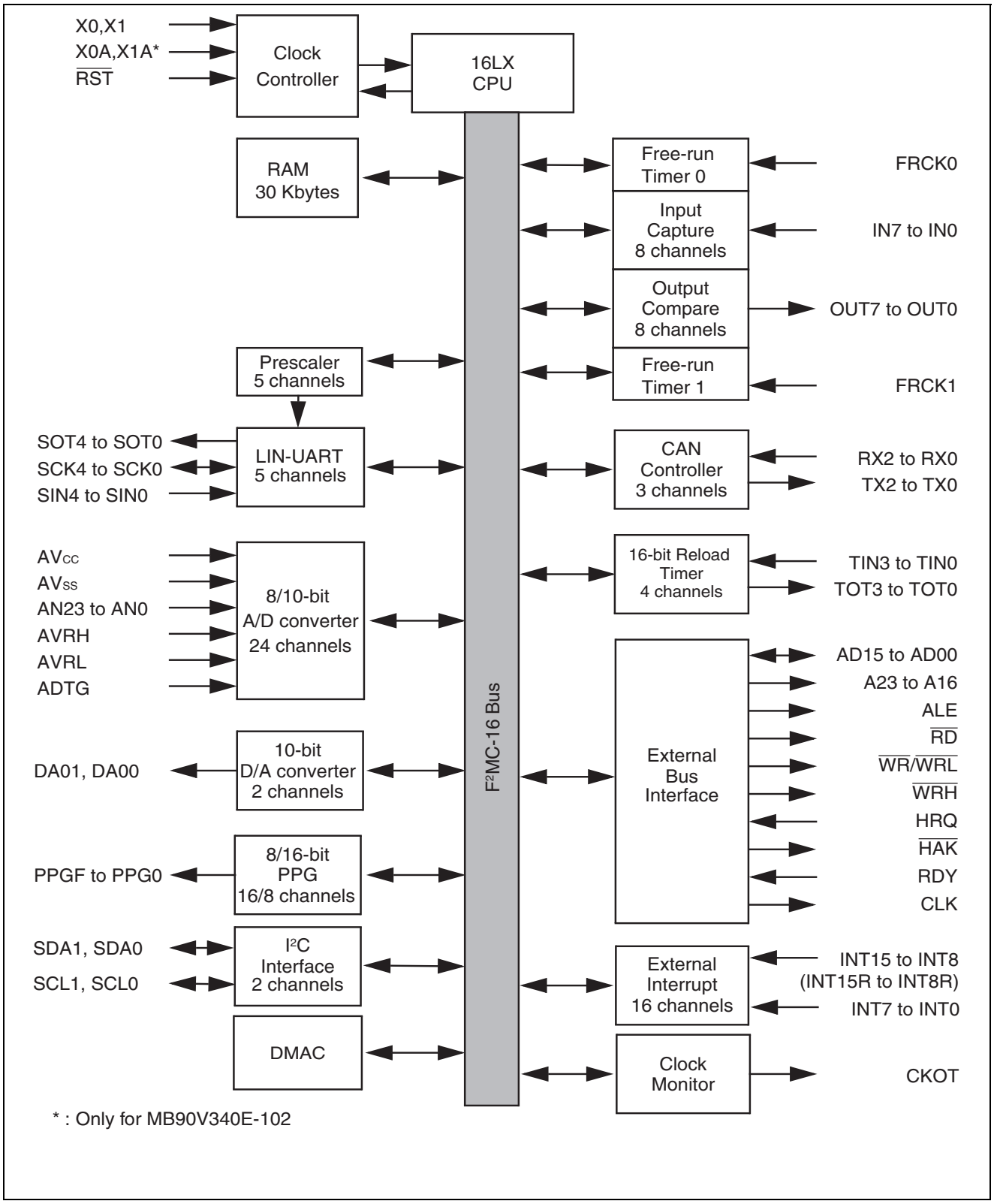
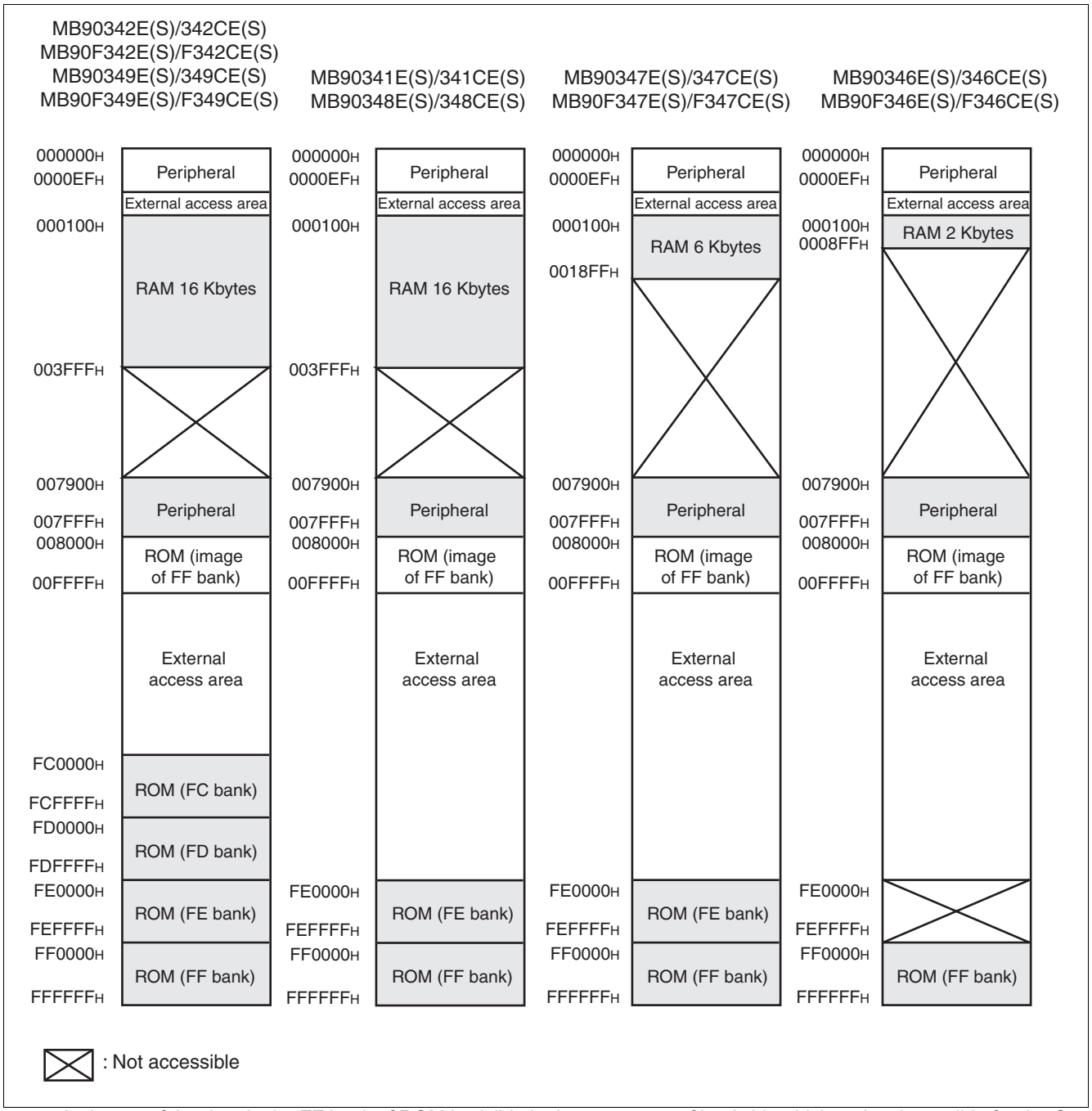
## 6. Block Diagrams

- MB90V340E-101/102






**Note:** :An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.
For example, when the address $00C000_H$ is accessed, the data at $FFC000_H$ in ROM is actually accessed.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
As a result, the image between $FF8000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF7FFF_H$ is visible only in bank FF.

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $0000C4_H$, $0000C5_H$ | Reserved | | | | |
| $0000C6_H$ | External Interrupt Enable 0 | ENIR0 | R/W | External Interrupt 0 | $00000000_B$ |
| $0000C7_H$ | External Interrupt Source 0 | EIRR0 | R/W | | $XXXXXXXX_B$ |
| $0000C8_H$ | External Interrupt Level Setting 0 | ELVR0 | R/W | | $00000000_B$ |
| $0000C9_H$ | External Interrupt Level Setting 0 | ELVR0 | R/W | | $00000000_B$ |
| $0000CA_H$ | External Interrupt Enable 1 | ENIR1 | R/W | External Interrupt 1 | $00000000_B$ |
| $0000CB_H$ | External Interrupt Source 1 | EIRR1 | R/W | | $XXXXXXXX_B$ |
| $0000CC_H$ | External Interrupt Level Setting 1 | ELVR1 | R/W | | $00000000_B$ |
| $0000CD_H$ | External Interrupt Level Setting 1 | ELVR1 | R/W | | $00000000_B$ |
| $0000CE_H$ | External Interrupt Source Select | EISSR | R/W | | $00000000_B$ |
| $0000CF_H$ | PLL/Sub clock Control Register | PSCCR | W | PLL | $XXXX0000_B$ |
| $0000D0_H$ | DMA Buffer Address Pointer L Register | BAPL | R/W | DMA | $XXXXXXXX_B$ |
| $0000D1_H$ | DMA Buffer Address Pointer M Register | BAPM | R/W | | $XXXXXXXX_B$ |
| $0000D2_H$ | DMA Buffer Address Pointer H Register | BAPH | R/W | | $XXXXXXXX_B$ |
| $0000D3_H$ | DMA Control Register | DMACS | R/W | | $XXXXXXXX_B$ |
| $0000D4_H$ | I/O Register Address Pointer L Register | IOAL | R/W | | $XXXXXXXX_B$ |
| $0000D5_H$ | I/O Register Address Pointer H Register | IOAH | R/W | | $XXXXXXXX_B$ |
| $0000D6_H$ | Data Counter L Register | DCTL | R/W | | $XXXXXXXX_B$ |
| $0000D7_H$ | Data Counter H Register | DCTH | R/W | | $XXXXXXXX_B$ |
| $0000D8_H$ | Serial Mode Register 2 | SMR2 | W,R/W | UART2 | $00000000_B$ |
| $0000D9_H$ | Serial Control Register 2 | SCR2 | W,R/W | | $00000000_B$ |
| $0000DA_H$ | Reception/Transmission Data Register 2 | RDR2/TDR2 | R/W | | $00000000_B$ |
| $0000DB_H$ | Serial Status Register 2 | SSR2 | R,R/W | | $00001000_B$ |
| $0000DC_H$ | Extended Communication Control Register 2 | ECCR2 | R,W, R/W | | $000000XX_B$ |
| $0000DD_H$ | Extended Status Control Register 2 | ESCR2 | R/W | | $00000100_B$ |
| $0000DE_H$ | Baud Rate Generator Register 20 | BGR20 | R/W | | $00000000_B$ |
| $0000DF_H$ | Baud Rate Generator Register 21 | BGR21 | R/W | | $00000000_B$ |
| $0000E0_H$ to $0000EF_H$ | Reserved for CAN Controller 2. Refer to "CAN Controllers" | | | | |
| $0000F0_H$ to $0000FF_H$ | External | | | | |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $007900_H$ | Reload Register L0 | PRLL0 | R/W | 16-bit PPG 0/1 | $XXXXXXXX_B$ |
| $007901_H$ | Reload Register H0 | PRLH0 | R/W | | $XXXXXXXX_B$ |
| $007902_H$ | Reload Register L1 | PRLL1 | R/W | | $XXXXXXXX_B$ |
| $007903_H$ | Reload Register H1 | PRLH1 | R/W | | $XXXXXXXX_B$ |
| $007904_H$ | Reload Register L2 | PRLL2 | R/W | 16-bit PPG 2/3 | $XXXXXXXX_B$ |
| $007905_H$ | Reload Register H2 | PRLH2 | R/W | | $XXXXXXXX_B$ |
| $007906_H$ | Reload Register L3 | PRLL3 | R/W | | $XXXXXXXX_B$ |
| $007907_H$ | Reload Register H3 | PRLH3 | R/W | | $XXXXXXXX_B$ |
| $007908_H$ | Reload Register L4 | PRLL4 | R/W | 16-bit PPG 4/5 | $XXXXXXXX_B$ |
| $007909_H$ | Reload Register H4 | PRLH4 | R/W | | $XXXXXXXX_B$ |
| $00790A_H$ | Reload Register L5 | PRLL5 | R/W | | $XXXXXXXX_B$ |
| $00790B_H$ | Reload Register H5 | PRLH5 | R/W | | $XXXXXXXX_B$ |
| $00790C_H$ | Reload Register L6 | PRLL6 | R/W | 16-bit PPG 6/7 | $XXXXXXXX_B$ |
| $00790D_H$ | Reload Register H6 | PRLH6 | R/W | | $XXXXXXXX_B$ |
| $00790E_H$ | Reload Register L7 | PRLL7 | R/W | | $XXXXXXXX_B$ |
| $00790F_H$ | Reload Register H7 | PRLH7 | R/W | | $XXXXXXXX_B$ |
| $007910_H$ | Reload Register L8 | PRLL8 | R/W | 16-bit PPG 8/9 | $XXXXXXXX_B$ |
| $007911_H$ | Reload Register H8 | PRLH8 | R/W | | $XXXXXXXX_B$ |
| $007912_H$ | Reload Register L9 | PRLL9 | R/W | | $XXXXXXXX_B$ |
| $007913_H$ | Reload Register H9 | PRLH9 | R/W | | $XXXXXXXX_B$ |
| $007914_H$ | Reload Register LA | PRLLA | R/W | 16-bit PPG A/B | $XXXXXXXX_B$ |
| $007915_H$ | Reload Register HA | PRLHA | R/W | | $XXXXXXXX_B$ |
| $007916_H$ | Reload Register LB | PRLLB | R/W | | $XXXXXXXX_B$ |
| $007917_H$ | Reload Register HB | PRLHB | R/W | | $XXXXXXXX_B$ |
| $007918_H$ | Reload Register LC | PRLLC | R/W | 16-bit PPG C/D | $XXXXXXXX_B$ |
| $007919_H$ | Reload Register HC | PRLHC | R/W | | $XXXXXXXX_B$ |
| $00791A_H$ | Reload Register LD | PRLLD | R/W | | $XXXXXXXX_B$ |
| $00791B_H$ | Reload Register HD | PRLHD | R/W | | $XXXXXXXX_B$ |
| $00791C_H$ | Reload Register LE | PRLLE | R/W | 16-bit PPG E/F | $XXXXXXXX_B$ |
| $00791D_H$ | Reload Register HE | PRLHE | R/W | | $XXXXXXXX_B$ |
| $00791E_H$ | Reload Register LF | PRLLF | R/W | | $XXXXXXXX_B$ |
| $00791F_H$ | Reload Register HF | PRLHF | R/W | | $XXXXXXXX_B$ |
| $007920_H$ | Input Capture 0 | IPCP0 | R | Input Capture 0/1 | $XXXXXXXX_B$ |
| $007921_H$ | Input Capture 0 | IPCP0 | R | | $XXXXXXXX_B$ |
| $007922_H$ | Input Capture 1 | IPCP1 | R | | $XXXXXXXX_B$ |
| $007923_H$ | Input Capture 1 | IPCP1 | R | | $XXXXXXXX_B$ |

*(Continued)*

**List of Message Buffers (DLC Registers and Data Registers) (3)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| $007AF0_H$ to $007AF7_H$ | $007CF0_H$ to $007CF7_H$ | Data Register 14 (8 bytes) | DTR14 | R/W | $XXXXXXXX_B$ to $XXXXXXXX_B$ |
| $007AF8_H$ to $007AFF_H$ | $007CF8_H$ to $007CFF_H$ | Data Register 15 (8 bytes) | DTR15 | R/W | $XXXXXXXX_B$ to $XXXXXXXX_B$ |

## 10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

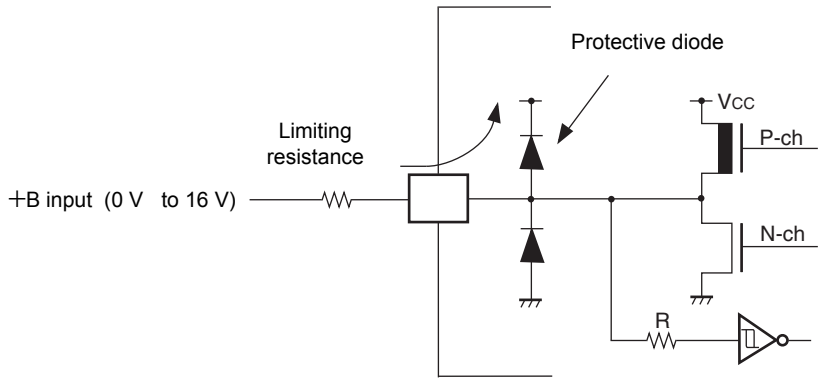
| Interrupt cause | EI$^2$OS Support | DMA channel number | Interrupt vector | | Interrupt control register | |
|---|---|---|---|---|---|---|
| | | | Number | Address | Number | Address |
| Reset | N | — | #08 | FFFFDC$_H$ | — | — |
| INT9 instruction | N | — | #09 | FFFFD8$_H$ | — | — |
| Exception | N | — | #10 | FFFFD4$_H$ | — | — |
| CAN 0 RX | N | — | #11 | FFFFD0$_H$ | ICR00 | 0000B0$_H$ |
| CAN 0 TX/NS | N | — | #12 | FFFFCC$_H$ | | |
| CAN 1 RX / Input Capture 6 | Y1 | — | #13 | FFFFC8$_H$ | ICR01 | 0000B1$_H$ |
| CAN 1 TX/NS / Input Capture 7 | Y1 | — | #14 | FFFFC4$_H$ | | |
| CAN 2 RX / I$^2$C0 | N | — | #15 | FFFFC0$_H$ | ICR02 | 0000B2$_H$ |
| CAN 2 TX/NS | N | — | #16 | FFFFBC$_H$ | | |
| 16-bit Reload Timer 0 | Y1 | 0 | #17 | FFFFB8$_H$ | ICR03 | 0000B3$_H$ |
| 16-bit Reload Timer 1 | Y1 | 1 | #18 | FFFFB4$_H$ | | |
| 16-bit Reload Timer 2 | Y1 | 2 | #19 | FFFFB0$_H$ | ICR04 | 0000B4$_H$ |
| 16-bit Reload Timer 3 | Y1 | — | #20 | FFFFAC$_H$ | | |
| PPG 0/1/4/5 | N | — | #21 | FFFFA8$_H$ | ICR05 | 0000B5$_H$ |
| PPG 2/3/6/7 | N | — | #22 | FFFFA4$_H$ | | |
| PPG 8/9/C/D | N | — | #23 | FFFFA0$_H$ | ICR06 | 0000B6$_H$ |
| PPG A/B/E/F | N | — | #24 | FFFF9C$_H$ | | |
| Time Base Timer | N | — | #25 | FFFF98$_H$ | ICR07 | 0000B7$_H$ |
| External Interrupt 0 to 3, 8 to 11 | Y1 | 3 | #26 | FFFF94$_H$ | | |
| Watch Timer | N | — | #27 | FFFF90$_H$ | ICR08 | 0000B8$_H$ |
| External Interrupt 4 to 7, 12 to 15 | Y1 | 4 | #28 | FFFF8C$_H$ | | |
| A/D Converter | Y1 | 5 | #29 | FFFF88$_H$ | ICR09 | 0000B9$_H$ |
| Free-run Timer 0 / Free-run Timer 1 | N | — | #30 | FFFF84$_H$ | | |
| Input Capture 4/5 / I$^2$C1 | Y1 | 6 | #31 | FFFF80$_H$ | ICR10 | 0000BA$_H$ |
| Output Compare 0/1/4/5 | Y1 | 7 | #32 | FFFF7C$_H$ | | |
| Input Capture 0 to 3 | Y1 | 8 | #33 | FFFF78$_H$ | ICR11 | 0000BB$_H$ |
| Output Compare 2/3/6/7 | Y1 | 9 | #34 | FFFF74$_H$ | | |
| UART 0 RX | Y2 | 10 | #35 | FFFF70$_H$ | ICR12 | 0000BC$_H$ |
| UART 0 TX | Y1 | 11 | #36 | FFFF6C$_H$ | | |
| UART 1 RX / UART 3 RX | Y2 | 12 | #37 | FFFF68$_H$ | ICR13 | 0000BD$_H$ |
| UART 1 TX / UART 3 TX | Y1 | 13 | #38 | FFFF64$_H$ | | |

*(Continued)*

*(Continued)*

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

■ Input/output equivalent circuits




*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

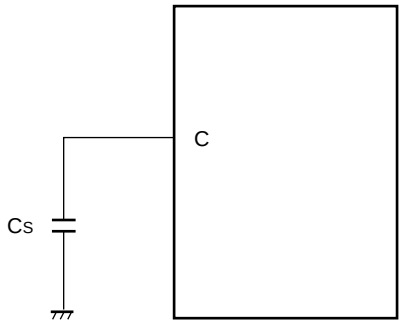
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 11.2 Recommended Operating Conditions

($V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Power supply voltage | $V_{CC}$, $AV_{CC}$ | 4.0 | 5.0 | 5.5 | V | Under normal operation |
| | | 3.5 | 5.0 | 5.5 | V | Under normal operation, when not using the A/D converter and not Flash programming. |
| | | 4.5 | 5.0 | 5.5 | V | When External bus is used. |
| | | 3.0 | — | 5.5 | V | Maintains RAM data in stop mode |
| Smoothing capacitor | $C_S$ | 0.1 | — | 1.0 | µF | Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the $V_{CC}$ should be greater than this capacitor. |
| Operating temperature | $T_A$ | −40 | — | +105 | °C | |

C Pin Connection Diagram




WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## 11.4 AC Characteristics

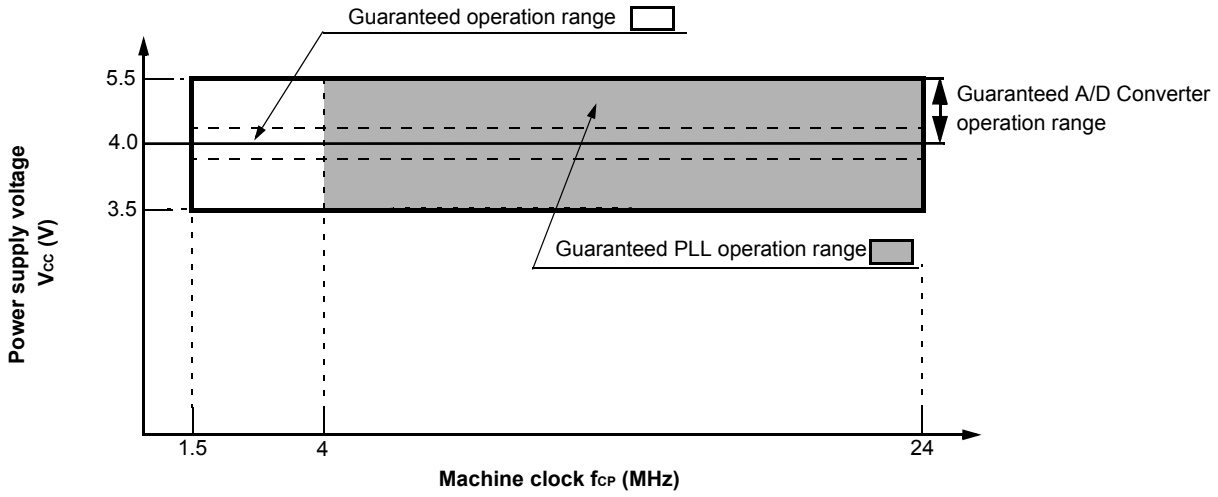
### *11.4.1 Clock Timing*

($T_A$ = –40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

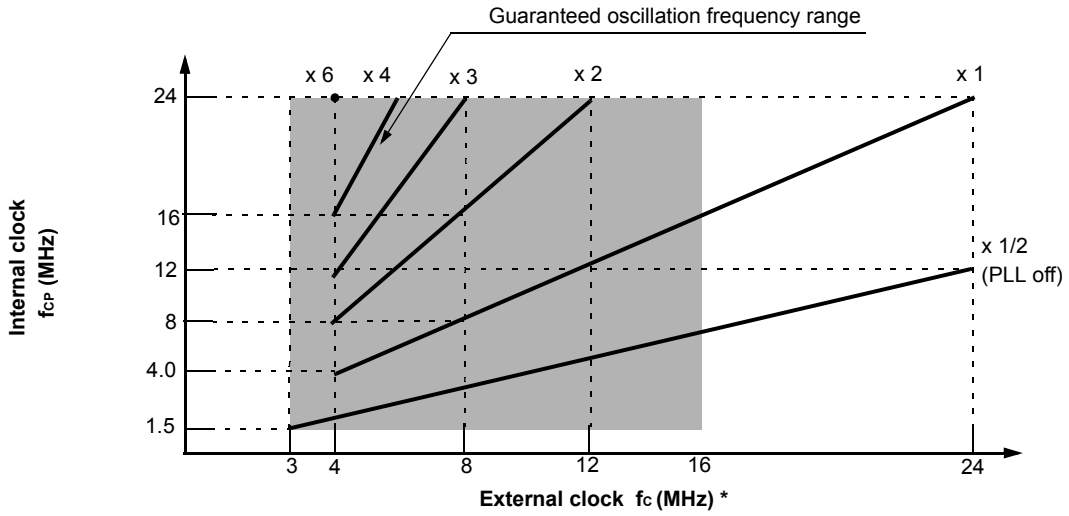
| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_C$ | X0, X1 | 3 | — | 16 | MHz | When using an oscillation circuit |
| | | | 4 | — | 16 | MHz | PLL multiplied by 1<br>When using an oscillation circuit |
| | | | 4 | — | 12 | MHz | PLL multiplied by 2<br>When using an oscillation circuit |
| | | | 4 | — | 8 | MHz | PLL multiplied by 3<br>When using an oscillation circuit |
| | | | 4 | — | 6 | MHz | PLL multiplied by 4<br>When using an oscillation circuit |
| | | | — | — | 4 | MHz | PLL multiplied by 6<br>When using an oscillation circuit |
| | | | 3 | — | 24 | MHz | When using an external clock* |
| | $f_{CL}$ | X0A, X1A | — | 32.768 | 100 | kHz | |
| Clock cycle time | $t_{CYL}$ | X0, X1 | 62.5 | — | 333 | ns | When using an oscillation circuit |
| | | X0, X1 | 41.67 | — | 333 | ns | When using an external clock |
| | $t_{CYLL}$ | X0A, X1A | 10 | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | 10 | — | — | ns | Duty ratio is about 30% to 70%. |
| | $P_{WHL}$, $P_{WLL}$ | X0A | 5 | 15.2 | — | µs | |
| Input clock rise and fall time | $t_{CR}$, $t_{CF}$ | X0 | — | — | 5 | ns | When using external clock |
| Internal operating clock frequency (machine clock) | $f_{CP}$ | — | 1.5 | — | 24 | MHz | When using main clock |
| | $f_{CPL}$ | — | — | 8.192 | 50 | kHz | When using sub clock |
| Internal operating clock cycle time (machine clock) | $t_{CP}$ | — | 41.67 | — | 666 | ns | When using main clock |
| | $t_{CPL}$ | — | 20 | 122.1 | — | µs | When using sub clock |

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in “Relation between the external clock frequency and machine clock frequency”.

Guaranteed PLL operation range




**Guaranteed operation range of MB90340E series**



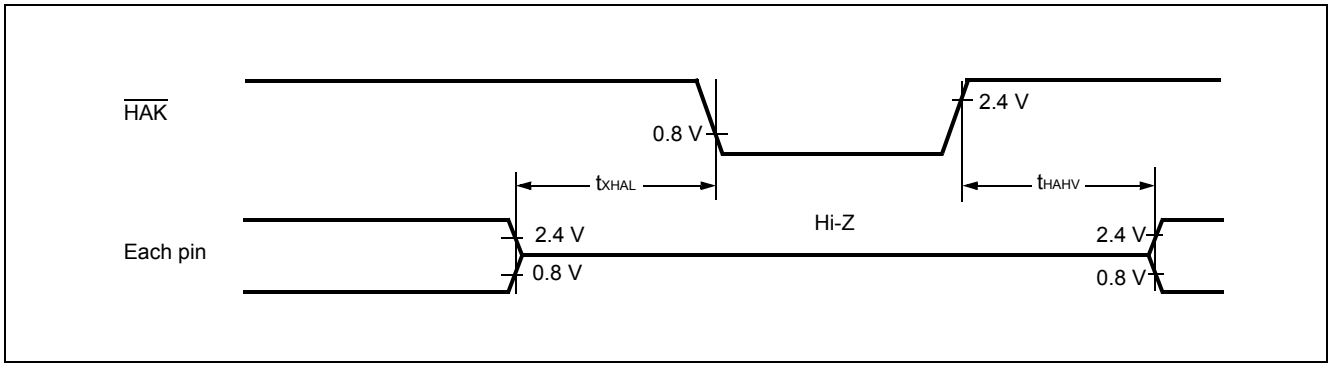

* : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

### 11.4.8 Hold Timing

($T_A = -40°C$ to $+105°C$, $V_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = 0.0\ V$, $f_{CP} \leq 24$ MHz)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Pin floating → $\overline{HAK}$ ↓ time | $t_{XHAL}$ | $\overline{HAK}$ | — | 30 | $t_{CP}$ | ns |
| $\overline{HAK}$ ↑ time → Pin valid time | $t_{HAHV}$ | $\overline{HAK}$ | | $t_{CP}$ | 2 $t_{CP}$ | ns |

**Note:** : There is more than 1 cycle from when HRQ reads in until the $\overline{HAK}$ is changed.

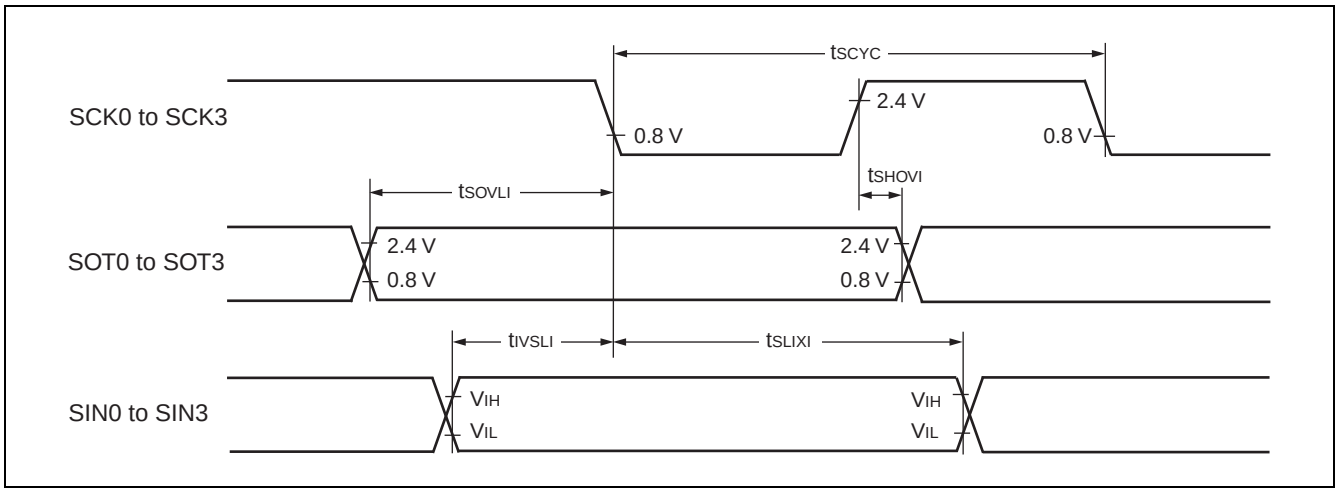


■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1**

($T_A$ = −40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal clock operation output pins are $C_L$ = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | −50 | +50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↓ → Valid SIN hold time | $t_{SLIXI}$ | SCK0 to SCK3, SIN0 to SIN3 | | 0 | — | ns |
| SOT → SCK ↓ delay time | $t_{SOVLI}$ | SCK0 to SCK3, SOT0 to SOT3 | | 3 $t_{CP}$ − 70 | — | ns |

**Note:**
- $C_L$ is load capacity value of pins when testing.
- $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".



## 11.6 Definition of A/D Converter Terms

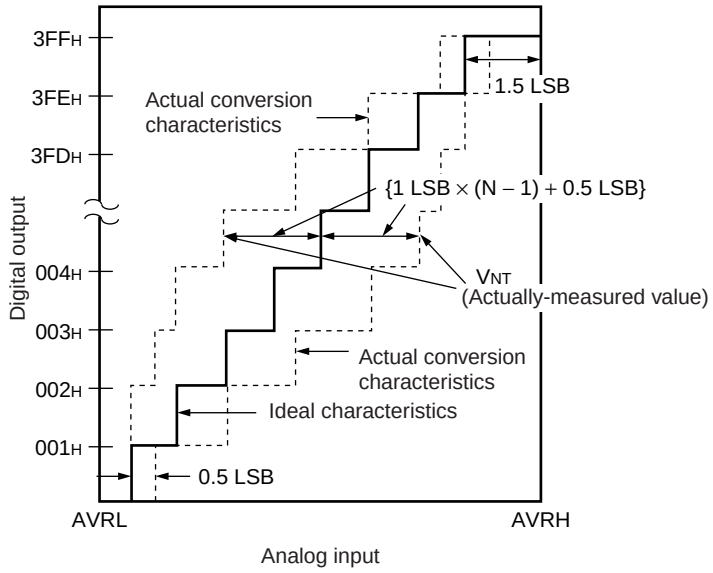
Resolution : Analog variation that is recognized by the A/D converter.

Non linearity error : The deviation between the actual conversion characteristics and a line that joins the zero-transition line ( “00 0000 0000” ← → “00 0000 0001” ) to the full-scale transition line ( “11 1111 1110” ← → “11 1111 1111” ) .

Differential linearity error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Total error : Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.

Total error




$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

N : Value of the digital output from the A/D converter

$V_{OT}$ (Ideal value) = AVRL + 0.5 LSB [V]

$V_{FST}$ (Ideal value) = AVRH − 1.5 LSB [V]

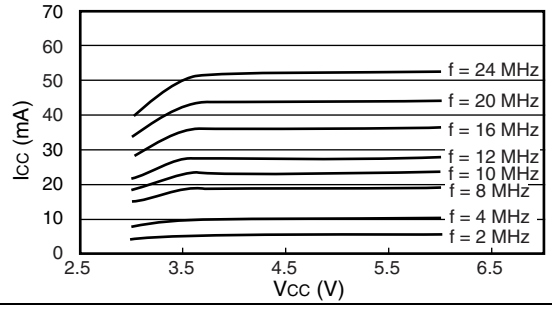
$V_{NT}$ : A voltage at which the digital output transitions from $(N - 1)_H$ to $N_H$.

*(Continued)*

■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES

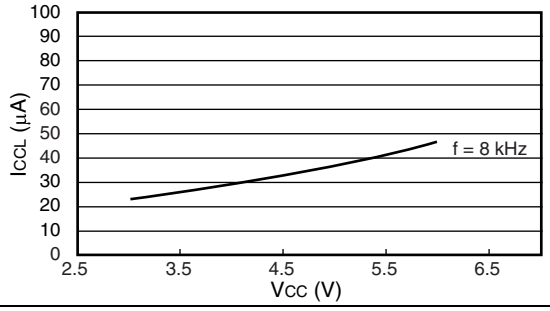
$I_{CC} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



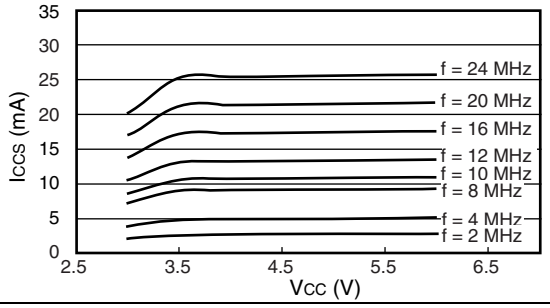

$I_{CCL} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



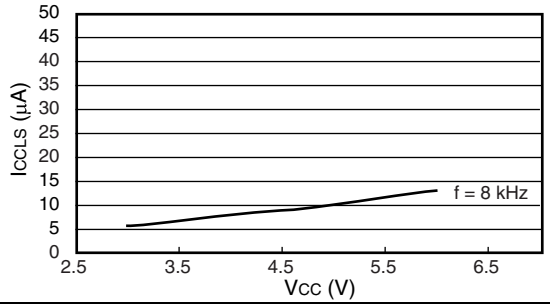

$I_{CCS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



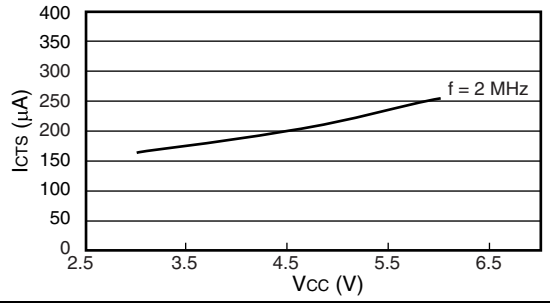

$I_{CCLS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



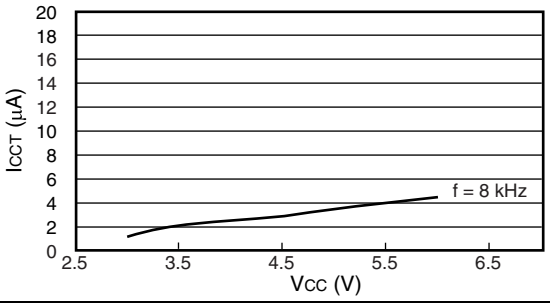

$I_{CTS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



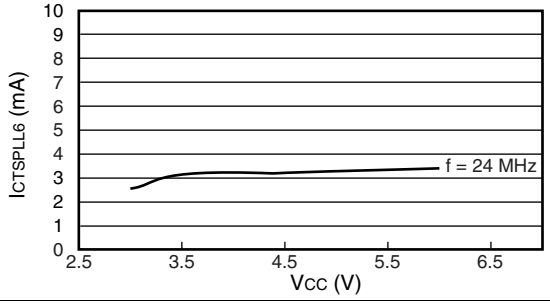

$I_{CCT} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



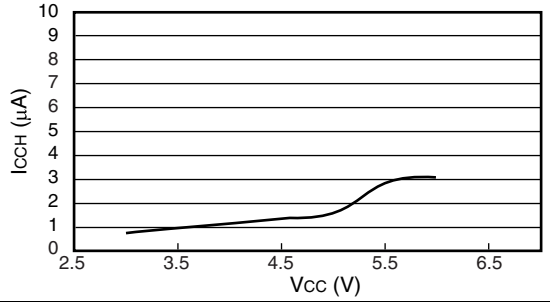

$I_{CTSPLL6} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



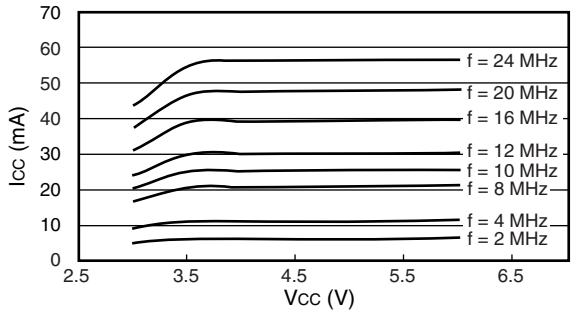

$I_{CCH} - V_{CC}$

$T_A = +25°C$, stopped

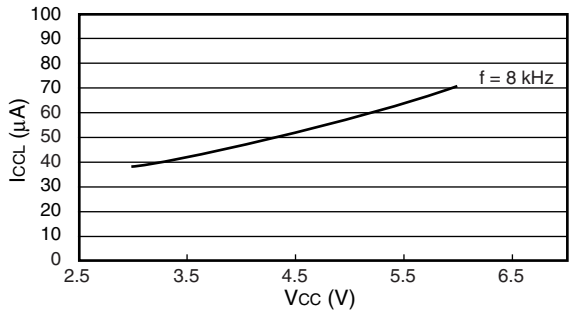


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

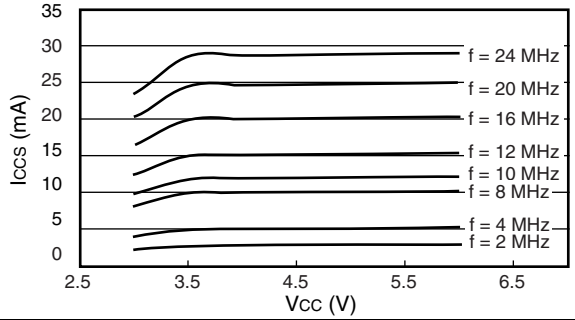
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



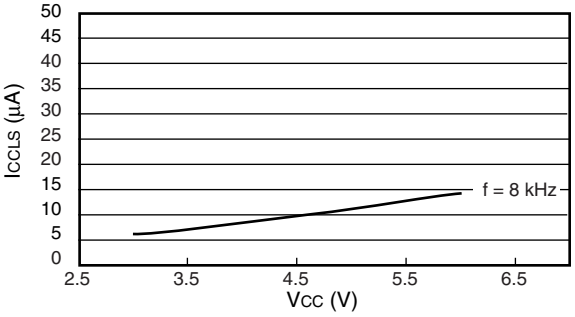

$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



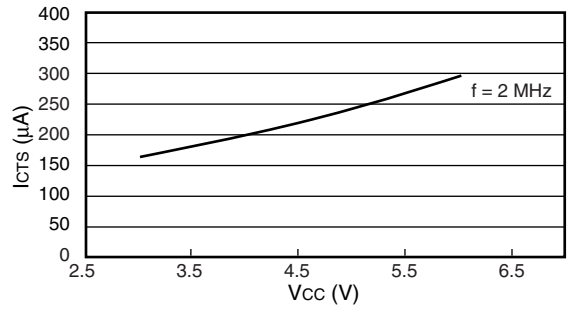

$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



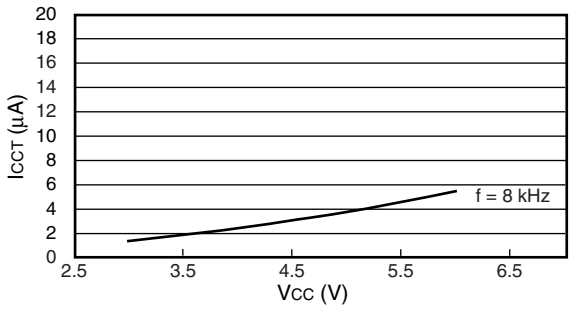

$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



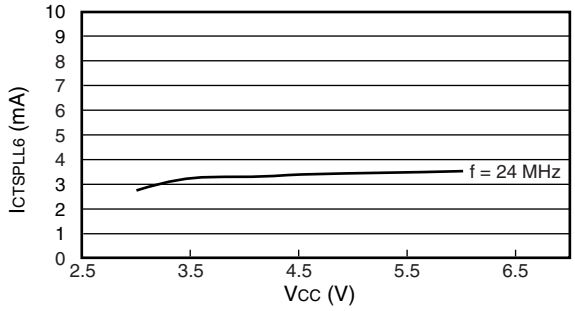

$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



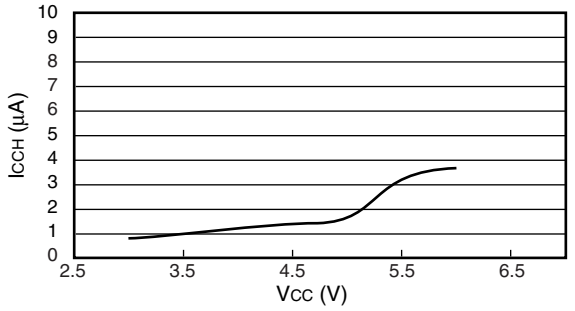

$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency




$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency




$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped



*(Continued)*

| Part number | Package | Remarks |
|---|---|---|
| MB90346EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90346ESPF | | |
| MB90346CEPF | | |
| MB90346CESPF | | |
| MB90346EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90346ESPMC | | |
| MB90346CEPMC | | |
| MB90346CESPMC | | |
| MB90347EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90347ESPF | | |
| MB90347CEPF | | |
| MB90347CESPF | | |
| MB90347EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90347ESPMC | | |
| MB90347CEPMC | | |
| MB90347CESPMC | | |
| MB90348EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90348ESPF | | |
| MB90348CEPF | | |
| MB90348CESPF | | |
| MB90348EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90348ESPMC | | |
| MB90348CEPMC | | |
| MB90348CESPMC | | |
| MB90349EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90349ESPF | | |
| MB90349CEPF | | |
| MB90349CESPF | | |
| MB90349EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90349ESPMC | | |
| MB90349CEPMC | | |
| MB90349CESPMC | | |
| MB90V340E-101CR | 299-pin ceramic PGA (PGA-299C-A01) | For evaluation |
| MB90V340E-102CR | | |