# Infineon Technologies - MB90347ESPMC-GS-334E1 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CANbus, EBI/EMI, LINbus, SCI, UART/USART |
| Peripherals | DMA, POR, WDT |
| Number of I/O | 82 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | Mask ROM |
| EEPROM Size | - |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 5.5V |
| Data Converters | A/D 16x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-334e1 |

## Contents

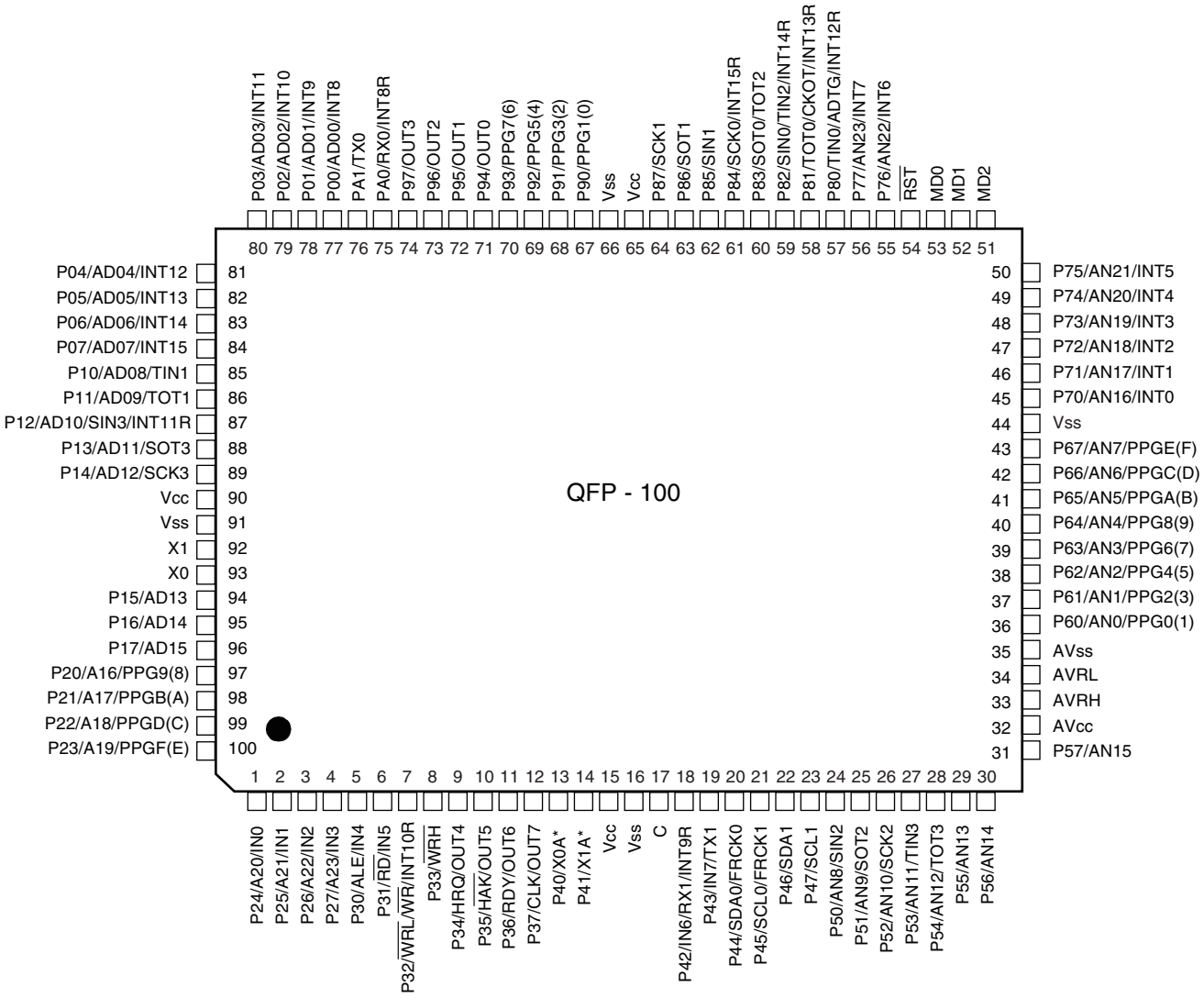
*(Continued)*

| Part Number / Parameter | MB90V340E-101, MB90V340E-102 | MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S) | MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) |
|---|---|---|---|
| External Interrupt (16 channels) | Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded intelligent I/O services (EI$^2$OS) and DMA | | |
| D/A Converter | 2 channels | — | |
| Sub clock (maximum 100 kHz) | Only for MB90V340E-102 | Devices with sub clock : devices without an S suffix in the part number<br>Devices without sub clock : devices with an S suffix in the part number | |
| I/O Ports | Virtually all external pins can be used as general purpose I/O port<br>All ports are push-pull outputs<br>Bit-wise settable as input/output or peripheral signal<br>Can be configured 8 as CMOS schmitt trigger/ automotive inputs (in blocks of 8 pins)<br>TTL input level settable for external bus (32-pin only for external bus) | | |
| Flash Memory | — | Supports automatic programming, Embedded Algorithm<br>Write/Erase/Erase-Suspend/Resume commands<br>A flag indicating completion of the algorithm<br>Number of erase cycles : 10000 cycles<br>Data retention time : 20 years<br>Boot block configuration<br>Erase can be performed on each block<br>Block protection with external programming voltage<br>Flash Security Feature for protecting the content of the Flash (except for MB90F346E(S) and MB90F346CE (S) ) | |

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01-E) is used.
Please refer to the Emulator operation manual for details.

■ MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)

(TOP VIEW)



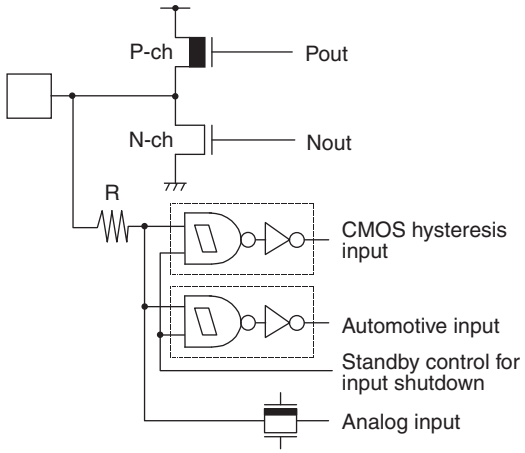
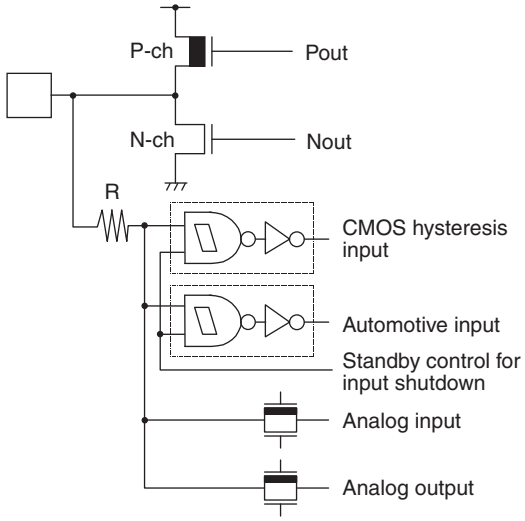
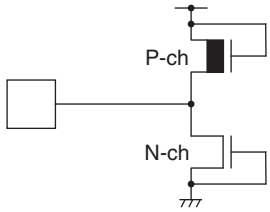
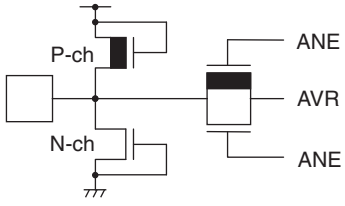

(FPT-100P-M06)

* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

*(Continued)*

| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 61 | 59 | P84 | F | General purpose I/O pin. |
| | | SCK0 | | Clock I/O pin for UART0 |
| | | INT15R | | External interrupt request input pin |
| 62 | 60 | P85 | M | General purpose I/O pin. |
| | | SIN1 | | Serial data input pin for UART1 |
| 63 | 61 | P86 | F | General purpose I/O pin. |
| | | SOT1 | | Serial data output pin for UART1 |
| 64 | 62 | P87 | F | General purpose I/O pin. |
| | | SCK1 | | Clock I/O pin for UART1 |
| 65 | 63 | $V_{CC}$ | — | Power (3.5 V to 5.5 V) input pin |
| 66 | 64 | $V_{SS}$ | — | GND pin |
| 67 to 70 | 65 to 68 | P90 to P93 | F | General purpose I/O pins |
| | | PPG1, 3, 5, 7 | | Output pins for PPGs |
| 71 to 74 | 69 to 72 | P94 to P97 | F | General purpose I/O pins |
| | | OUT0 to OUT3 | | Waveform output pins for output compares. This function is enabled when the OCU enables waveform output. |
| 75 | 73 | PA0 | F | General purpose I/O pin. |
| | | RX0 | | RX input pin for CAN0 Interface |
| | | INT8R | | External interrupt request input pin |
| 76 | 74 | PA1 | F | General purpose I/O pin. |
| | | TX0 | | TX Output pin for CAN0 |
| 77 to 84 | 75 to 82 | P00 to P07 | G | General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD00 to AD07 | | I/O pins for 8 lower bits of the external address/data bus.<br>This function is enabled when the external bus is enabled. |
| | | INT8 to INT15 | | External interrupt request input pins. |
| 85 | 83 | P10 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor.<br>This function is enabled in single-chip mode. |
| | | AD08 | | I/O pin for the external address/data bus.<br>This function is enabled when the external bus is enabled. |
| | | TIN1 | | Event input pin for the reload timer |

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| I |  | ■ CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>■ CMOS hysteresis input (with function to disconnect input during standby)<br>■ Automotive input (with function to disconnect input during standby)<br>■ A/D converter analog input |
| J |  | ■ CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>■ D/A analog output<br>■ CMOS hysteresis input (with function to disconnect input during standby)<br>■ Automotive input (with function to disconnect input during standby)<br>■ A/D converter analog input |
| K |  | Power supply input protection circuit |
| L |  | ■ A/D converter reference voltage power supply input pin, with the protection circuit<br>■ Flash memory devices do not have a protection circuit against $V_{CC}$ for pin AVRH |

### 5. Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply ($AV_{CC}$, AVRH, AVRL) and analog inputs (AN0 to AN23) after turning-on the digital power supply ($V_{CC}$).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or $AV_{CC}$ (turning on/off the analog and digital power supplies simultaneously is acceptable).

### 6. Connection of Unused A/D Converter Pins when the A/D Converter is Used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

### 7. Crystal Oscillator Circuit

The X0, X1 pins and X0A, X1A pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

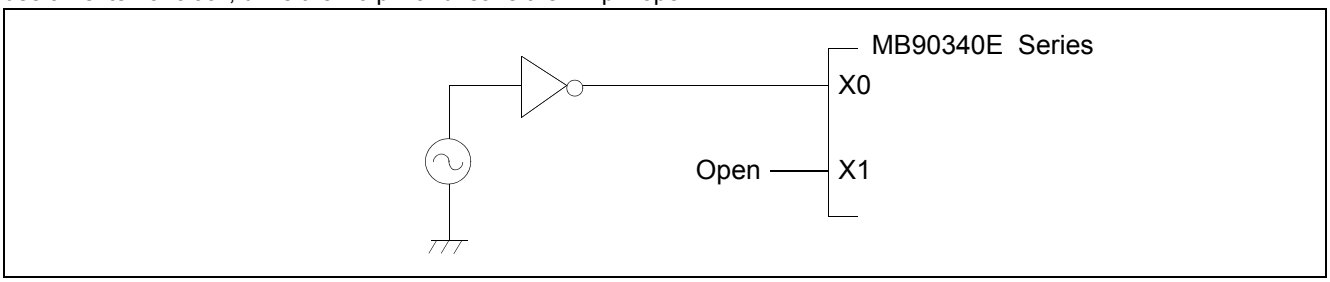
For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

### 8. Pull-up/down resistors

The MB90340E Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

### 9. Using external clock

To use an external clock, drive the X0 pin and leave the X1 pin open.




### 10. Precautions when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

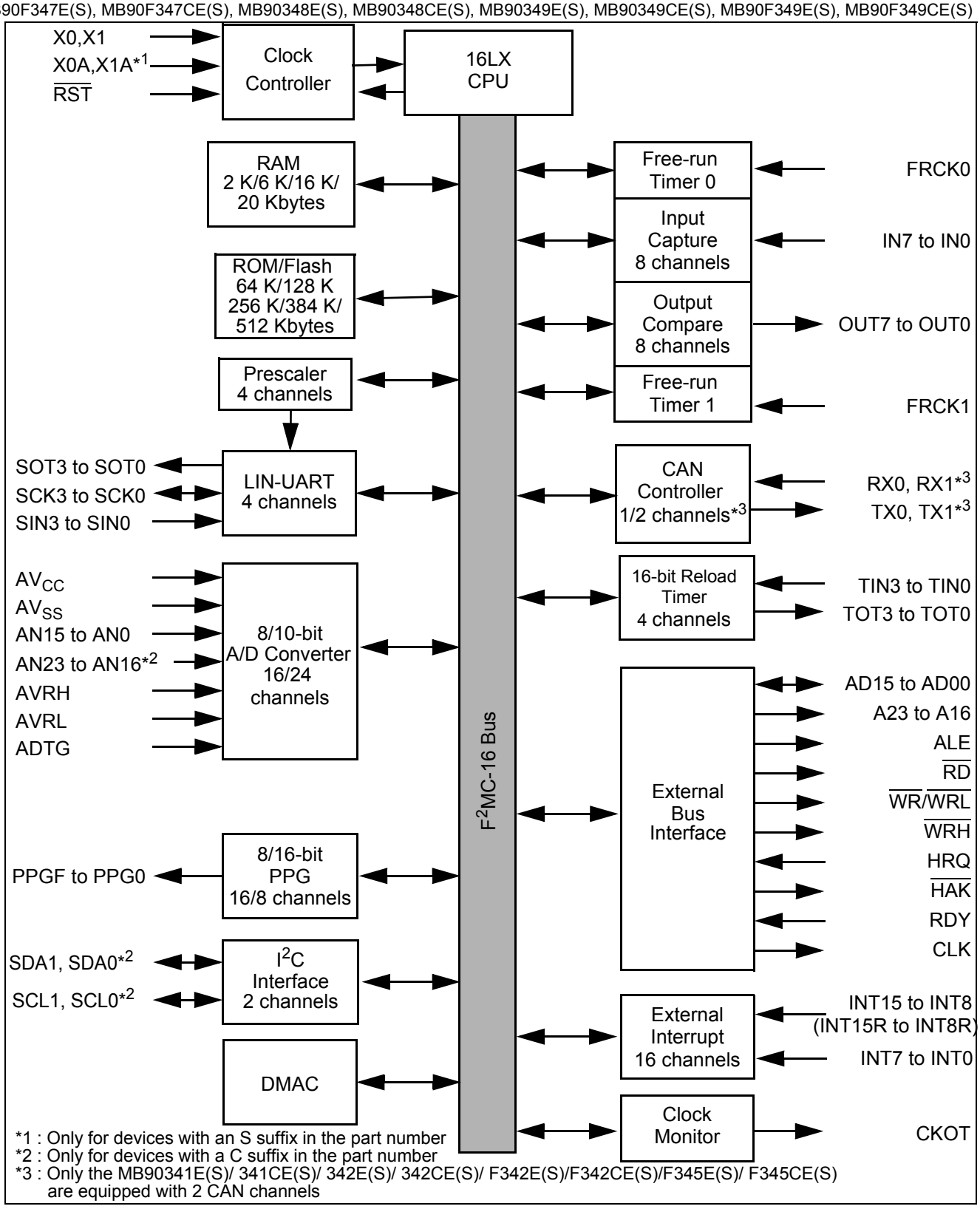
### 11. Notes on operation in PLL clock mode

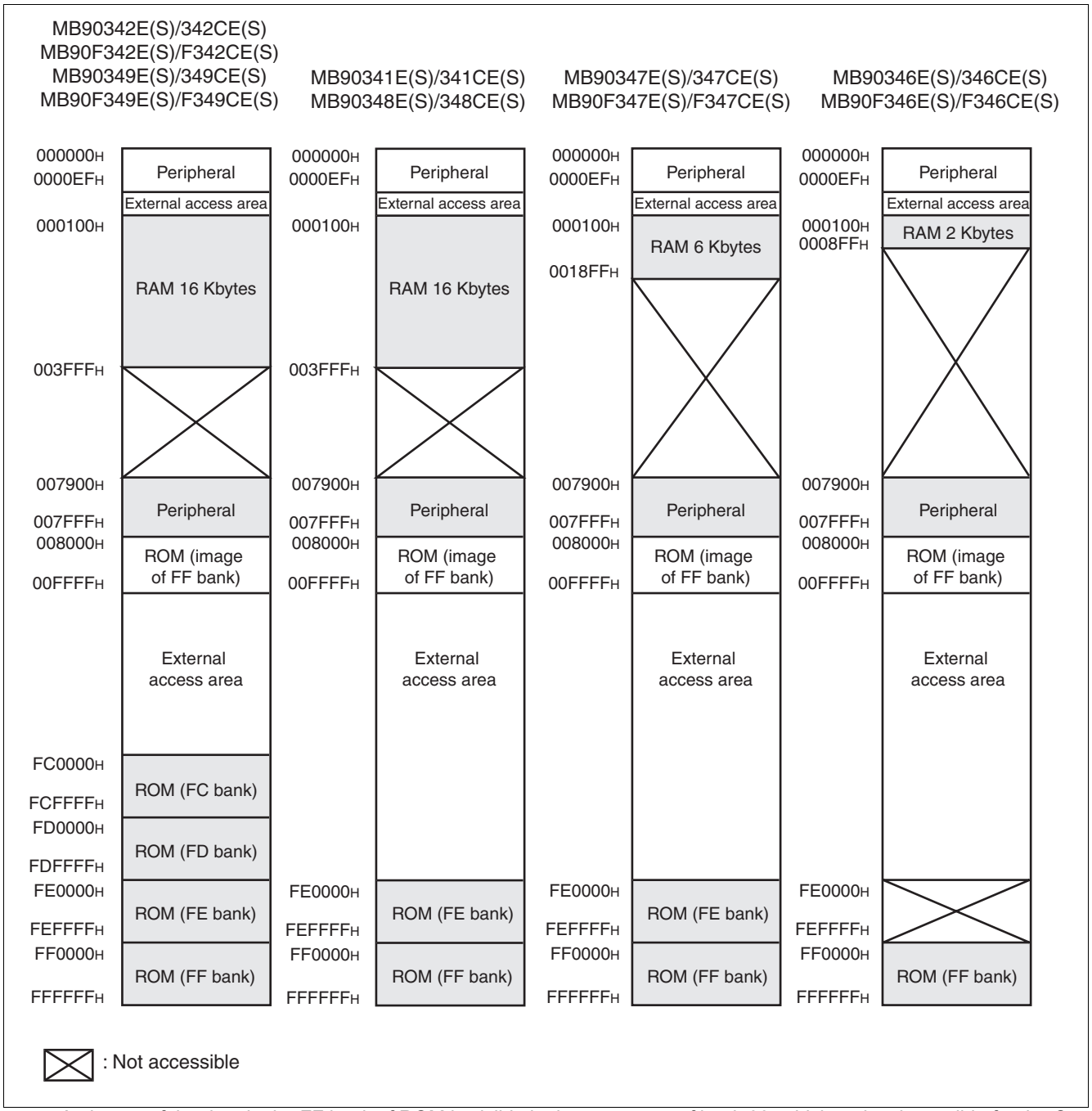
If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

### 12. Notes on Power-On

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50 µs or more (0.2 V to 2.7 V)

■ MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)






**Note:** :An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.
For example, when the address $00C000_H$ is accessed, the data at $FFC000_H$ in ROM is actually accessed.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
As a result, the image between $FF8000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF7FFF_H$ is visible only in bank FF.

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $007900_H$ | Reload Register L0 | PRLL0 | R/W | 16-bit PPG 0/1 | $XXXXXXXX_B$ |
| $007901_H$ | Reload Register H0 | PRLH0 | R/W | | $XXXXXXXX_B$ |
| $007902_H$ | Reload Register L1 | PRLL1 | R/W | | $XXXXXXXX_B$ |
| $007903_H$ | Reload Register H1 | PRLH1 | R/W | | $XXXXXXXX_B$ |
| $007904_H$ | Reload Register L2 | PRLL2 | R/W | 16-bit PPG 2/3 | $XXXXXXXX_B$ |
| $007905_H$ | Reload Register H2 | PRLH2 | R/W | | $XXXXXXXX_B$ |
| $007906_H$ | Reload Register L3 | PRLL3 | R/W | | $XXXXXXXX_B$ |
| $007907_H$ | Reload Register H3 | PRLH3 | R/W | | $XXXXXXXX_B$ |
| $007908_H$ | Reload Register L4 | PRLL4 | R/W | 16-bit PPG 4/5 | $XXXXXXXX_B$ |
| $007909_H$ | Reload Register H4 | PRLH4 | R/W | | $XXXXXXXX_B$ |
| $00790A_H$ | Reload Register L5 | PRLL5 | R/W | | $XXXXXXXX_B$ |
| $00790B_H$ | Reload Register H5 | PRLH5 | R/W | | $XXXXXXXX_B$ |
| $00790C_H$ | Reload Register L6 | PRLL6 | R/W | 16-bit PPG 6/7 | $XXXXXXXX_B$ |
| $00790D_H$ | Reload Register H6 | PRLH6 | R/W | | $XXXXXXXX_B$ |
| $00790E_H$ | Reload Register L7 | PRLL7 | R/W | | $XXXXXXXX_B$ |
| $00790F_H$ | Reload Register H7 | PRLH7 | R/W | | $XXXXXXXX_B$ |
| $007910_H$ | Reload Register L8 | PRLL8 | R/W | 16-bit PPG 8/9 | $XXXXXXXX_B$ |
| $007911_H$ | Reload Register H8 | PRLH8 | R/W | | $XXXXXXXX_B$ |
| $007912_H$ | Reload Register L9 | PRLL9 | R/W | | $XXXXXXXX_B$ |
| $007913_H$ | Reload Register H9 | PRLH9 | R/W | | $XXXXXXXX_B$ |
| $007914_H$ | Reload Register LA | PRLLA | R/W | 16-bit PPG A/B | $XXXXXXXX_B$ |
| $007915_H$ | Reload Register HA | PRLHA | R/W | | $XXXXXXXX_B$ |
| $007916_H$ | Reload Register LB | PRLLB | R/W | | $XXXXXXXX_B$ |
| $007917_H$ | Reload Register HB | PRLHB | R/W | | $XXXXXXXX_B$ |
| $007918_H$ | Reload Register LC | PRLLC | R/W | 16-bit PPG C/D | $XXXXXXXX_B$ |
| $007919_H$ | Reload Register HC | PRLHC | R/W | | $XXXXXXXX_B$ |
| $00791A_H$ | Reload Register LD | PRLLD | R/W | | $XXXXXXXX_B$ |
| $00791B_H$ | Reload Register HD | PRLHD | R/W | | $XXXXXXXX_B$ |
| $00791C_H$ | Reload Register LE | PRLLE | R/W | 16-bit PPG E/F | $XXXXXXXX_B$ |
| $00791D_H$ | Reload Register HE | PRLHE | R/W | | $XXXXXXXX_B$ |
| $00791E_H$ | Reload Register LF | PRLLF | R/W | | $XXXXXXXX_B$ |
| $00791F_H$ | Reload Register HF | PRLHF | R/W | | $XXXXXXXX_B$ |
| $007920_H$ | Input Capture 0 | IPCP0 | R | Input Capture 0/1 | $XXXXXXXX_B$ |
| $007921_H$ | Input Capture 0 | IPCP0 | R | | $XXXXXXXX_B$ |
| $007922_H$ | Input Capture 1 | IPCP1 | R | | $XXXXXXXX_B$ |
| $007923_H$ | Input Capture 1 | IPCP1 | R | | $XXXXXXXX_B$ |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $007948_H$ | Timer 0/Reload 0 | TMR0/TMRLR0 | R/W | 16-bit Reload Timer 0 | $XXXXXXXX_B$ |
| $007949_H$ | | | R/W | | $XXXXXXXX_B$ |
| $00794A_H$ | Timer 1/Reload 1 | TMR1/TMRLR1 | R/W | 16-bit Reload Timer 1 | $XXXXXXXX_B$ |
| $00794B_H$ | | | R/W | | $XXXXXXXX_B$ |
| $00794C_H$ | Timer 2/Reload 2 | TMR2/TMRLR2 | R/W | 16-bit Reload Timer 2 | $XXXXXXXX_B$ |
| $00794D_H$ | | | R/W | | $XXXXXXXX_B$ |
| $00794E_H$ | Timer 3/Reload 3 | TMR3/TMRLR3 | R/W | 16-bit Reload Timer 3 | $XXXXXXXX_B$ |
| $00794F_H$ | | | R/W | | $XXXXXXXX_B$ |
| $007950_H$ | Serial Mode Register 3 | SMR3 | W,R/W | UART3 | $00000000_B$ |
| $007951_H$ | Serial Control Register 3 | SCR3 | W,R/W | | $00000000_B$ |
| $007952_H$ | Reception/Transmission Data Register 3 | RDR3/TDR3 | R/W | | $00000000_B$ |
| $007953_H$ | Serial Status Register 3 | SSR3 | R,R/W | | $00001000_B$ |
| $007954_H$ | Extended Communication Control Register 3 | ECCR3 | R,W, R/W | | $000000XX_B$ |
| $007955_H$ | Extended Status Control Register | ESCR3 | R/W | | $00000100_B$ |
| $007956_H$ | Baud Rate Generator Register 30 | BGR30 | R/W | | $00000000_B$ |
| $007957_H$ | Baud Rate Generator Register 31 | BGR31 | R/W | | $00000000_B$ |
| $007958_H$ | Serial Mode Register 4 | SMR4 | W,R/W | UART4 | $00000000_B$ |
| $007959_H$ | Serial Control Register 4 | SCR4 | W,R/W | | $00000000_B$ |
| $00795A_H$ | Reception/Transmission Data Register 4 | RDR4/TDR4 | R/W | | $00000000_B$ |
| $00795B_H$ | Serial Status Register 4 | SSR4 | R,R/W | | $00001000_B$ |
| $00795C_H$ | Extended Communication Control Register 4 | ECCR4 | R,W, R/W | | $000000XX_B$ |
| $00795D_H$ | Extended Status Control Register | ESCR4 | R/W | | $00000100_B$ |
| $00795E_H$ | Baud Rate Generator Register 40 | BGR40 | R/W | | $00000000_B$ |
| $00795F_H$ | Baud Rate Generator Register 41 | BGR41 | R/W | | $00000000_B$ |
| $007960_H$ to $00796B_H$ | Reserved | | | | |
| $00796C_H$ | Clock Output Enable Register | CLKR | R/W | Clock Monitor | $XXXX0000_B$ |
| $00796D_H$ | Reserved | | | | |
| $00796E_H$ | CAN Direct Mode Register | CDMR | R/W | CAN Clock sync | $XXXXXXX0_B$ |
| $00796F_H$ | CAN Switch Register | CANSWR | R/W | CAN 0/1 | $XXXXXX00_B$ |

*(Continued)*

# 11. Electrical Characteristics

## 11.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1 | $V_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | |
| | $AV_{CC}$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | $V_{CC} = AV_{CC}$*2 |
| | AVRH, AVRL | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | $AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH $\geq$ AVRL |
| Input voltage*1 | $V_I$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | *3 |
| Output voltage*1 | $V_O$ | $V_{SS} - 0.3$ | $V_{SS} + 6.0$ | V | *3 |
| Maximum Clamp Current | $I_{CLAMP}$ | −4.0 | +4.0 | mA | *5 |
| Total Maximum Clamp Current | $\Sigma\lvert I_{CLAMP}\rvert$ | — | 40 | mA | *5 |
| “L” level maximum output current | $I_{OL}$ | — | 15 | mA | *4, *6 |
| “L” level average output current | $I_{OLAV}$ | — | 4 | mA | *4, *7 |
| “L” level maximum overall output current | $\Sigma I_{OL}$ | — | 100 | mA | *4 |
| “L” level average overall output current | $\Sigma I_{OLAV}$ | — | 50 | mA | *4, *8 |
| “H” level maximum output current | $I_{OH}$ | — | −15 | mA | *4, *6 |
| “H” level average output current | $I_{OHAV}$ | — | −4 | mA | *4, *7 |
| “H” level maximum overall output current | $\Sigma I_{OH}$ | — | −100 | mA | *4 |
| “H” level average overall output current | $\Sigma I_{OHAV}$ | — | −50 | mA | *4, *8 |
| Power consumption | $P_D$ | — | 450 | mW | |
| Operating temperature | $T_A$ | −40 | +105 | °C | |
| Storage temperature | $T_{STG}$ | −55 | +150 | °C | |

*1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V

*2: Set $AV_{CC}$ and $V_{CC}$ to the same voltage. Make sure that $AV_{CC}$ does not exceed $V_{CC}$ and that the voltage at the analog inputs does not exceed $AV_{CC}$ when the power is switched on.

*3: $V_I$ and $V_O$ should not exceed $V_{CC} + 0.3$ V. $V_I$ should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the $I_{CLAMP}$ rating supersedes the $V_I$ rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, PA1

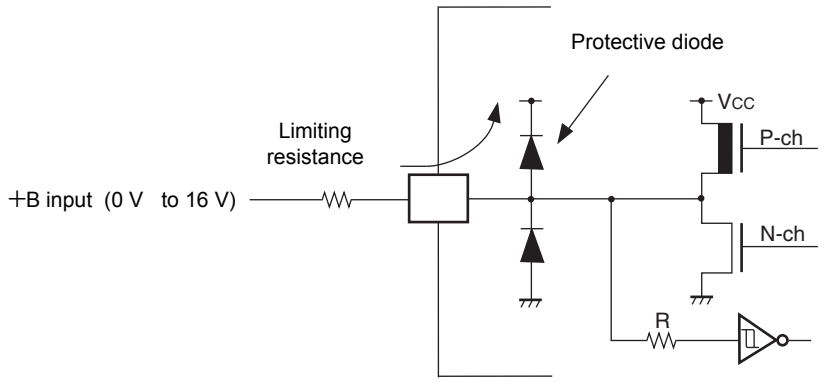
*5:
- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (Evaluation device : P50 to P55) , P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1
- Use within recommended operating conditions.
- Use with DC voltage (current)
- The +B signal should always be applied by using a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed the rated value, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.

*(Continued)*

*(Continued)*

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

■ Input/output equivalent circuits




*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

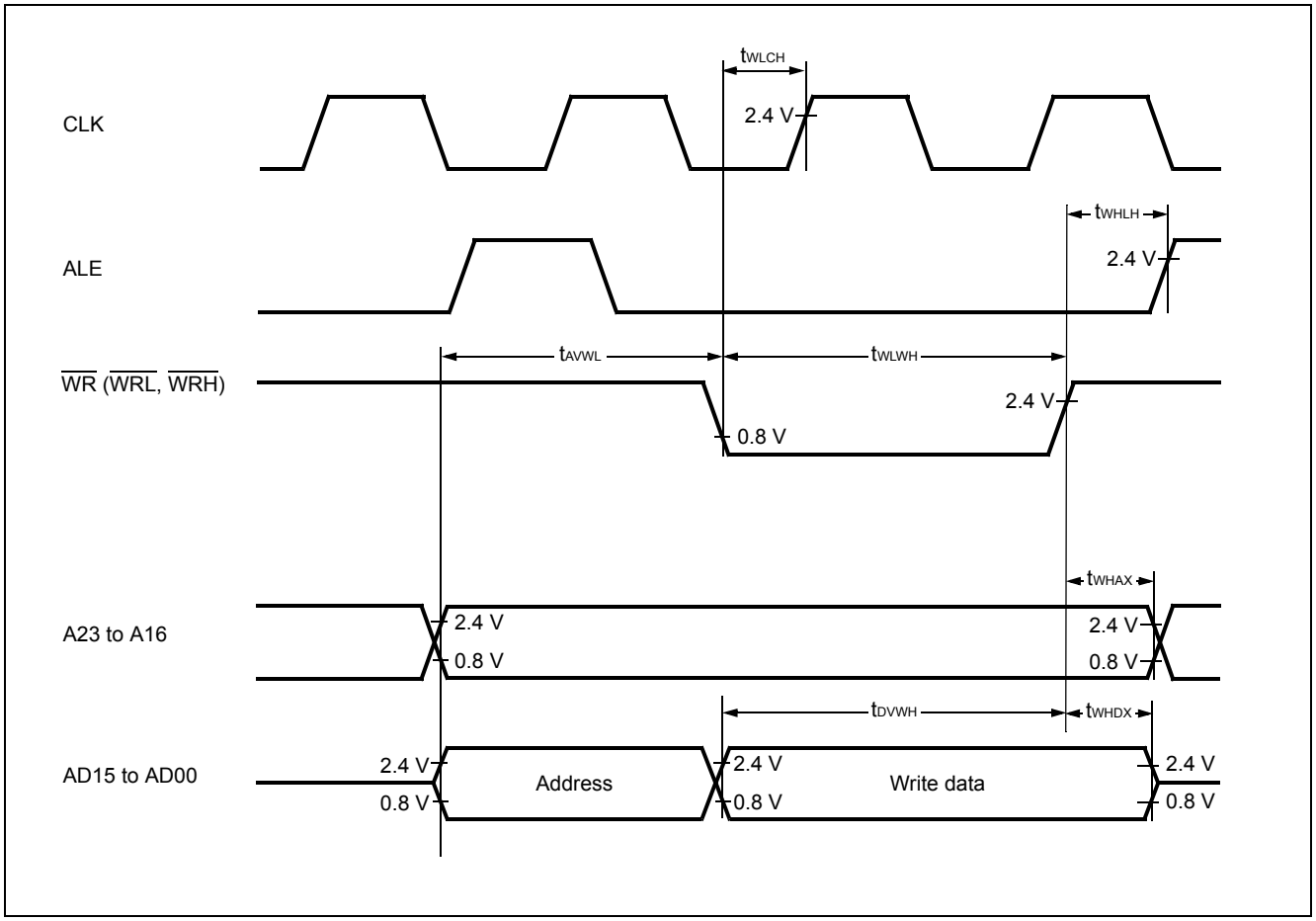
*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

### 11.4.6 Bus Timing (Write)

($T_A$ = −40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $f_{CP}$ ≤ 24 MHz)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Valid address → $\overline{WR}$ ↓ time | $t_{AVWL}$ | A23 to A16, AD15 to AD00, $\overline{WR}$ | — | $t_{CP}$−15 | — | ns |
| $\overline{WR}$ pulse width | $t_{WLWH}$ | $\overline{WR}$ | | 3 $t_{CP}$/2 − 20 | — | ns |
| Valid data output → $\overline{WR}$ ↑ time | $t_{DVWH}$ | AD15 to AD00, $\overline{WR}$ | | 3 $t_{CP}$/2 − 20 | — | ns |
| $\overline{WR}$ ↑ → Data hold time | $t_{WHDX}$ | AD15 to AD00, $\overline{WR}$ | | 15 | — | ns |
| $\overline{WR}$ ↑ → Address valid time | $t_{WHAX}$ | A23 to A16, $\overline{WR}$ | | $t_{CP}$/2 − 10 | — | ns |
| $\overline{WR}$ ↑ → ALE ↑ time | $t_{WHLH}$ | $\overline{WR}$, ALE | | $t_{CP}$/2 − 15 | — | ns |
| $\overline{WR}$ ↓ → CLK ↑ time | $t_{WLCH}$ | $\overline{WR}$, CLK | | $t_{CP}$/2 − 15 | — | ns |



*11.4.9 LIN-UART0/1/2/3*

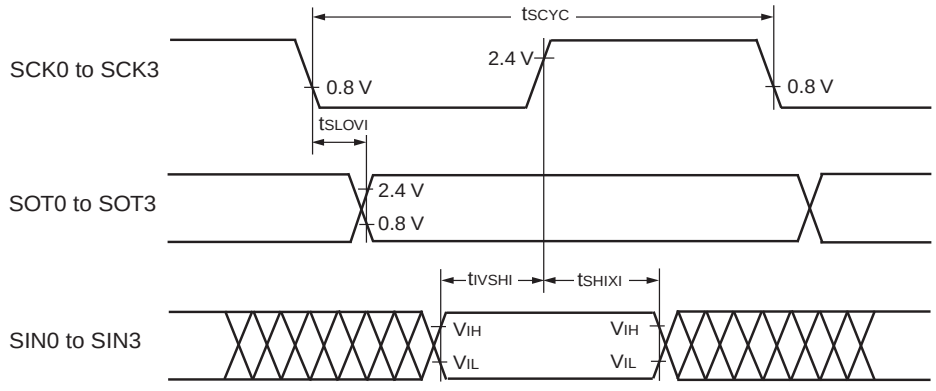
■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0**

($T_A$ = −40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

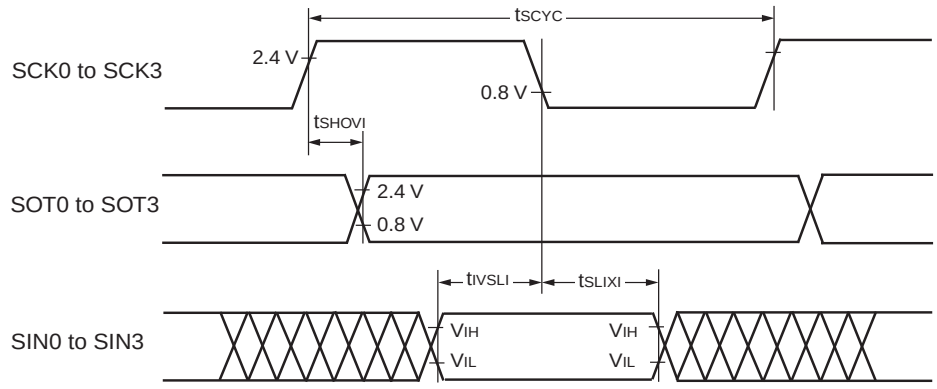
| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal shift clock mode output pins are $C_L$ = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | −50 | +50 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXI}$ | SCK0 to SCK3, SIN0 to SIN3 | | 0 | — | ns |
| Serial clock “L” pulse width | $t_{SHSL}$ | SCK0 to SCK3 | External shift clock mode output pins are $C_L$ = 80 pF + 1 TTL. | 3 $t_{CP}$ - $t_R$ | — | ns |
| Serial clock “H” pulse width | $t_{SLSH}$ | SCK0 to SCK3 | | $t_{CP}$ + 10 | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCK0 to SCK3, SOT0 to SOT3 | | — | 2 $t_{CP}$ + 60 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHE}$ | SCK0 to SCK3, SIN0 to SIN3 | | 30 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXE}$ | SCK0, SCK1, SIN0 to SIN3 | | $t_{CP}$ + 30 | — | ns |
| SCK fall time | $t_F$ | SCK0 to SCK3 | | — | 10 | ns |
| SCK rise time | $t_R$ | SCK0 to SCK3 | | — | 10 | ns |

**Note:**
- AC characteristic in CLK synchronized mode.
- $C_L$ is load capacity value of pins when testing.
- $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

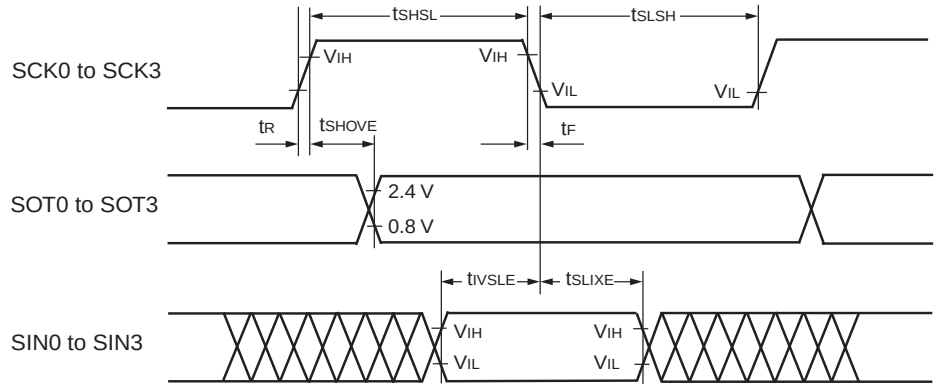
- Internal Shift Clock Mode



- Internal Shift Clock Mode




- External Shift Clock Mode

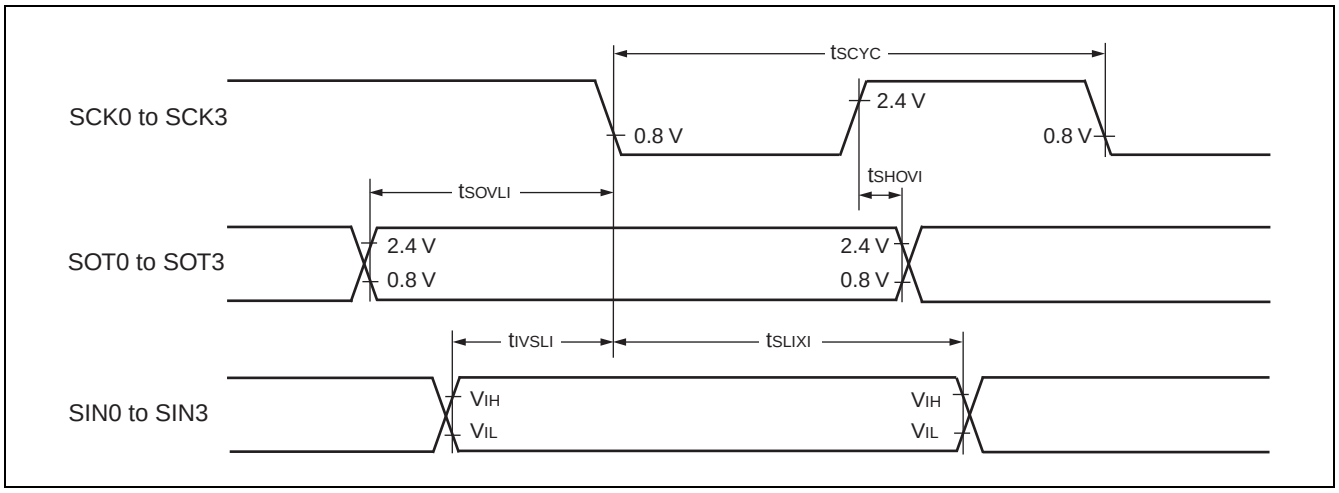


■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1**

($T_A$ = −40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

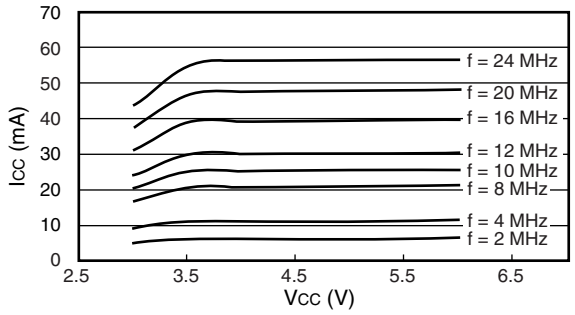
| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal clock operation output pins are $C_L$ = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | −50 | +50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↓ → Valid SIN hold time | $t_{SLIXI}$ | SCK0 to SCK3, SIN0 to SIN3 | | 0 | — | ns |
| SOT → SCK ↓ delay time | $t_{SOVLI}$ | SCK0 to SCK3, SOT0 to SOT3 | | 3 $t_{CP}$ − 70 | — | ns |

**Note:**
- $C_L$ is load capacity value of pins when testing.
- $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".

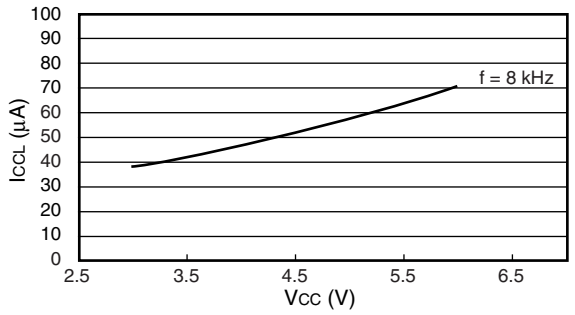


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

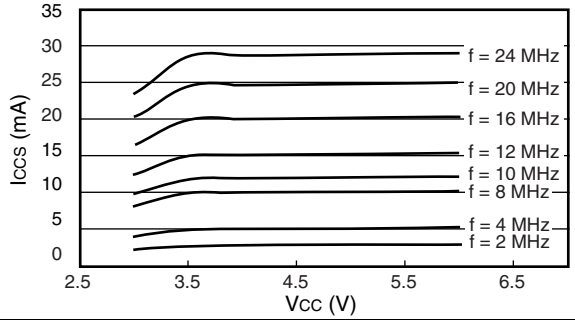
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



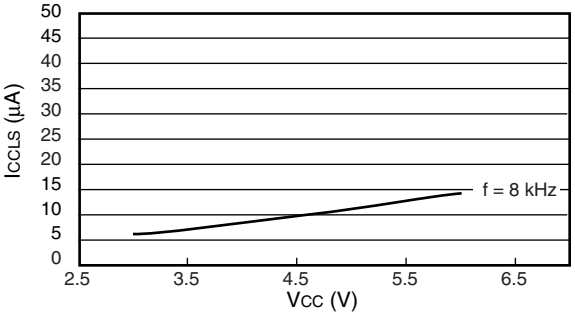

$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



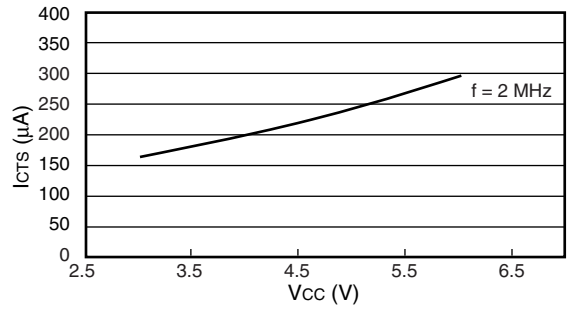

$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



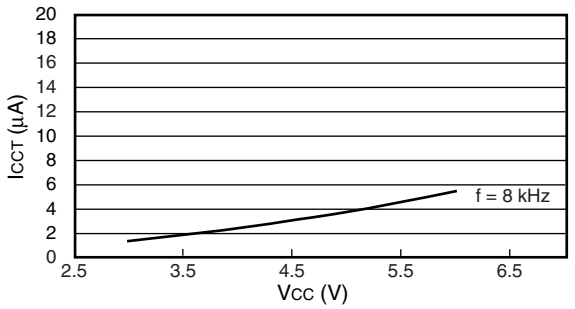

$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



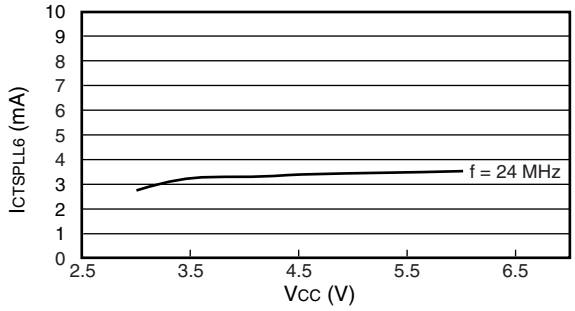

$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



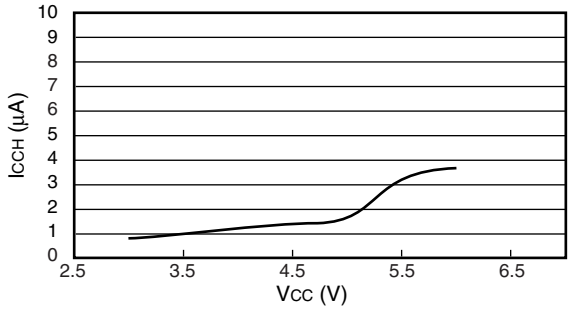

$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency




$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency

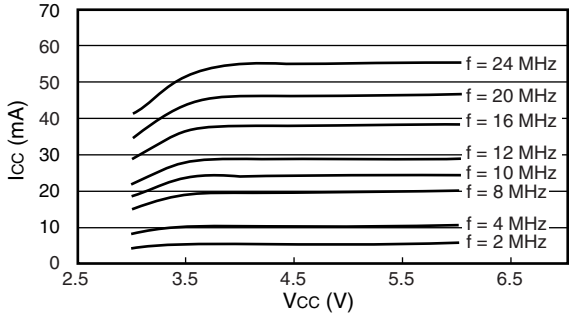



$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

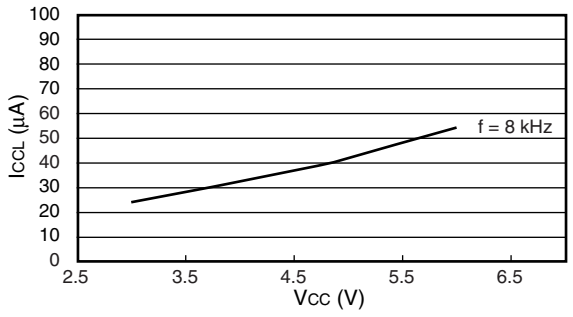


■ MB90347E, MB90347ES, MB90347CE, MB90347CES

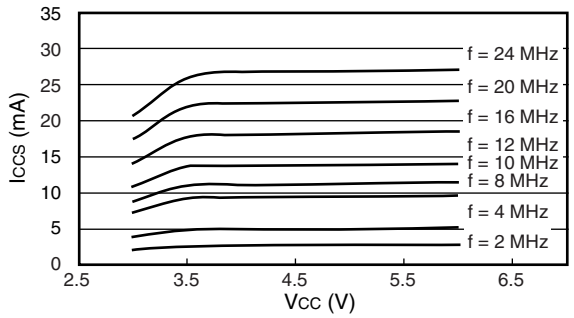
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



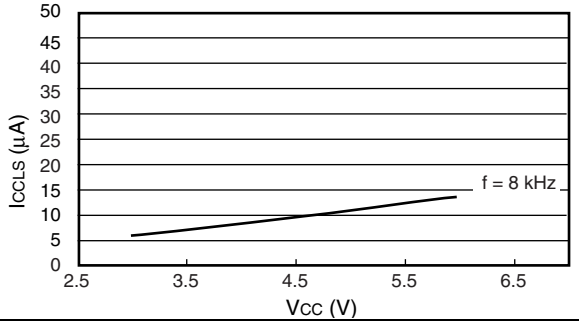

$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



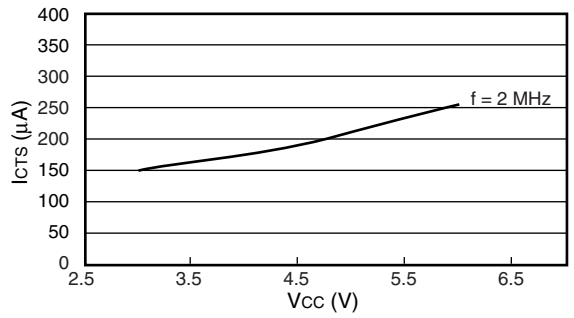

$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



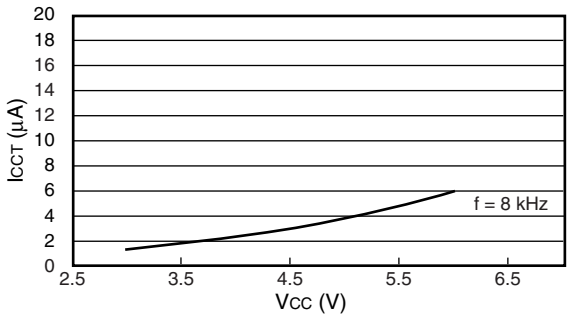

$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



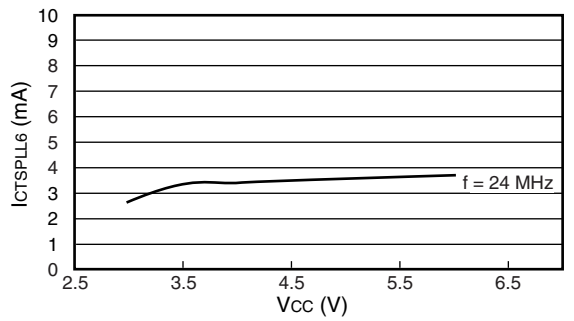

$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



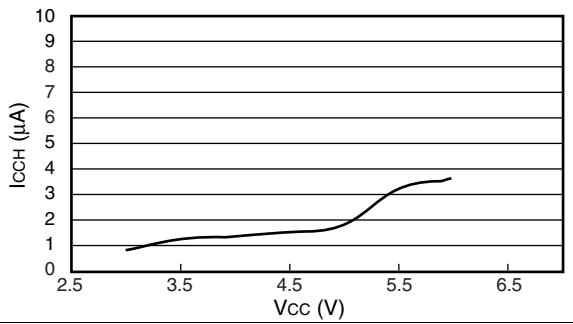

$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



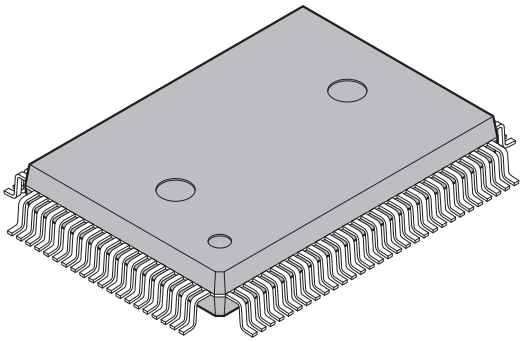

$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency




$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

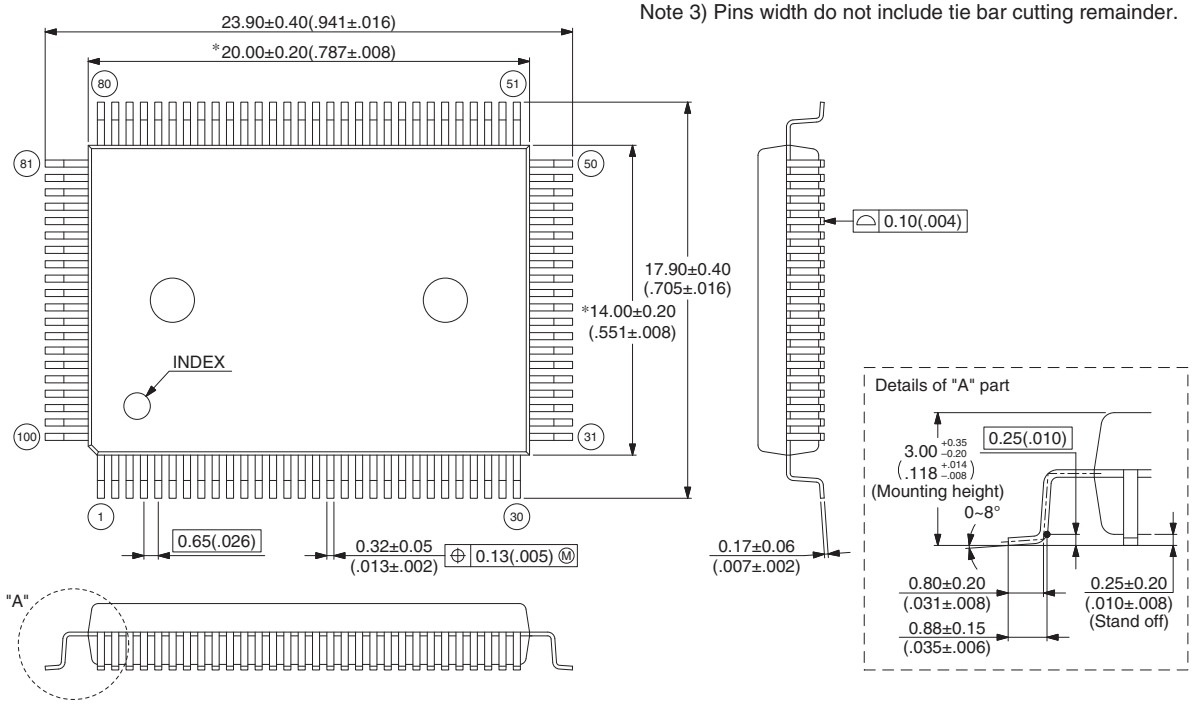


*(Continued)*

| 100-pin plastic QFP | | |
|---|---|---|
|  | Lead pitch | 0.65 mm |
| | Package width × package length | 14.00 × 20.00 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 3.35 mm MAX |
| | Code (Reference) | P-QFP100-14×20-0.65 |
| (FPT-100P-M06) | | |

100-pin plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values.

## 15. Major Changes

**Spansiion Publication Number: DS07-13747-4E**

| Page | Section | Change Results |
|---|---|---|
| ___ | ___ | Deleted the part numbers;<br>MB90F343E(S), MB90F343CE(S) |
| 51 | Electrical Characteristics<br>Absolute Maximum Ratings | Added “*6” in remark for “L" level maximum output current and “H” level maximum output current.<br>Added “*7” in remark for “L" level average output current and “H” level average output current.<br>Added “*8” in remark for “L"level average overall output current and “H” level average overall output current. |
| 52 | | Added as follows.<br>“*6:The maximum output current is defined as the peak value of the current of any one of the corresponding pins.”<br>“*7:The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.”<br>“*8:The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.” |

**NOTE: Please see “Document History” about later revised information.**

# Document History

| Document Title: MB90340E Series F2MC-16LX 16-bit Microcontroller Datasheet<br>Document Number: 002-04498 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | — | AKIH | 08/23/2010 | Migrated to Cypress and assigned document number 002-04498.<br>No change to document contents or format. |
| *A | 5221535 | AKIH | 05/04/2016 | Updated to Cypress template |