





Welcome to **E-XFL.COM** 

What is "Embedded - Microcontrollers"?

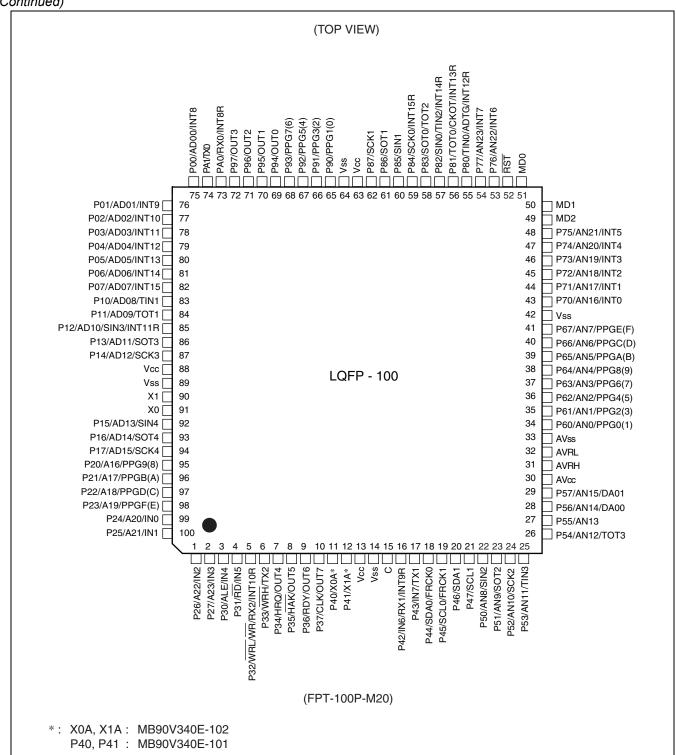
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	F <sup>2</sup> MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-458e1







This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.



Pin No.			I/O				
QFP100* <sup>1</sup>	LQFP100*2	Pin name	Circuit type*3	Function			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to A is applied to AV <sub>CC</sub> .			
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter			
35	33	AV <sub>SS</sub>	K	Analog GND pin for the A/D Converter			
		P60 to P67		General purpose I/O pins.			
36 to 43	34 to 41	AN0 to AN7	],	Analog input pins for the A/D converter			
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs			
44	42	$V_{SS}$		GND pin			
		P70 to P75		General purpose I/O pins.			
45 to 50	43 to 48	AN16 to AN21	I	Analog input pins for the A/D converter (devices with a C suffix in the part number)			
		INT0 to INT5		External interrupt request input pins			
51	49	MD2	D	Input pin for specifying the operating mode.			
52, 53	50, 51	MD1, MD0	С	Input pins for specifying the operating mode.			
54	52	RST	E	Reset input pin			
		P76, P77		General purpose I/O pins.			
55, 56	53, 54	AN22, AN23	1	Analog input pins for the A/D converter (devices with a C suffix in the part number)			
		INT6, INT7		External interrupt request input pins			
		P80		General purpose I/O pin.			
57	55	TIN0	]	Event input pin for the reload timer			
57	55	ADTG	<b>-</b>	Trigger input pin for the A/D converter			
		INT12R		External interrupt request input pin			
		P81		General purpose I/O pin.			
58	56	ТОТ0	] F	Output pin for the reload timer			
30	56	СКОТ	<b>-</b>	Output pin for the clock monitor			
		INT13R		External interrupt request input pin			
		P82		General purpose I/O pin.			
59	57	SIN0	] <sub>M</sub>	Serial data input pin for UART0			
วิช	57	TIN2	] IVI	Event input pin for the reload timer			
		INT14R		External interrupt request input pin			
		P83		General purpose I/O pin.			
60	58	SOT0	F	Serial data output pin for UART0			
		TOT2		Output pin for the reload timer			



Pir	ı No.		I/O				
QFP100*1	LQFP100*2	Pin name	Circuit type*3	Function			
		P11		General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.			
86	84	AD09	G	I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.			
		TOT1		Output pin for the reload timer			
		P12		General purpose I/O pin. The register can be set to select whether to use a pull-up resistor.  This function is enabled in single-chip mode.			
87	85	AD10	N I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.				
		SIN3		Serial data input pin for UART3			
		INT11R	1	External interrupt request input pin			
		P13		General purpose I/O pin. The register can be set to select whether to use a pull-up resistor.  This function is enabled in single-chip mode.			
88	86	AD11	I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.				
		SOT3	1	Serial data output pin for UART3			
		P14		General purpose I/O pin. The register can be set to select whether to use a pull-up resistor.  This function is enabled in single-chip mode.			
89	87	AD12	I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.				
		SCK3		Clock I/O pin for UART3			
90	88	V <sub>CC</sub>	_	Power (3.5 V to 5.5 V) input pin			
91	89	V <sub>SS</sub>		GND pin			
92	90	X1	Α	Main clock output pin			
93	91	X0	7^	Main clock input pin			
94	92	P15	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor.  This function is enabled in single-chip mode.			
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.			
95	93	P16	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor.  This function is enabled in single-chip mode.			
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.			



Type	Circuit	Remarks
1	P-ch Nout  R  CMOS hysteresis input  Automotive input  Standby control for input shutdown  Analog input	<ul> <li>■ CMOS level output (I<sub>OL</sub> = 4 mA, I<sub>OH</sub> = -4 mA)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ A/D converter analog input</li> </ul>
J	P-ch Pout  N-ch Nout  R  CMOS hysteresis input  Automotive input  Standby control for input shutdown  Analog input  Analog output	<ul> <li>■ CMOS level output (I<sub>OL</sub> = 4 mA, I<sub>OH</sub> = -4 mA)</li> <li>■ D/A analog output</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ A/D converter analog input</li> </ul>
к	P-ch N-ch	Power supply input protection circuit
L	P-ch ANE AVR AVR ANE	<ul> <li>A/D converter reference voltage power supply input pin, with the protection circuit</li> <li>Flash memory devices do not have a protection circuit against V<sub>CC</sub> for pin AVRH</li> </ul>



Туре	Circuit	Remarks
M	P-ch Pout  N-ch Nout  R  Automotive input  Standby control for input shutdown	<ul> <li>■ CMOS level output (I<sub>OL</sub> = 4 mA, I<sub>OH</sub> = -4 mA)</li> <li>■ CMOS input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> </ul>
N	Pull-up control  P-ch Pout  N-ch Nout  R  TTL input  Standby control for input shutdown	<ul> <li>■ CMOS level output (I<sub>OL</sub> = 4 mA, I<sub>OH</sub> = −4 mA)</li> <li>■ CMOS input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ TTL input (with function to disconnect input during standby)</li> <li>Programmable pull-up resistor: 50 kΩ approx</li> </ul>
0	P-ch Pout  Nout  R  CMOS input  Automotive input  Standby control for input shutdown  Analog input	<ul> <li>■ CMOS level output (I<sub>OL</sub> = 4 mA, I<sub>OH</sub> = -4 mA)</li> <li>■ CMOS input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ A/D converter analog input</li> </ul>



# 5. Handling Devices

#### 1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than V<sub>CC</sub> or lower than V<sub>SS</sub> is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V<sub>CC</sub> and V<sub>SS</sub> pins.
- The AV<sub>CC</sub> power supply is applied before the V<sub>CC</sub> voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV<sub>CC</sub>, AVRH) exceed the digital power-supply voltage.

## 2. Handling unused pins

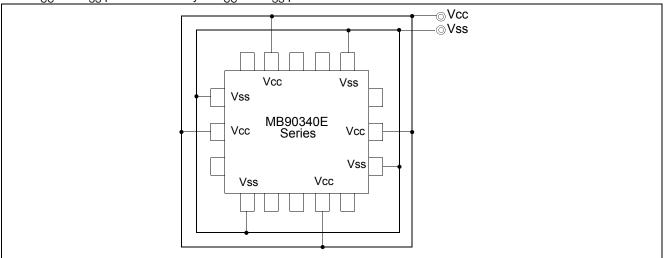
Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 k $\Omega$  or more.

## 3. Power supply pins (V<sub>CC</sub>/V<sub>SS</sub>)

■ If there are multiple V<sub>CC</sub> and V<sub>SS</sub> pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the  $V_{CC}$  and  $V_{SS}$  pins to the power supply and ground externally. Connect  $V_{CC}$  and  $V_{SS}$  pins to the device from the current supply source at a possibly low impedance.

■ As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1  $\mu$ F as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  pins in the vicinity of  $V_{CC}$  and  $V_{SS}$  pins of the device.



#### 4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to  $V_{CC}$  or  $V_{SS}$  pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to  $V_{CC}$  or  $V_{SS}$  pins and to provide a low-impedance connection.



# Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV $_{CC}$ , AVRH, AVRL) and analog inputs (AN0 to AN23) after turning-on the digital power supply (V $_{CC}$ ).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or  $AV_{CC}$  (turning on/off the analog and digital power supplies simultaneously is acceptable).

### 6. Connection of Unused A/D Converter Pins when the A/D Converter is Used

Connect unused pins of A/D converter to  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AVRH = AVRL = V_{SS}$ .

# 7. Crystal Oscillator Circuit

The X0, X1 pins and X0A, X1A pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

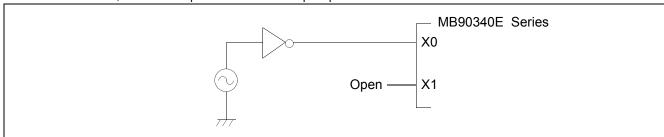
For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

## 8. Pull-up/down resistors

The MB90340E Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

### 9. Using external clock

To use an external clock, drive the X0 pin and leave the X1 pin open.



# 10.Precautions when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

# 11. Notes on operation in PLL clock mode

If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

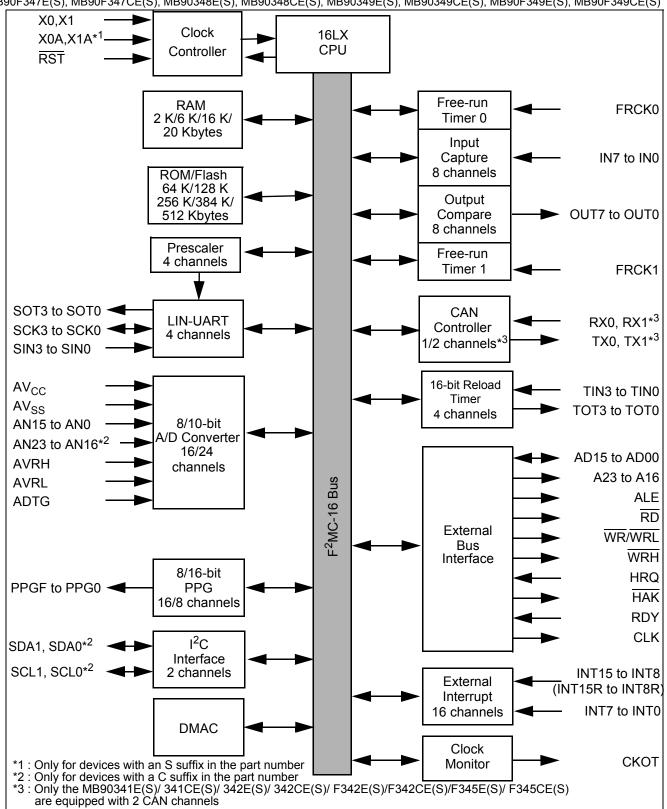
#### 12.Notes on Power-On

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50  $\mu$ s or more (0.2 V to 2.7 V)

Document Number: 002-04498 Rev. \*A



■ MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345CE(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346CE(S), MB90F346CE(S), MB90347CE(S), MB90347CE(S), MB90F347CE(S), MB90F347CE(S), MB90F349CE(S), MB90F34CE(S), MB90F34CE(S), MB90F34CE(S), MB90F34CE(S), MB90F3AC(S), MB90F3AC(S), MB90F3AC(S), MB90F3AC(S), MB90F3AC(S),





Address	Register	Abbreviation	Access	Resource name	Initial value
000060 <sub>H</sub>	Timer Control Status 0	TMCSR0	R/W	16-bit Reload	00000000 <sub>B</sub>
000061 <sub>H</sub>	Timer Control Status 0	TMCSR0	R/W	Timer 0	XXXX0000 <sub>B</sub>
000062 <sub>H</sub>	Timer Control Status 1	TMCSR1	R/W	16-bit Reload	00000000 <sub>B</sub>
000063 <sub>H</sub>	Timer Control Status 1	TMCSR1	R/W	Timer 1	XXXX0000 <sub>B</sub>
000064 <sub>H</sub>	Timer Control Status 2	TMCSR2	R/W	16-bit Reload	00000000 <sub>B</sub>
000065 <sub>H</sub>	Timer Control Status 2	TMCSR2	R/W	Timer 2	XXXX0000 <sub>B</sub>
000066 <sub>H</sub>	Timer Control Status 3	TMCSR3	R/W	16-bit Reload	00000000 <sub>B</sub>
000067 <sub>H</sub>	Timer Control Status 3	TMCSR3	R/W	Timer 3	XXXX0000 <sub>B</sub>
000068 <sub>H</sub>	A/D Control Status 0	ADCS0	R/W		000XXXX0 <sub>B</sub>
000069 <sub>H</sub>	A/D Control Status 1	ADCS1	R/W		0000000X <sub>B</sub>
00006A <sub>H</sub>	A/D Data 0	ADCR0	R	1.00	00000000 <sub>B</sub>
00006B <sub>H</sub>	A/D Data 1	ADCR1	R	A/D Converter	XXXXXX00 <sub>B</sub>
00006C <sub>H</sub>	ADC Setting 0	ADSR0	R/W		00000000 <sub>B</sub>
00006D <sub>H</sub>	ADC Setting 1	ADSR1	R/W		00000000 <sub>B</sub>
00006E <sub>H</sub>	Reserved	1		1	•
00006F <sub>H</sub>	ROM Mirror Function Select	ROMM	W	ROM Mirror	XXXXXXX1 <sub>B</sub>
000070 <sub>H</sub> to 00008F <sub>H</sub>	Reserved for CAN Controller 0/1. Refer to	"CAN Controllers"			
000090 <sub>H</sub>	Pasanyad	O/ II V CONTIONED			
	Reserved	CANA CONTROLLER			
000090 <sub>H</sub> to 00009A <sub>H</sub>	Reserved  DMA Descriptor Channel Specified Register	DCSR	R/W		00000000 <sub>B</sub>
000090 <sub>H</sub> to 00009A <sub>H</sub>	DMA Descriptor Channel Specified		R/W	DMA	00000000 <sub>B</sub>
000090 <sub>H</sub> to 00009A <sub>H</sub> 00009B <sub>H</sub>	DMA Descriptor Channel Specified Register	DCSR		DMA	
000090 <sub>H</sub> to 00009A <sub>H</sub> 00009B <sub>H</sub> 00009C <sub>H</sub>	DMA Descriptor Channel Specified Register DMA Status L Register	DCSR DSRL	R/W	DMA Address Match Detection 0	00000000 <sub>B</sub>
000090 <sub>H</sub> 100009A <sub>H</sub> 100009B <sub>H</sub> 100009C <sub>H</sub> 100009D <sub>H</sub>	DMA Descriptor Channel Specified Register DMA Status L Register DMA Status H Register	DCSR DSRL DSRH	R/W R/W	Address Match	00000000 <sub>B</sub>
000090 <sub>H</sub> 00009B <sub>H</sub> 00009C <sub>H</sub> 00009D <sub>H</sub> 00009E <sub>H</sub>	DMA Descriptor Channel Specified Register  DMA Status L Register  DMA Status H Register  Address Detect Control Register 0  Delayed Interrupt Trigger/Release	DCSR DSRL DSRH PACSR0	R/W R/W	Address Match Detection 0	00000000 <sub>B</sub> 00000000 <sub>B</sub>
000090 <sub>H</sub> 00009B <sub>H</sub> 00009C <sub>H</sub> 00009B <sub>H</sub> 00009C <sub>H</sub> 00009D <sub>H</sub>	DMA Descriptor Channel Specified Register  DMA Status L Register  DMA Status H Register  Address Detect Control Register 0  Delayed Interrupt Trigger/Release Register	DCSR DSRL DSRH PACSR0 DIRR	R/W R/W R/W	Address Match Detection 0  Delayed Interrupt  Low Power	00000000 <sub>B</sub> 00000000 <sub>B</sub> 00000000 <sub>B</sub>
000090 <sub>H</sub>	DMA Descriptor Channel Specified Register  DMA Status L Register  DMA Status H Register  Address Detect Control Register 0  Delayed Interrupt Trigger/Release Register  Low-power Mode Control Register	DCSR DSRL DSRH PACSR0 DIRR LPMCR	R/W R/W R/W R/W W,R/W	Address Match Detection 0  Delayed Interrupt  Low Power Control Circuit  Low Power	00000000 <sub>B</sub> 00000000 <sub>B</sub> 00000000 <sub>B</sub> XXXXXXX0 <sub>B</sub>



# 9. CAN Controllers

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
- Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
- 29-bit ID and 8-byte data
- Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
- Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

# List of Control Registers (1)

Address		Dominton	Abbassistica	A	Initial Value	
CAN0	CAN1		Abbreviation	Access	Initial Value	
000070 <sub>H</sub>	000080 <sub>H</sub>	Message Buffer	BVALR	R/W	00000000 <sub>B</sub>	
000071 <sub>H</sub>	000081 <sub>H</sub>	Valid Register	BVALR	R/VV	00000000B	
000072 <sub>H</sub>	000082 <sub>H</sub>	Transmit Request	TREQR	R/W	00000000 <sub>R</sub>	
000073 <sub>H</sub>	000083 <sub>H</sub>	Register	IREQR	R/VV	00000000B	
000074 <sub>H</sub>	000084 <sub>H</sub>	Transmit Cancel	TCAND		00000000 <sub>R</sub>	
000075 <sub>H</sub>	000085 <sub>H</sub>	Register	TCANR	W	00000000B	
000076 <sub>H</sub>	000086 <sub>H</sub>	Transmission	TCR	R/W	00000000 <sub>R</sub>	
000077 <sub>H</sub>	000087 <sub>H</sub>	Complete Register	TCR	IN/VV	00000000B	
000078 <sub>H</sub>	000088 <sub>H</sub>	Receive Complete	DOD	R/W	00000000 <sub>R</sub>	
000079 <sub>H</sub>	000089 <sub>H</sub>	Register	RCR	R/VV	00000000B	
00007A <sub>H</sub>	00008A <sub>H</sub>	Remote Request	DDTDD	DAM	00000000 <sub>R</sub>	
00007B <sub>H</sub>	00008B <sub>H</sub>	Receiving Register	RRTRR	R/W	00000000B	
00007C <sub>H</sub>	00008C <sub>H</sub>	Receive Overrun	DOVIDD	DAM	00000000 <sub>R</sub>	
00007D <sub>H</sub>	00008D <sub>H</sub>	Register	ROVRR	R/W	00000000B	
00007E <sub>H</sub>	00008E <sub>H</sub>	Reception Interrupt	DIED	DAM	00000000 <sub>R</sub>	
00007F <sub>H</sub>	00008F <sub>H</sub>	Enable Register	RIER	R/W	00000000B	

Document Number: 002-04498 Rev. \*A



# List of Message Buffers (DLC Registers and Data Registers) (1)

Address		B	A11		1.20.176.1	
CAN0	CAN1		Abbreviation	Access	Initial Value	
007A60 <sub>H</sub>	007C60 <sub>H</sub>	DI O Danistan O	DI ODO	DAM	2000000	
007A61 <sub>H</sub>	007C61 <sub>H</sub>	DLC Register 0	DLCR0	R/W	XXXXXXXX <sub>B</sub>	
007A62 <sub>H</sub>	007C62 <sub>H</sub>	DI O De vieter 4	DI OD4	DAM	2000000	
007A63 <sub>H</sub>	007C63 <sub>H</sub>	DLC Register 1	DLCR1	R/W	XXXXXXXXB	
007A64 <sub>H</sub>	007C64 <sub>H</sub>	DI C Decistes 2	DI CDO	DAM	VVVVVVV	
007A65 <sub>H</sub>	007C65 <sub>H</sub>	DLC Register 2	DLCR2	R/W	XXXXXXXXB	
007A66 <sub>H</sub>	007C66 <sub>H</sub>	DLC Pogistor 2	DLCR3	R/W	vvvvvvv	
007A67 <sub>H</sub>	007C67 <sub>H</sub>	DLC Register 3	DLCR3	R/VV	XXXXXXXX <sub>B</sub>	
007A68 <sub>H</sub>	007C68 <sub>H</sub>	DLC Pogistor 4	DLCR4	R/W	vvvvvvv	
007A69 <sub>H</sub>	007C69 <sub>H</sub>	DLC Register 4	DLCR4	R/VV	XXXXXXXXB	
007A6A <sub>H</sub>	007C6A <sub>H</sub>	DI C Dogistor F	DI CDE	R/W	vvvvvvv	
007A6B <sub>H</sub>	007C6B <sub>H</sub>	DLC Register 5	DLCR5	R/VV	XXXXXXXXB	
007A6C <sub>H</sub>	007C6C <sub>H</sub>	DLC Register 6	DLCR6	R/W	XXXXXXXX <sub>B</sub>	
007A6D <sub>H</sub>	007C6D <sub>H</sub>	DLC Register 0	DLCKO	IV VV	~~~~~B	
007A6E <sub>H</sub>	007C6E <sub>H</sub>	— DLC Register 7	DLCR7	R/W	XXXXXXXX <sub>B</sub>	
007A6F <sub>H</sub>	007C6F <sub>H</sub>	DLC Register 7	DLCKI	IN/ VV	YYYYYYY B	
007A70 <sub>H</sub>	007C70 <sub>H</sub>	DLC Register 8	DLCR8	R/W	XXXXXXXX <sub>B</sub>	
007A71 <sub>H</sub>	007C71 <sub>H</sub>	DLC Register 6	DLCKO		~~~~~B	
007A72 <sub>H</sub>	007C72 <sub>H</sub>	DLC Register 9	DLCR9	R/W	XXXXXXXX <sub>B</sub>	
007A73 <sub>H</sub>	007C73 <sub>H</sub>	DEC Register 9	DEGING		XXXXXXXB	
007A74 <sub>H</sub>	007C74 <sub>H</sub>	DLC Register 10	DLCR10	R/W	XXXXXXXX <sub>B</sub>	
007A75 <sub>H</sub>	007C75 <sub>H</sub>	DEC Register 10	DECIVIO	1000	XXXXXXXB	
007A76 <sub>H</sub>	007C76 <sub>H</sub>	DLC Register 11	DLCR11	R/W	XXXXXXXX <sub>B</sub>	
007A77 <sub>H</sub>	007C77 <sub>H</sub>	DEC Register 11	DEGITT	TV VV	XXXXXXXB	
007A78 <sub>H</sub>	007C78 <sub>H</sub>	— DLC Register 12	DLCR12	R/W	XXXXXXXX <sub>B</sub>	
007A79 <sub>H</sub>	007C79 <sub>H</sub>	DEC Register 12	DEGITIZ	TV VV	XXXXXXXB	
007A7A <sub>H</sub>	007C7A <sub>H</sub>	— DLC Register 13	DLCR13	R/W	XXXXXXXX <sub>B</sub>	
007A7B <sub>H</sub>	007C7B <sub>H</sub>	DEO Negister 13	DEGICIO	I V V V	WWW B	
007A7C <sub>H</sub>	007C7C <sub>H</sub>	DLC Register 14	DLCR14	R/W	XXXXXXXX <sub>B</sub>	
007A7D <sub>H</sub>	007C7D <sub>H</sub>	DEO Negister 14	DEGICIT	I V V V	WWW B	
007A7E <sub>H</sub>	007C7E <sub>H</sub>	DLC Register 15	DLCR15	R/W	XXXXXXXX <sub>B</sub>	
007A7F <sub>H</sub>	007C7F <sub>H</sub>	DEO ROGISTO 15	DEOICIO	1000	700000B	

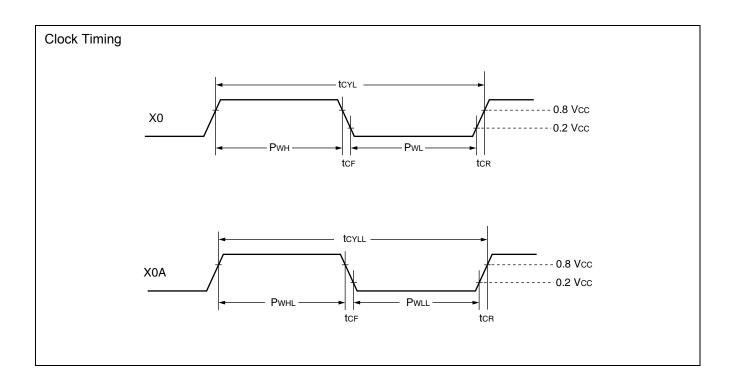


# 11.3 DC Characteristics

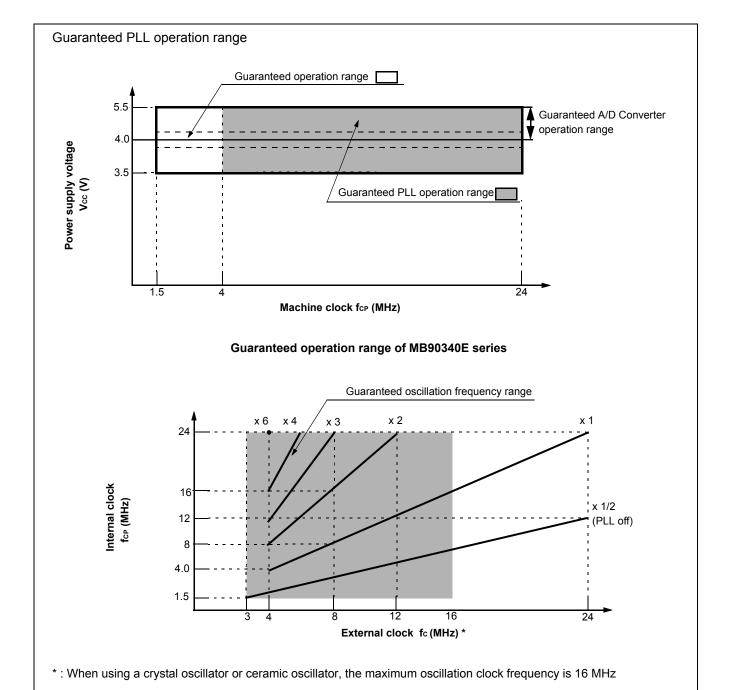
(T<sub>A</sub> = -40°C to +105°C, V<sub>CC</sub> = 5.0 V  $\pm$  10%, f<sub>CP</sub> $\leq$  24 MHz, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Davamatav	Symb	Dia	Condition	Value		I I ton! 4	Damanka		
Parameter	ol	Pin	Condition	Min	Тур	Max	Unit	Remarks	
	V <sub>IHS</sub>		_	0.8 V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)	
	$V_{IHA}$			0.8 V <sub>CC</sub>		$V_{CC} + 0.3$	V	Port inputs if Automotive input levels are selected	
Input H voltage	V <sub>IHT</sub>			2.0		$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected	
(At $V_{CC} = 5 \text{ V} \pm 10\%$ )	V <sub>IHS</sub>		_	0.7 V <sub>CC</sub>		$V_{CC} + 0.3$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected	
	V <sub>IHI</sub>			0.7 V <sub>CC</sub>		$V_{CC} + 0.3$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected	
	V <sub>IHR</sub>		_	0.8 V <sub>CC</sub>		$V_{CC} + 0.3$	V	RST input pin (CMOS hysteresis)	
	$V_{IHM}$	_		$V_{CC} - 0.3$		$V_{CC} + 0.3$	V	MD input pin	
	V <sub>ILS</sub>		_	V <sub>SS</sub> - 0.3		0.2 V <sub>CC</sub>	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)	
	V <sub>ILA</sub>			V <sub>SS</sub> - 0.3		0.5 V <sub>CC</sub>	V	Port inputs if Automotive input levels are selected	
Input L	V <sub>ILT</sub>			V <sub>SS</sub> - 0.3		0.8	V	Port inputs if TTL input levels are selected	
voltage (At $V_{CC} = 5 \text{ V} \pm 10\%$ )	V <sub>ILS</sub>			V <sub>SS</sub> - 0.3		0.3 V <sub>CC</sub>	V	P12, P50, P82, P85 inputs if CMOS input levels are selected	
	V <sub>ILI</sub>			V <sub>SS</sub> - 0.3		0.3 V <sub>CC</sub>	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected	
	$V_{ILR}$			$V_{SS} - 0.3$		0.2 V <sub>CC</sub>	V	RST input pin (CMOS hysteresis)	
	$V_{ILM}$			$V_{SS} - 0.3$		$V_{SS} + 0.3$	V	MD input pin	
Output H voltage	V <sub>OH</sub>	Normal outputs	$V_{CC} = 4.5 \text{ V},$ $I_{OH} = -4.0 \text{ mA}$	V <sub>CC</sub> — 0.5			V		
Output H voltage	V <sub>OHI</sub>	I <sup>2</sup> C current outputs	$V_{CC} = 4.5 \text{ V},$ $I_{OH} = -3.0 \text{ mA}$	V <sub>CC</sub> — 0.5			V		
Output L voltage	V <sub>OL</sub>	Normal outputs	$V_{CC} = 4.5 \text{ V},$ $I_{OL} = 4.0 \text{ mA}$			0.4	V		
Output L voltage	V <sub>OLI</sub>	I <sup>2</sup> C current outputs	$V_{CC} = 4.5 \text{ V},$ $I_{OL} = 3.0 \text{ mA}$			0.4	V		







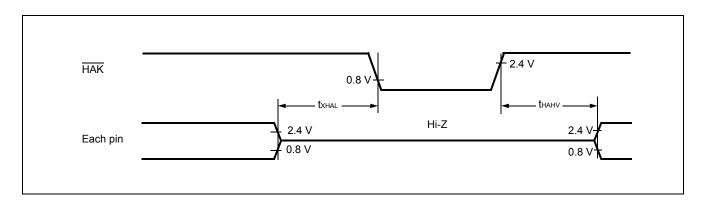




# 11.4.8 Hold Timing

Parameter	Symbol	Pin	Condition	Value		Unit	
Farameter	Syllibol	FIII	Condition	Min	Max	Oilit	
Pin floating $\rightarrow \overline{HAK} \downarrow time$	t <sub>XHAL</sub>	HAK		30	t <sub>CP</sub>	ns	
HAK ↑ time → Pin valid time	t <sub>HAHV</sub>	HAK		t <sub>CP</sub>	2 t <sub>CP</sub>	ns	

**Note:** : There is more than 1 cycle from when HRQ reads in until the HAK is changed.





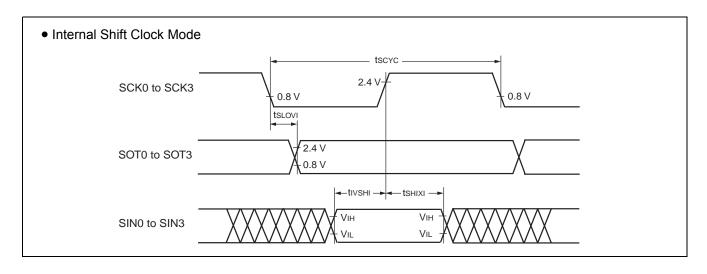
### 11.4.9 LIN-UART0/1/2/3

# ■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

Dorometer	Cumbal	Pin	Condition	Va	Value		
Parameter	Symbol	PIII	Condition	Min	Max	Unit	
Serial clock cycle time	t <sub>SCYC</sub>	SCK0 to SCK3		5 t <sub>CP</sub>		ns	
$SCK \downarrow \to SOT$ delay time	t <sub>SLOVI</sub>	SCK0 to SCK3, SOT0 to SOT3	Internal shift clock	-50	+50	ns	
Valid SIN → SCK↑	t <sub>IVSHI</sub>	SCK0 to SCK3, SIN0 to SIN3	mode output pins are $C_L = 80 \text{ pF} + 1 \text{ TTL}.$	t <sub>CP</sub> + 80		ns	
SCK ↑ → Valid SIN hold time	t <sub>SHIXI</sub>	SCK0 to SCK3, SIN0 to SIN3		0		ns	
Serial clock "L" pulse width	t <sub>SHSL</sub>	SCK0 to SCK3		3 t <sub>CP</sub> - t <sub>R</sub>	—	ns	
Serial clock "H" pulse width	t <sub>SLSH</sub>	SCK0 to SCK3		t <sub>CP</sub> + 10		ns	
$SCK \downarrow \  o \ SOT$ delay time	t <sub>SLOVE</sub>	SCK0 to SCK3, SOT0 to SOT3		_	2 t <sub>CP</sub> + 60	ns	
Valid SIN → SCK↑	t <sub>IVSHE</sub>	SCK0 to SCK3, SIN0 to SIN3	External shift clock mode output pins are CL = 80 pF + 1 TTL.	30	_	ns	
SCK ↑ → Valid SIN hold time	t <sub>SHIXE</sub>	SCK0, SCK1, SIN0 to SIN3		t <sub>CP</sub> + 30	_	ns	
SCK fall time	t <sub>F</sub>	SCK0 to SCK3			10	ns	
SCK rise time	t <sub>R</sub>	SCK0 to SCK3			10	ns	

### Note:

- AC characteristic in CLK synchronized mode.
- C<sub>L</sub> is load capacity value of pins when testing.
  t<sub>CP</sub> is internal operating clock cycle time (machine clock) . Refer to " (1) Clock Timing".





# 11.5 A/D Converter

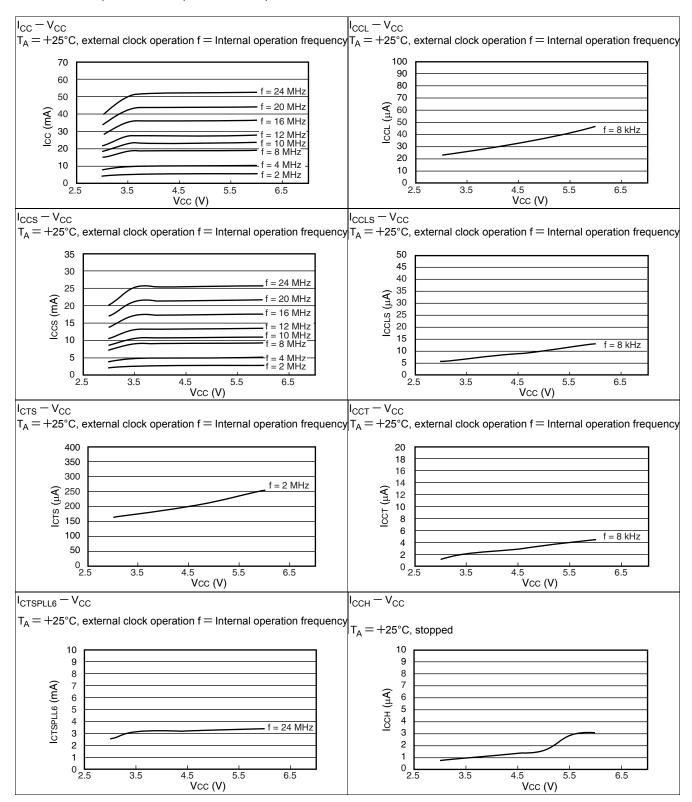
 $(T_{A} = -40 ^{\circ} C \text{ to } +105 ^{\circ} C, \ 3.0 \ V \leq \text{AVRH} - \text{AVRL}, \ V_{CC} = \text{AV}_{CC} = 5.0 \ \text{V} \pm 10 \%, \ f_{CP} \leq 24 \ \text{MHz}, \ V_{SS} = \text{AV}_{SS} = 0 \ \text{V})$ 

Donomoton	Value					I I sa !4	Domonico
Parameter	Symbol	Pin	Min	Тур	Max	Unit	Remarks
Resolution					10	bit	
Total error			_		±3.0	LSB	
Nonlinearity error			_		±2.5	LSB	
Differential nonlinearity error	_	_	_	_	±1.9	LSB	
Zero reading voltage	V <sub>OT</sub>	AN0 to AN23	AVRL - 1.5 × LSB	AVRL + 0.5 × LSB	AVRL + 2.5 × LSB	V	
Full scale reading voltage	V <sub>FST</sub>	AN0 to AN23	AVRH - 3.5 × LSB	AVRH - 1.5 × LSB	AVRH + 0.5 × LSB	V	
Compare time			1.0		16500		$4.5 \text{ V} \leq \text{AV}_{\text{CC}} \leq 5.5 \text{ V}$
Compare time			2.0	]	16500	μS	4.0 V≤ AV <sub>CC</sub> < 4.5 V
Compling time			0.5		8	0	$4.5 \text{ V} \leq \text{AV}_{\text{CC}} \leq 5.5 \text{ V}$
Sampling time			1.2		$\int_{-\infty}^{\infty}$	μS	4.0 V≤ AV <sub>CC</sub> < 4.5 V
Analog port input current	I <sub>AIN</sub>	AN0 to AN23	-0.3	_	+0.3	μА	
Analog input voltage range	V <sub>AIN</sub>	AN0 to AN23	AVRL		AVRH	V	
Reference		AVRH	AVRL + 2.7	Ī	AV <sub>CC</sub>	V	
voltage range		AVRL	0	Ī	AVRH — 2.7	٧	
Power supply	I <sub>A</sub>	$AV_{CC}$		3.5	7.5	mA	
current	I <sub>AH</sub>	$AV_{CC}$		Ī	5	μΑ	*
Reference	I <sub>R</sub>	AVRH		600	900	μΑ	
voltage current	I <sub>RH</sub>	AVRH	_	_	5	μΑ	*
Offset between input channels		AN0 to AN23	_		4	LSB	

<sup>\*:</sup> If the A/D convertor is not operating, a current when CPU is stopped is applicable ( $V_{CC} = AV_{CC} = AVRH = 5.0 \text{ V}$ ). Note: : The accuracy gets worse as |AVRH - AVRL| becomes smaller.

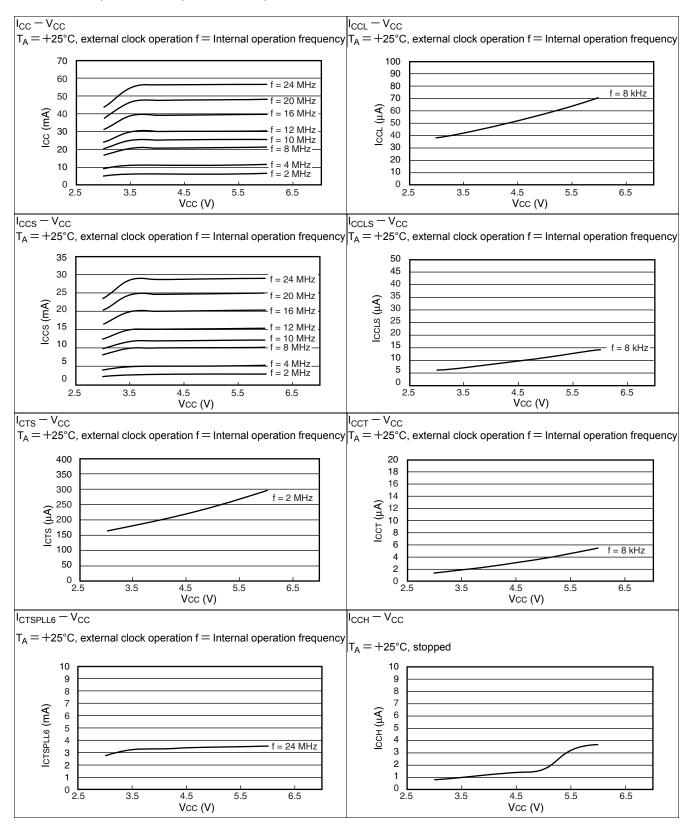


### ■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES





# ■ MB90F349E, MB90F349ES, MB90F349CE, MB90F349CES





# Sales, Solutions, and Legal Information

## **Worldwide Sales and Design Support**

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

### **Products**

ARM® Cortex® Microcontrollers

Automotive

Clocks & Buffers

Interface

Lighting & Power Control

Memory

Cypress.com/automotive

cypress.com/clocks

cypress.com/interface

cypress.com/powerpsoc

cypress.com/powerpsoc

cypress.com/memory

cypress.com/psoc

PSoC cypress.com/psoc
Touch Sensing cypress.com/touch
USB Controllers cypress.com/usb
Wireless/RF cypress.com/wireless

# PSoC® Solutions

cypress.com/psoc PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

## **Cypress Developer Community**

Community | Forums | Blogs | Video | Training

# **Technical Support**

cypress.com/support

© Cypress Semiconductor Corporation, 2006-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.