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#### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

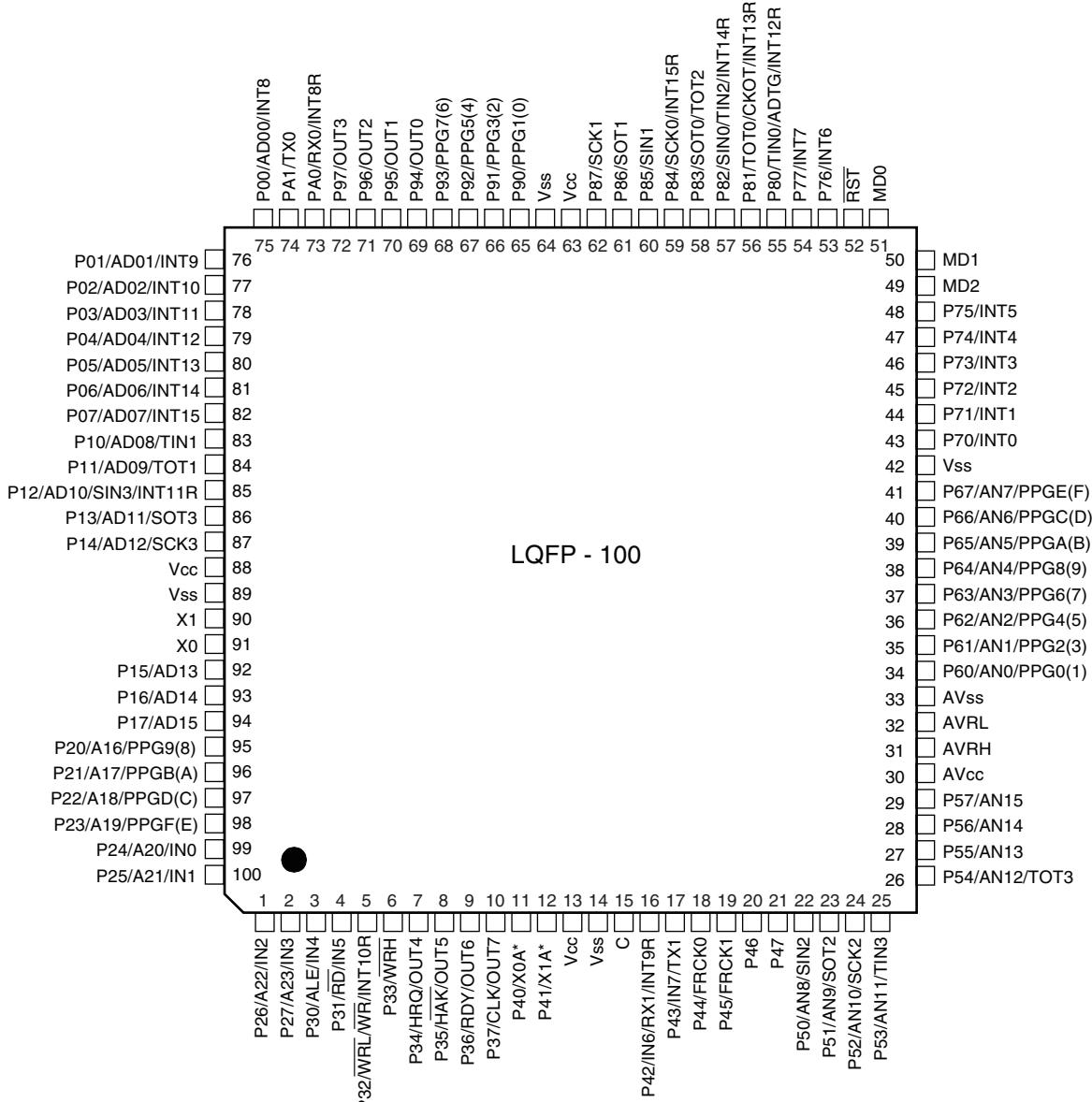
#### Applications of "[Embedded - Microcontrollers](#)"

##### Details

Product Status	Obsolete
Core Processor	F <sup>2</sup> MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-491e1">https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-491e1</a>

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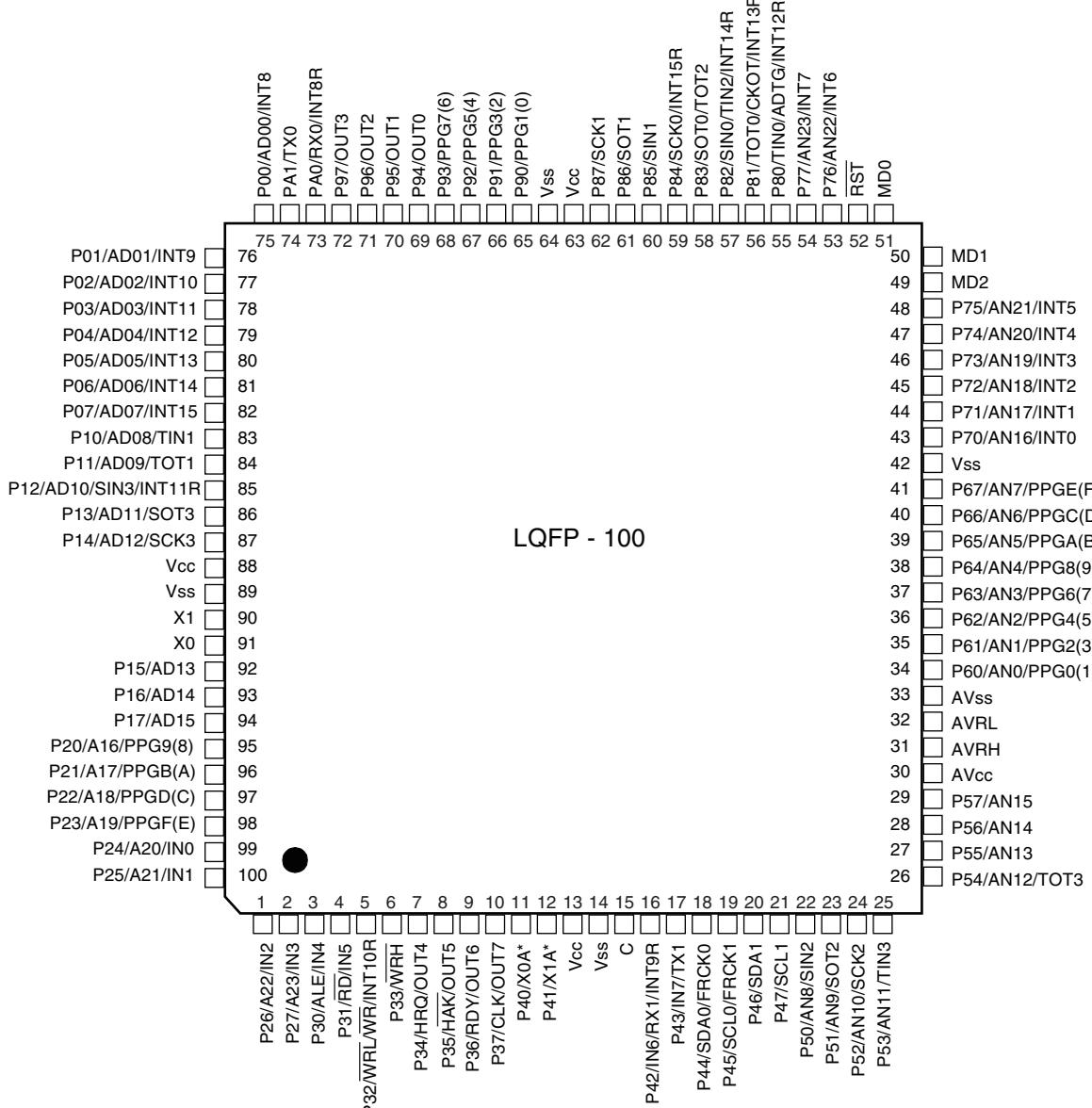
(TOP VIEW)



\* : X0A, X1A : devices without an S suffix in the part number

P40, P4 : devices with an S suffix in the part number

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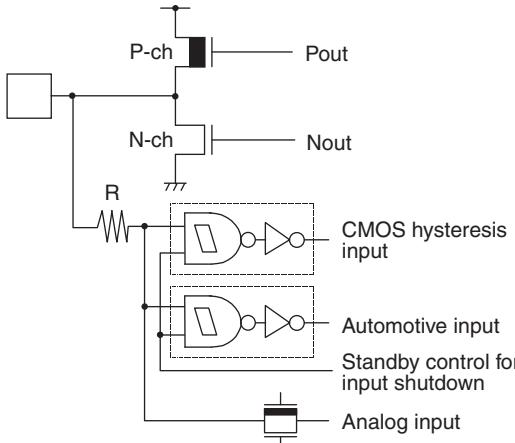
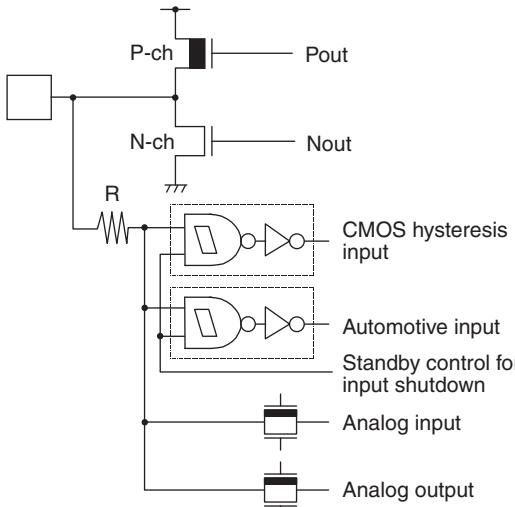
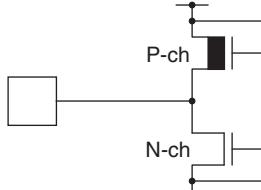
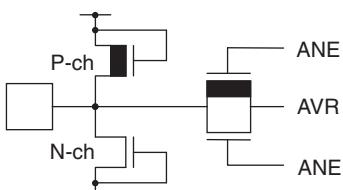
\* : X0A, X1A : devices without an S suffix in the part number  
 P40, P41 : devices with an S suffix in the part number

Pin No.		Pin name	I/O Circuit type <sup>*3</sup>	Function
QFP100 <sup>*1</sup>	LQFP100 <sup>*2</sup>			
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V <sub>CC</sub>	—	Power (3.5 V to 5.5 V) input pin
66	64	V <sub>SS</sub>	—	GND pin
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pins
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pins
		OUT0 to OUT3		Waveform output pins for output compares. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin
76	74	PA1	F	General purpose I/O pin.
		TX0		TX Output pin for CAN0
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer

*(Continued)*

Pin No.		Pin name	I/O Circuit type <sup>*3</sup>	Function
QFP100 <sup>*1</sup>	LQFP100 <sup>*2</sup>			
86	84	P11	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer
87	85	P12	N	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin
88	86	P13	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
89	87	P14	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3
90	88	V <sub>CC</sub>	—	Power (3.5 V to 5.5 V) input pin
91	89	V <sub>SS</sub>	—	GND pin
92	90	X1	A	Main clock output pin
93	91	X0		Main clock input pin
94	92	P15	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
95	93	P16	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.

*(Continued)*

Type	Circuit	Remarks
I	 <p>Pout Nout R CMOS hysteresis input Automotive input Standby control for input shutdown Analog input</p>	<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ A/D converter analog input</li> </ul>
J	 <p>Pout Nout R CMOS hysteresis input Automotive input Standby control for input shutdown Analog input Analog output</p>	<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ D/A analog output</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ A/D converter analog input</li> </ul>
K	 <p>P-ch N-ch</p>	Power supply input protection circuit
L	 <p>P-ch N-ch ANE AVR ANE</p>	<ul style="list-style-type: none"> <li>■ A/D converter reference voltage power supply input pin, with the protection circuit</li> <li>■ Flash memory devices do not have a protection circuit against <math>V_{CC}</math> for pin AVRH</li> </ul>

## 5. Handling Devices

### 1. Preventing latch-up

**CMOS IC may suffer latch-up under the following conditions:**

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  and  $V_{SS}$  pins.
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage ( $AV_{CC}$ ,  $AV_{RH}$ ) exceed the digital power-supply voltage.

### 2. Handling unused pins

Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of  $2\text{ k}\Omega$  or more.

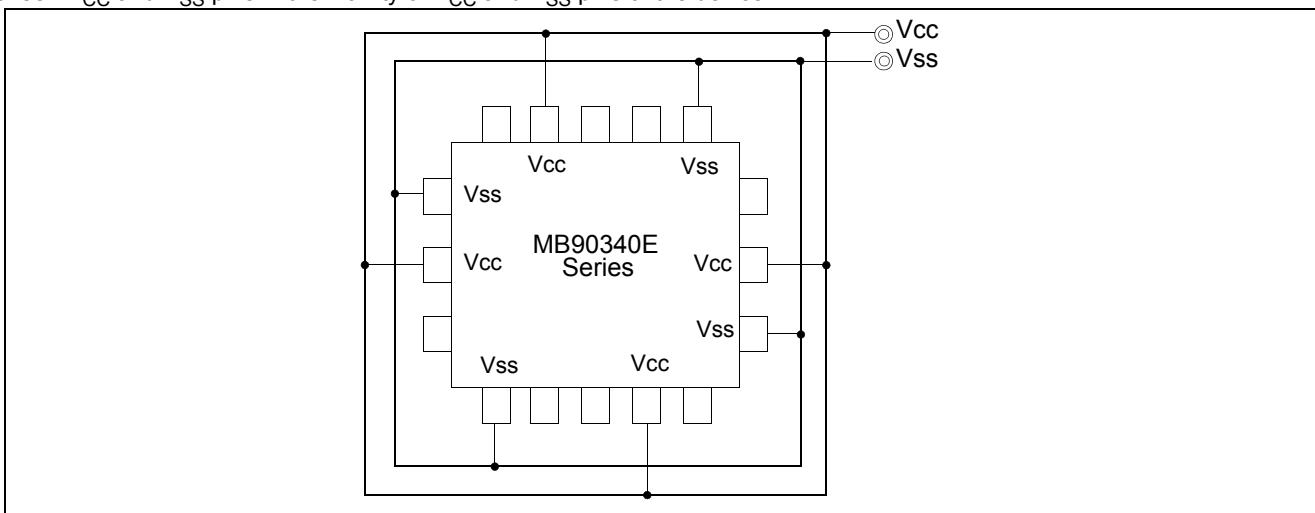
### 3. Power supply pins ( $V_{CC}/V_{SS}$ )

- If there are multiple  $V_{CC}$  and  $V_{SS}$  pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the  $V_{CC}$  and  $V_{SS}$  pins to the power supply and ground externally.

Connect  $V_{CC}$  and  $V_{SS}$  pins to the device from the current supply source at a possibly low impedance.

- As a measure against power supply noise, it is recommended to connect a capacitor of about  $0.1\text{ }\mu\text{F}$  as a bypass capacitor between  $V_{CC}$  and  $V_{SS}$  pins in the vicinity of  $V_{CC}$  and  $V_{SS}$  pins of the device.



### 4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to  $V_{CC}$  or  $V_{SS}$  pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to  $V_{CC}$  or  $V_{SS}$  pins and to provide a low-impedance connection.

Address	Register	Abbreviation	Access	Resource name	Initial value
007924 <sub>H</sub>	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX <sub>B</sub>
007925 <sub>H</sub>	Input Capture 2	IPCP2	R		XXXXXXXX <sub>B</sub>
007926 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXX <sub>B</sub>
007927 <sub>H</sub>	Input Capture 3	IPCP3	R		XXXXXXXX <sub>B</sub>
007928 <sub>H</sub>	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX <sub>B</sub>
007929 <sub>H</sub>	Input Capture 4	IPCP4	R		XXXXXXXX <sub>B</sub>
00792A <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXX <sub>B</sub>
00792B <sub>H</sub>	Input Capture 5	IPCP5	R		XXXXXXXX <sub>B</sub>
00792C <sub>H</sub>	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXX <sub>B</sub>
00792D <sub>H</sub>	Input Capture 6	IPCP6	R		XXXXXXXX <sub>B</sub>
00792E <sub>H</sub>	Input Capture 7	IPCP7	R		XXXXXXXX <sub>B</sub>
00792F <sub>H</sub>	Input Capture 7	IPCP7	R		XXXXXXXX <sub>B</sub>
007930 <sub>H</sub>	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX <sub>B</sub>
007931 <sub>H</sub>	Output Compare 0	OCCP0	R/W		XXXXXXXX <sub>B</sub>
007932 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX <sub>B</sub>
007933 <sub>H</sub>	Output Compare 1	OCCP1	R/W		XXXXXXXX <sub>B</sub>
007934 <sub>H</sub>	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX <sub>B</sub>
007935 <sub>H</sub>	Output Compare 2	OCCP2	R/W		XXXXXXXX <sub>B</sub>
007936 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX <sub>B</sub>
007937 <sub>H</sub>	Output Compare 3	OCCP3	R/W		XXXXXXXX <sub>B</sub>
007938 <sub>H</sub>	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX <sub>B</sub>
007939 <sub>H</sub>	Output Compare 4	OCCP4	R/W		XXXXXXXX <sub>B</sub>
00793A <sub>H</sub>	Output Compare 5	OCCP5	R/W		XXXXXXXX <sub>B</sub>
00793B <sub>H</sub>	Output Compare 5	OCCP5	R/W		XXXXXXXX <sub>B</sub>
00793C <sub>H</sub>	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX <sub>B</sub>
00793D <sub>H</sub>	Output Compare 6	OCCP6	R/W		XXXXXXXX <sub>B</sub>
00793E <sub>H</sub>	Output Compare 7	OCCP7	R/W		XXXXXXXX <sub>B</sub>
00793F <sub>H</sub>	Output Compare 7	OCCP7	R/W		XXXXXXXX <sub>B</sub>
007940 <sub>H</sub>	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000 <sub>B</sub>
007941 <sub>H</sub>	Timer Data 0	TCDT0	R/W		00000000 <sub>B</sub>
007942 <sub>H</sub>	Timer Control Status 0	TCCSL0	R/W		00000000 <sub>B</sub>
007943 <sub>H</sub>	Timer Control Status 0	TCCSH0	R/W		0XXXXXXX <sub>B</sub>
007944 <sub>H</sub>	Timer Data 1	TCDT1	R/W	Free-run Timer 1	00000000 <sub>B</sub>
007945 <sub>H</sub>	Timer Data 1	TCDT1	R/W		00000000 <sub>B</sub>
007946 <sub>H</sub>	Timer Control Status 1	TCCSL1	R/W		00000000 <sub>B</sub>
007947 <sub>H</sub>	Timer Control Status 1	TCCSH1	R/W		0XXXXXXX <sub>B</sub>

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Address	Register	Abbreviation	Access	Resource name	Initial value
007948 <sub>H</sub>	Timer 0/Reload 0	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX <sub>B</sub>
007949 <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>
00794A <sub>H</sub>	Timer 1/Reload 1	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX <sub>B</sub>
00794B <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>
00794C <sub>H</sub>	Timer 2/Reload 2	TMR2/TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX <sub>B</sub>
00794D <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>
00794E <sub>H</sub>	Timer 3/Reload 3	TMR3/TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX <sub>B</sub>
00794F <sub>H</sub>			R/W		XXXXXXXX <sub>B</sub>
007950 <sub>H</sub>	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000 <sub>B</sub>
007951 <sub>H</sub>	Serial Control Register 3	SCR3	W,R/W		00000000 <sub>B</sub>
007952 <sub>H</sub>	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000 <sub>B</sub>
007953 <sub>H</sub>	Serial Status Register 3	SSR3	R,R/W		00001000 <sub>B</sub>
007954 <sub>H</sub>	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XX <sub>B</sub>
007955 <sub>H</sub>	Extended Status Control Register	ESCR3	R/W		00000100 <sub>B</sub>
007956 <sub>H</sub>	Baud Rate Generator Register 30	BGR30	R/W		00000000 <sub>B</sub>
007957 <sub>H</sub>	Baud Rate Generator Register 31	BGR31	R/W		00000000 <sub>B</sub>
007958 <sub>H</sub>	Serial Mode Register 4	SMR4	W,R/W	UART4	00000000 <sub>B</sub>
007959 <sub>H</sub>	Serial Control Register 4	SCR4	W,R/W		00000000 <sub>B</sub>
00795A <sub>H</sub>	Reception/Transmission Data Register 4	RDR4/TDR4	R/W		00000000 <sub>B</sub>
00795B <sub>H</sub>	Serial Status Register 4	SSR4	R,R/W		00001000 <sub>B</sub>
00795C <sub>H</sub>	Extended Communication Control Register 4	ECCR4	R,W, R/W		000000XX <sub>B</sub>
00795D <sub>H</sub>	Extended Status Control Register	ESCR4	R/W		00000100 <sub>B</sub>
00795E <sub>H</sub>	Baud Rate Generator Register 40	BGR40	R/W		00000000 <sub>B</sub>
00795F <sub>H</sub>	Baud Rate Generator Register 41	BGR41	R/W		00000000 <sub>B</sub>
007960 <sub>H</sub> to 00796B <sub>H</sub>	Reserved				
00796C <sub>H</sub>	Clock Output Enable Register	CLKR	R/W	Clock Monitor	XXXX0000 <sub>B</sub>
00796D <sub>H</sub>	Reserved				
00796E <sub>H</sub>	CAN Direct Mode Register	CDMR	R/W	CAN Clock sync	XXXXXXXX0 <sub>B</sub>
00796F <sub>H</sub>	CAN Switch Register	CANSWR	R/W	CAN 0/1	XXXXXXXX00 <sub>B</sub>

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Address	Register	Abbreviation	Access	Resource name	Initial value
0079E0 <sub>H</sub>	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXX <sub>B</sub>
0079E1 <sub>H</sub>	Detect Address Setting 0	PADR0	R/W		XXXXXXXX <sub>B</sub>
0079E2 <sub>H</sub>	Detect Address Setting 0	PADR0	R/W		XXXXXXXX <sub>B</sub>
0079E3 <sub>H</sub>	Detect Address Setting 1	PADR1	R/W		XXXXXXXX <sub>B</sub>
0079E4 <sub>H</sub>	Detect Address Setting 1	PADR1	R/W		XXXXXXXX <sub>B</sub>
0079E5 <sub>H</sub>	Detect Address Setting 1	PADR1	R/W		XXXXXXXX <sub>B</sub>
0079E6 <sub>H</sub>	Detect Address Setting 2	PADR2	R/W		XXXXXXXX <sub>B</sub>
0079E7 <sub>H</sub>	Detect Address Setting 2	PADR2	R/W		XXXXXXXX <sub>B</sub>
0079E8 <sub>H</sub>	Detect Address Setting 2	PADR2	R/W		XXXXXXXX <sub>B</sub>
0079E9 <sub>H</sub> to 0079EF <sub>H</sub>	Reserved				
0079F0 <sub>H</sub>	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXX <sub>B</sub>
0079F1 <sub>H</sub>	Detect Address Setting 3	PADR3	R/W		XXXXXXXX <sub>B</sub>
0079F2 <sub>H</sub>	Detect Address Setting 3	PADR3	R/W		XXXXXXXX <sub>B</sub>
0079F3 <sub>H</sub>	Detect Address Setting 4	PADR4	R/W		XXXXXXXX <sub>B</sub>
0079F4 <sub>H</sub>	Detect Address Setting 4	PADR4	R/W		XXXXXXXX <sub>B</sub>
0079F5 <sub>H</sub>	Detect Address Setting 4	PADR4	R/W		XXXXXXXX <sub>B</sub>
0079F6 <sub>H</sub>	Detect Address Setting 5	PADR5	R/W		XXXXXXXX <sub>B</sub>
0079F7 <sub>H</sub>	Detect Address Setting 5	PADR5	R/W		XXXXXXXX <sub>B</sub>
0079F8 <sub>H</sub>	Detect Address Setting 5	PADR5	R/W		XXXXXXXX <sub>B</sub>
0079F9 <sub>H</sub> to 0079FF <sub>H</sub>	Reserved				
007A00 <sub>H</sub> to 007AFF <sub>H</sub>	Reserved for CAN Controller 0. Refer to " <a href="#">CAN Controllers</a> "				
007B00 <sub>H</sub> to 007BFF <sub>H</sub>	Reserved for CAN Controller 0. Refer to " <a href="#">CAN Controllers</a> "				
007C00 <sub>H</sub> to 007CFF <sub>H</sub>	Reserved for CAN Controller 1. Refer to " <a href="#">CAN Controllers</a> "				
007D00 <sub>H</sub> to 007DFF <sub>H</sub>	Reserved for CAN Controller 1. Refer to " <a href="#">CAN Controllers</a> "				
007E00 <sub>H</sub> to 007FFF <sub>H</sub>	Reserved				

- Note:**
- Initial value of "X" represents unknown value.
  - Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading "X".

## 9. CAN Controllers

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
- Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
- 29-bit ID and 8-byte data
- Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
- Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

**List of Control Registers (1)**

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070 <sub>H</sub>	000080 <sub>H</sub>	Message Buffer Valid Register	BVALR	R/W	00000000 <sub>B</sub>
000071 <sub>H</sub>	000081 <sub>H</sub>				00000000 <sub>B</sub>
000072 <sub>H</sub>	000082 <sub>H</sub>	Transmit Request Register	TREQR	R/W	00000000 <sub>B</sub>
000073 <sub>H</sub>	000083 <sub>H</sub>				00000000 <sub>B</sub>
000074 <sub>H</sub>	000084 <sub>H</sub>	Transmit Cancel Register	TCANR	W	00000000 <sub>B</sub>
000075 <sub>H</sub>	000085 <sub>H</sub>				00000000 <sub>B</sub>
000076 <sub>H</sub>	000086 <sub>H</sub>	Transmission Complete Register	TCR	R/W	00000000 <sub>B</sub>
000077 <sub>H</sub>	000087 <sub>H</sub>				00000000 <sub>B</sub>
000078 <sub>H</sub>	000088 <sub>H</sub>	Receive Complete Register	RCR	R/W	00000000 <sub>B</sub>
000079 <sub>H</sub>	000089 <sub>H</sub>				00000000 <sub>B</sub>
00007A <sub>H</sub>	00008A <sub>H</sub>	Remote Request Receiving Register	RRTRR	R/W	00000000 <sub>B</sub>
00007B <sub>H</sub>	00008B <sub>H</sub>				00000000 <sub>B</sub>
00007C <sub>H</sub>	00008C <sub>H</sub>	Receive Overrun Register	ROVRR	R/W	00000000 <sub>B</sub>
00007D <sub>H</sub>	00008D <sub>H</sub>				00000000 <sub>B</sub>
00007E <sub>H</sub>	00008E <sub>H</sub>	Reception Interrupt Enable Register	RIER	R/W	00000000 <sub>B</sub>
00007F <sub>H</sub>	00008F <sub>H</sub>				00000000 <sub>B</sub>

**List of Message Buffers (ID Registers) (1)**

<b>Address</b>		<b>Register</b>	<b>Abbreviation</b>	<b>Access</b>	<b>Initial Value</b>
<b>CAN0</b>	<b>CAN1</b>				
007A00 <sub>H</sub> to 007A1F <sub>H</sub>	007C00 <sub>H</sub> to 007C1F <sub>H</sub>	General-Purpose RAM	—	R/W	XXXXXXXXX <sub>B</sub> to XXXXXXXXX <sub>B</sub>
007A20 <sub>H</sub>	007C20 <sub>H</sub>	ID Register 0	IDR0	R/W	XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A21 <sub>H</sub>	007C21 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A22 <sub>H</sub>	007C22 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A23 <sub>H</sub>	007C23 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A24 <sub>H</sub>	007C24 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A25 <sub>H</sub>	007C25 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A26 <sub>H</sub>	007C26 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A27 <sub>H</sub>	007C27 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A28 <sub>H</sub>	007C28 <sub>H</sub>	ID Register 2	IDR2	R/W	XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A29 <sub>H</sub>	007C29 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A2A <sub>H</sub>	007C2A <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A2B <sub>H</sub>	007C2B <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A2C <sub>H</sub>	007C2C <sub>H</sub>	ID Register 3	IDR3	R/W	XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A2D <sub>H</sub>	007C2D <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A2E <sub>H</sub>	007C2E <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A2F <sub>H</sub>	007C2F <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A30 <sub>H</sub>	007C30 <sub>H</sub>	ID Register 4	IDR4	R/W	XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A31 <sub>H</sub>	007C31 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A32 <sub>H</sub>	007C32 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A33 <sub>H</sub>	007C33 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A34 <sub>H</sub>	007C34 <sub>H</sub>	ID Register 5	IDR5	R/W	XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A35 <sub>H</sub>	007C35 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A36 <sub>H</sub>	007C36 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A37 <sub>H</sub>	007C37 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A38 <sub>H</sub>	007C38 <sub>H</sub>	ID Register 6	IDR6	R/W	XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A39 <sub>H</sub>	007C39 <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A3A <sub>H</sub>	007C3A <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A3B <sub>H</sub>	007C3B <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A3C <sub>H</sub>	007C3C <sub>H</sub>	ID Register 7	IDR7	R/W	XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A3D <sub>H</sub>	007C3D <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A3E <sub>H</sub>	007C3E <sub>H</sub>				XXXXXXXXX <sub>B</sub> XXXXXXXXX <sub>B</sub>
007A3F <sub>H</sub>	007C3F <sub>H</sub>				

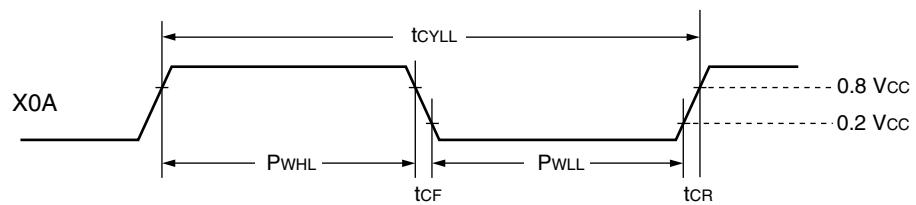
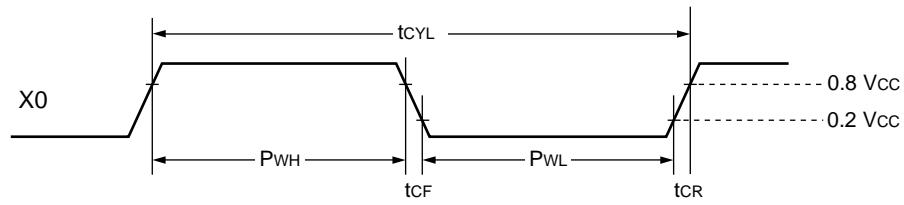
### 11.3 DC Characteristics

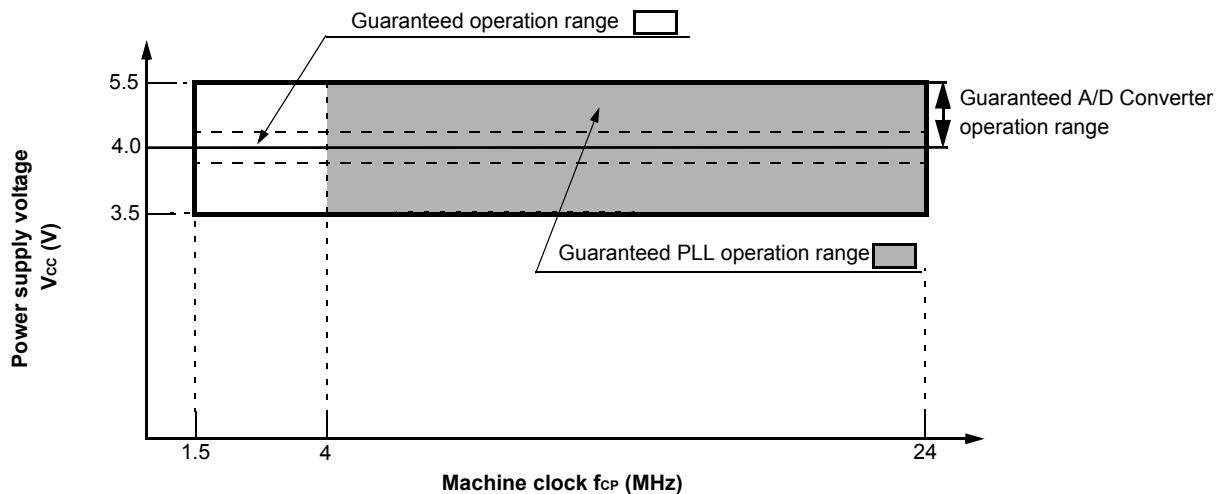
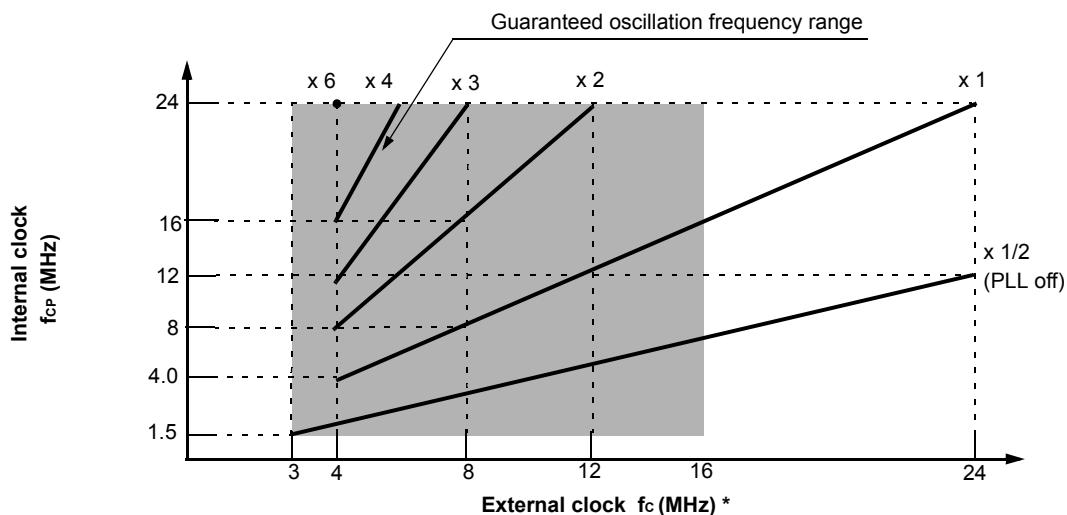
( $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $f_{CP} \leq 24 \text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5 \text{ V} \pm 10\%$ )	$V_{IHS}$	—	—	0.8 $V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	$V_{IHA}$	—	—	0.8 $V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if Automotive input levels are selected
	$V_{IHT}$	—	—	2.0	—	$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected
	$V_{IHS}$	—	—	0.7 $V_{CC}$	—	$V_{CC} + 0.3$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	$V_{IHI}$	—	—	0.7 $V_{CC}$	—	$V_{CC} + 0.3$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	$V_{IHR}$	—	—	0.8 $V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{RST}$ input pin (CMOS hysteresis)
	$V_{IHM}$	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5 \text{ V} \pm 10\%$ )	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	0.2 $V_{CC}$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	$V_{ILA}$	—	—	$V_{SS} - 0.3$	—	0.5 $V_{CC}$	V	Port inputs if Automotive input levels are selected
	$V_{ILT}$	—	—	$V_{SS} - 0.3$	—	0.8	V	Port inputs if TTL input levels are selected
	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	0.3 $V_{CC}$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	$V_{ILI}$	—	—	$V_{SS} - 0.3$	—	0.3 $V_{CC}$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	$V_{ILR}$	—	—	$V_{SS} - 0.3$	—	0.2 $V_{CC}$	V	$\overline{RST}$ input pin (CMOS hysteresis)
	$V_{ILM}$	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	$V_{OH}$	Normal outputs	$V_{CC} = 4.5 \text{ V}$ , $I_{OH} = -4.0 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	$V_{OHI}$	$I^2\text{C}$ current outputs	$V_{CC} = 4.5 \text{ V}$ , $I_{OH} = -3.0 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	$V_{OL}$	Normal outputs	$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 4.0 \text{ mA}$	—	—	0.4	V	
Output L voltage	$V_{OLI}$	$I^2\text{C}$ current outputs	$V_{CC} = 4.5 \text{ V}$ , $I_{OL} = 3.0 \text{ mA}$	—	—	0.4	V	

(Continued)

Clock Timing



**Guaranteed PLL operation range**

**Guaranteed operation range of MB90340E series**


\* : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

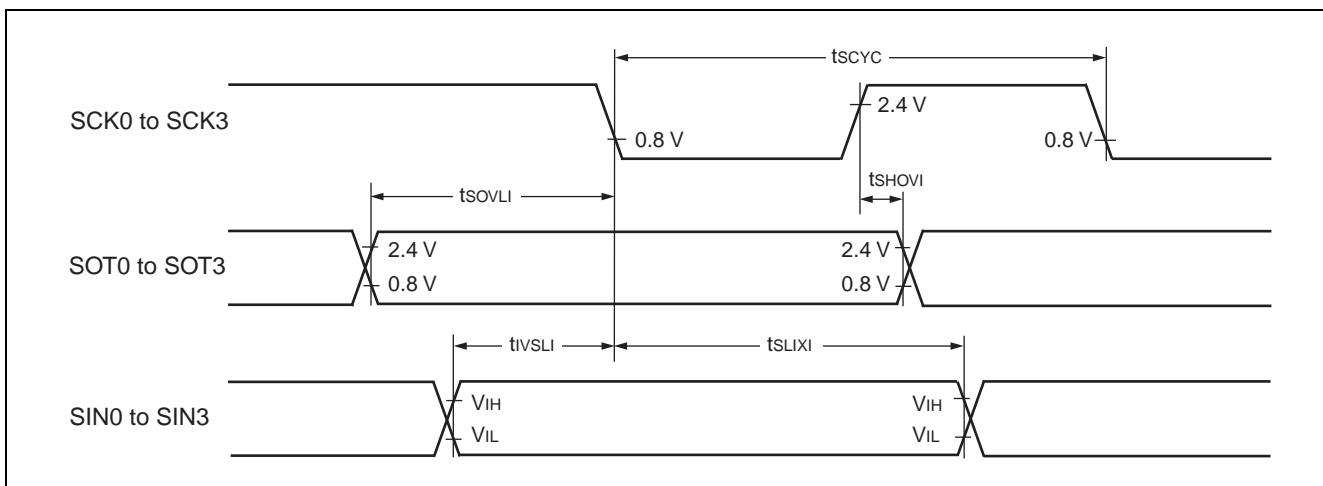
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $f_{CP} \leq 24 \text{ MHz}$ ,  $V_{SS} = 0 \text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK0 to SCK3	Internal clock operation output pins are $C_L = 80 \text{ pF} + 1 \text{ TTL}$ .	5 $t_{CP}$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	$t_{SHOVI}$	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLI}$	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	$t_{SLIXI}$	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	$t_{SOVLI}$	SCK0 to SCK3, SOT0 to SOT3		3 $t_{CP} - 70$	—	ns

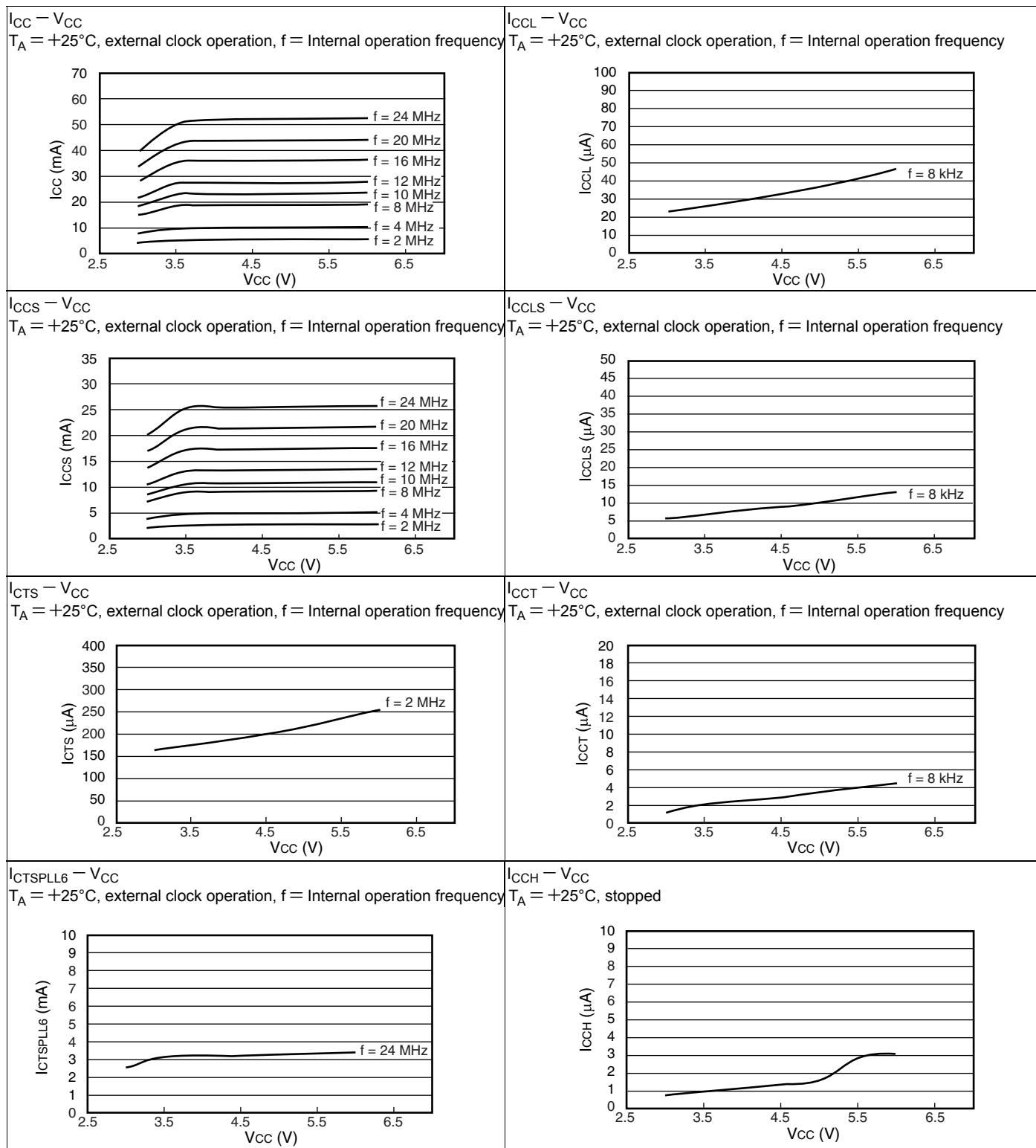
**Note:**

- $C_L$  is load capacity value of pins when testing.
- $t_{CP}$  is internal operating clock cycle time (machine clock) . Refer to “[Clock Timing](#)”.

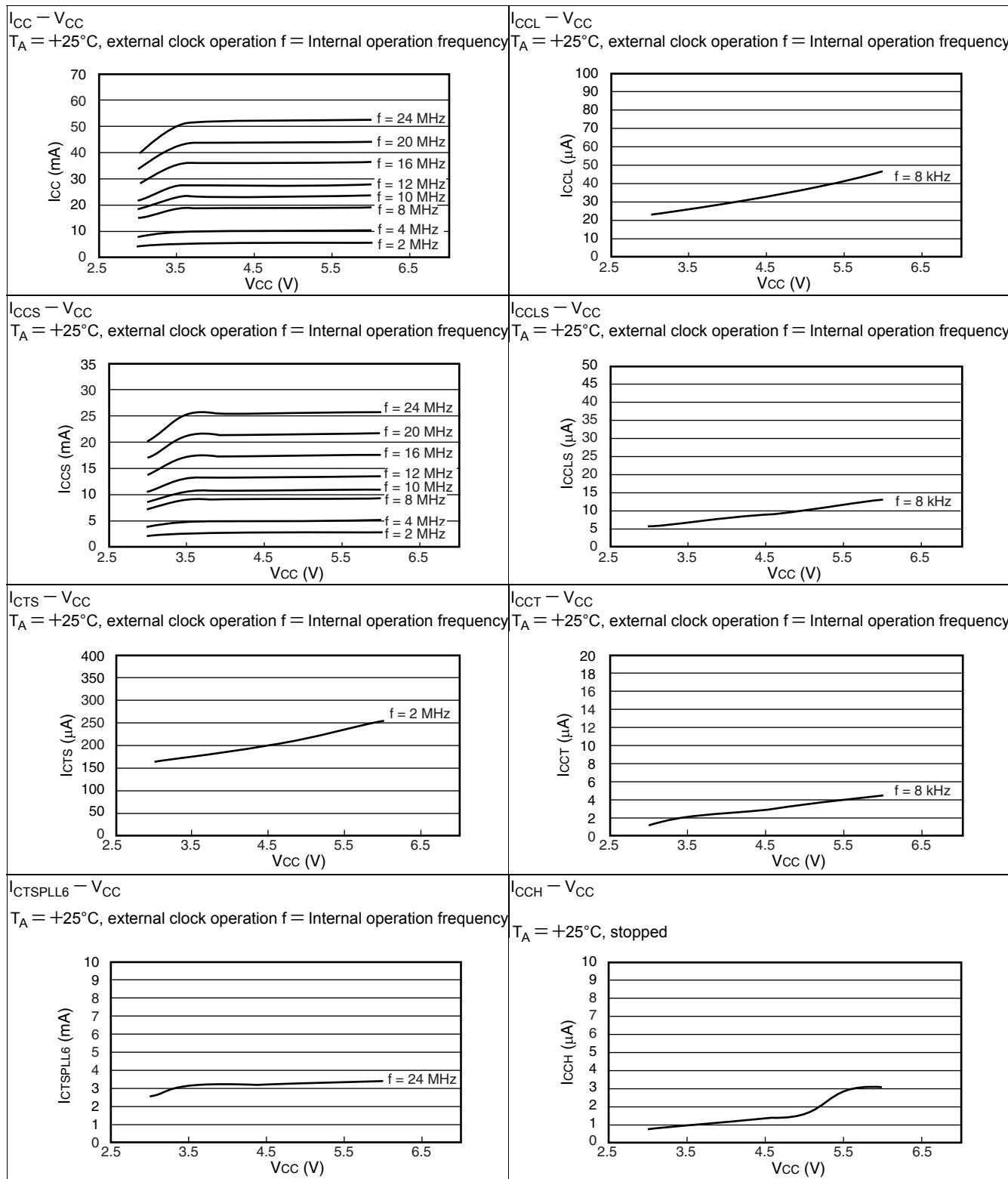


## 12. Example Characteristics

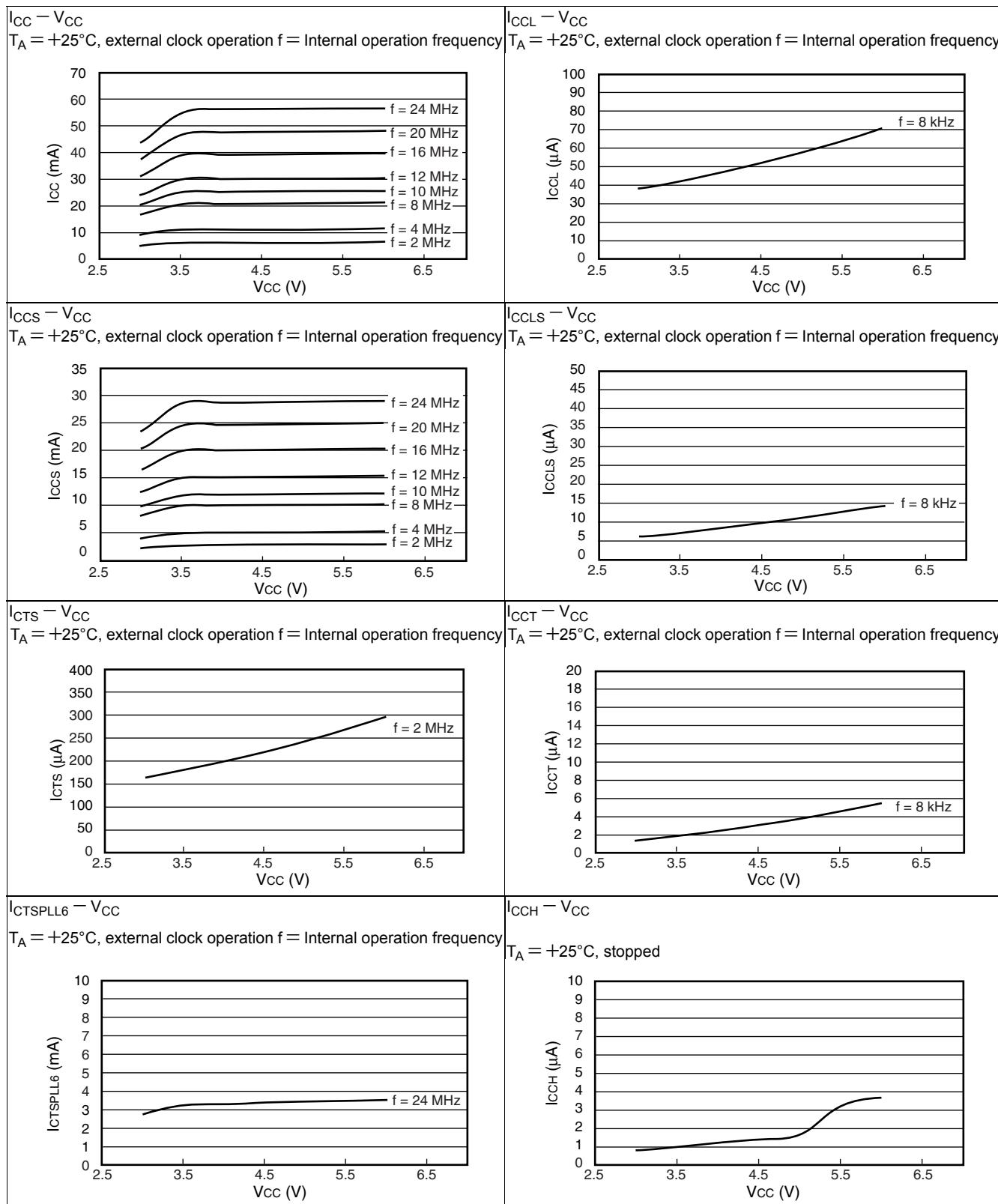
- MB90F346E, MB90F346ES, MB90F346CE, MB90F346CES



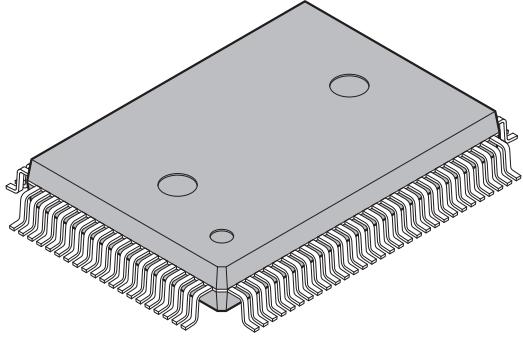
■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES

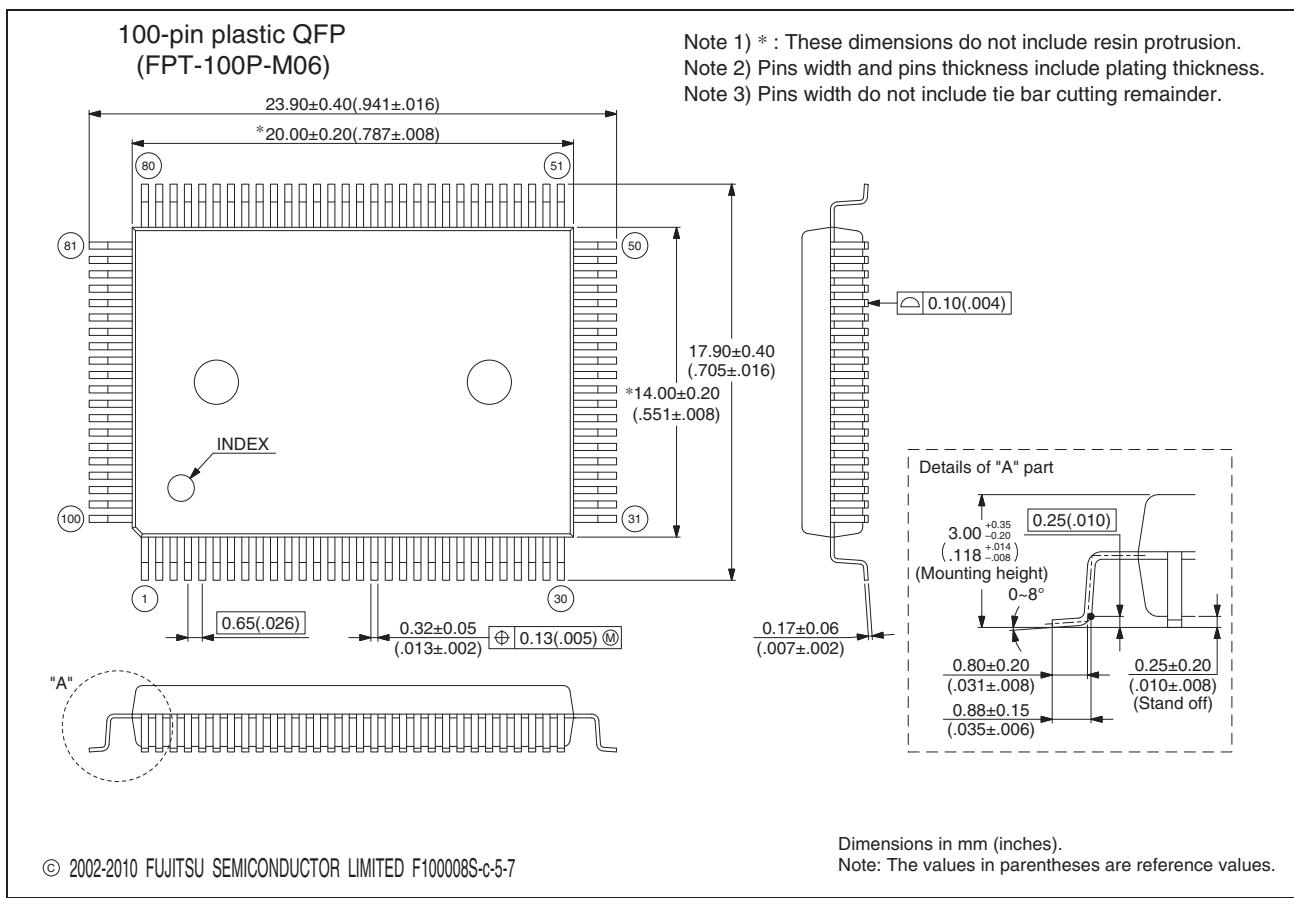


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES



(Continued)

100-pin plastic QFP  (FPT-100P-M06)	<table border="1"> <tbody> <tr> <td>Lead pitch</td><td>0.65 mm</td></tr> <tr> <td>Package width × package length</td><td>14.00 × 20.00 mm</td></tr> <tr> <td>Lead shape</td><td>Gullwing</td></tr> <tr> <td>Sealing method</td><td>Plastic mold</td></tr> <tr> <td>Mounting height</td><td>3.35 mm MAX</td></tr> <tr> <td>Code (Reference)</td><td>P-QFP100-14×20-0.65</td></tr> <tr> <td></td><td></td></tr> </tbody> </table>	Lead pitch	0.65 mm	Package width × package length	14.00 × 20.00 mm	Lead shape	Gullwing	Sealing method	Plastic mold	Mounting height	3.35 mm MAX	Code (Reference)	P-QFP100-14×20-0.65		
Lead pitch	0.65 mm														
Package width × package length	14.00 × 20.00 mm														
Lead shape	Gullwing														
Sealing method	Plastic mold														
Mounting height	3.35 mm MAX														
Code (Reference)	P-QFP100-14×20-0.65														



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