Infineon Technologies - MB90347ESPMC-GS-589E1 Datasheet

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What is "Embedded - Microcontrollers"?

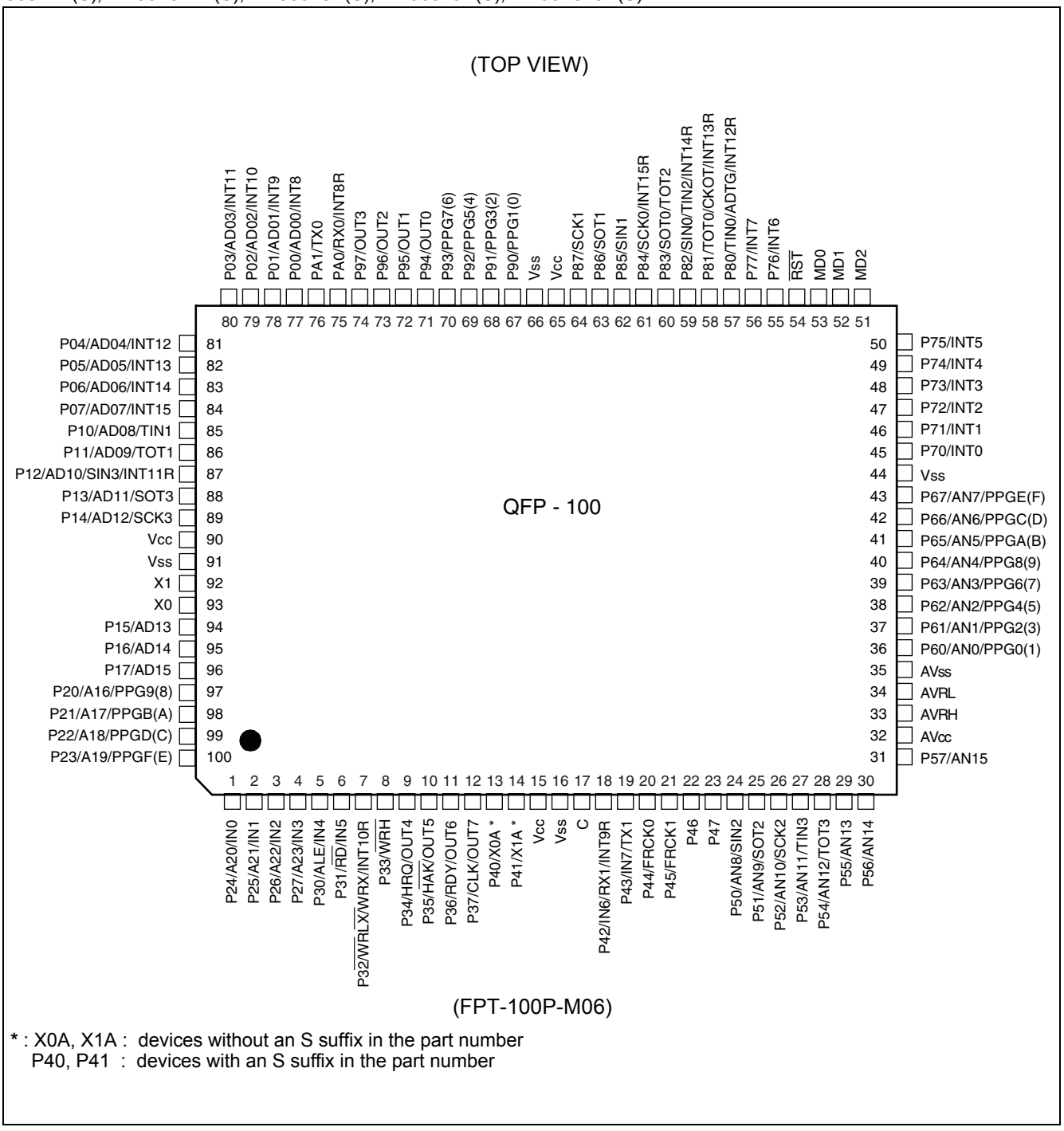
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-589e1

2. Pin Assignments

■ MB90341E(S), MB90342E(S), MB90F342E(S), MB90F345E(S), MB90346E(S), MB90F346E(S), MB90347E(S), MB90F347E(S), MB90348E(S), MB90349E(S), MB90F349E(S)



(FPT-100P-M06)

***** : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

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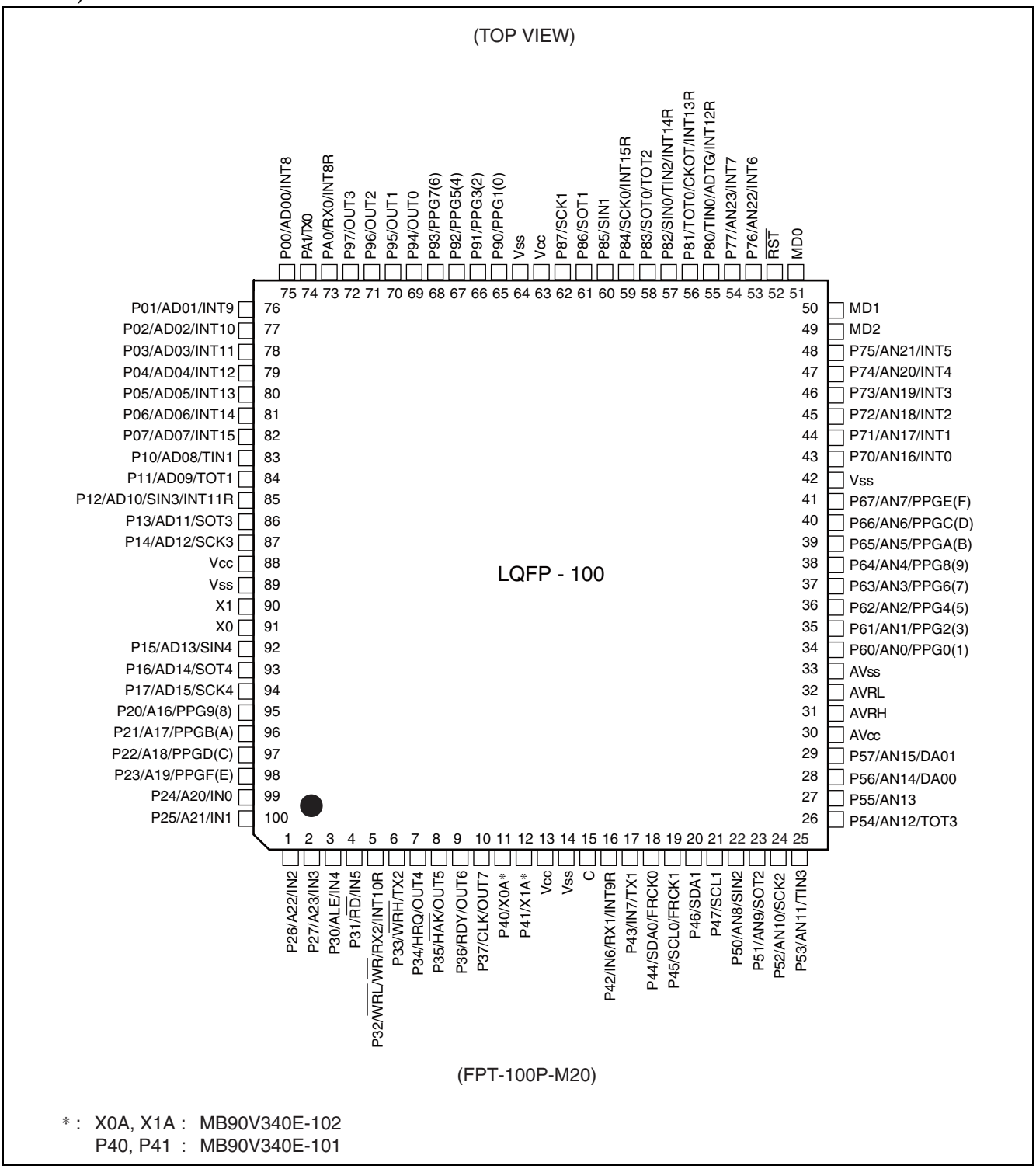

This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

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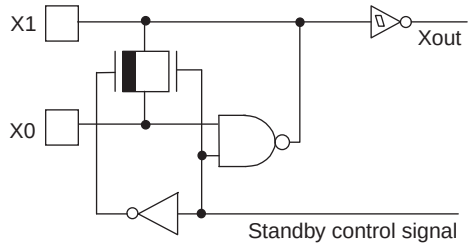
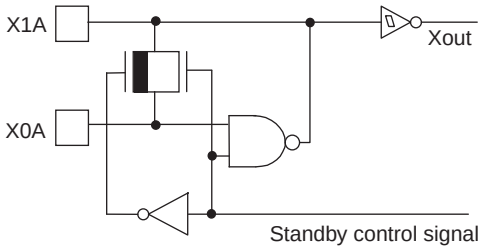
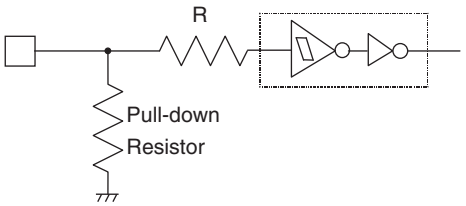
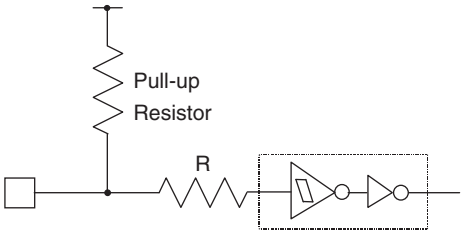
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
96	94	P17	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
97 to 100	95 to 98	P20 to P23	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9,PPGB,PPGD,PPGF		Output pins for PPGs

1 : FPT-100P-M06

2 : FPT-100P-M20

3 : For I/O circuit type, refer to “I/O Circuit Type”.

4. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		■ MASK ROM and evaluation products: CMOS hysteresis input pin ■ Flash memory products: CMOS input pin
D		MASK ROM and evaluation products: ■ CMOS hysteresis input pin ■ Pull-down resistor value: approx. 50 kΩ Flash memory products: ■ CMOS input pin ■ No pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ

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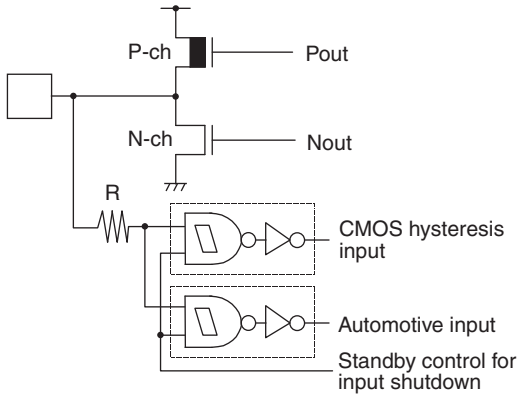
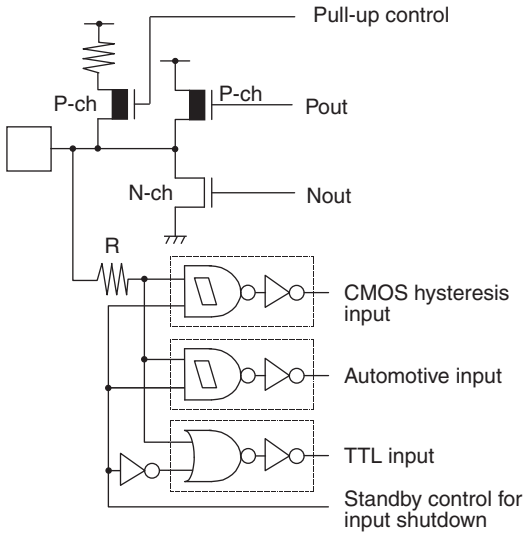
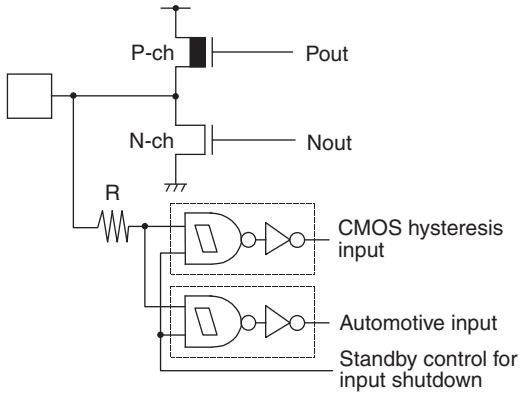
Type	Circuit	Remarks
F		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
G		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) ■ Programmable pull-up resistor: 50 kΩ approx.
H		■ CMOS level output (I_{OL} = 3 mA, I_{OH} = –3 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)

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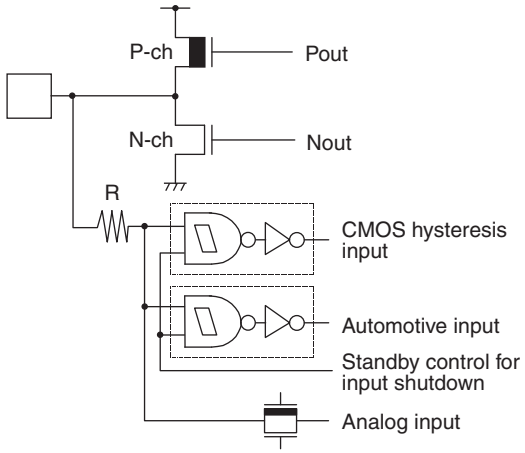
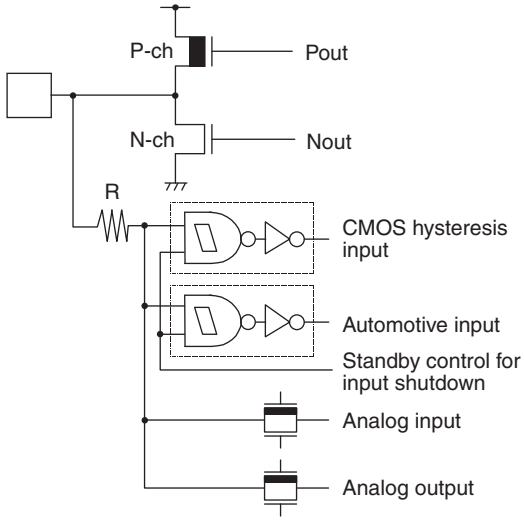
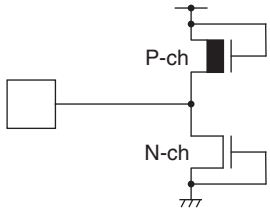
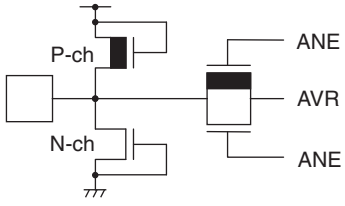
Type	Circuit	Remarks
I		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
J		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ D/A analog output ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
K		Power supply input protection circuit
L		■ A/D converter reference voltage power supply input pin, with the protection circuit ■ Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH

5. Handling Devices

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Handling unused pins

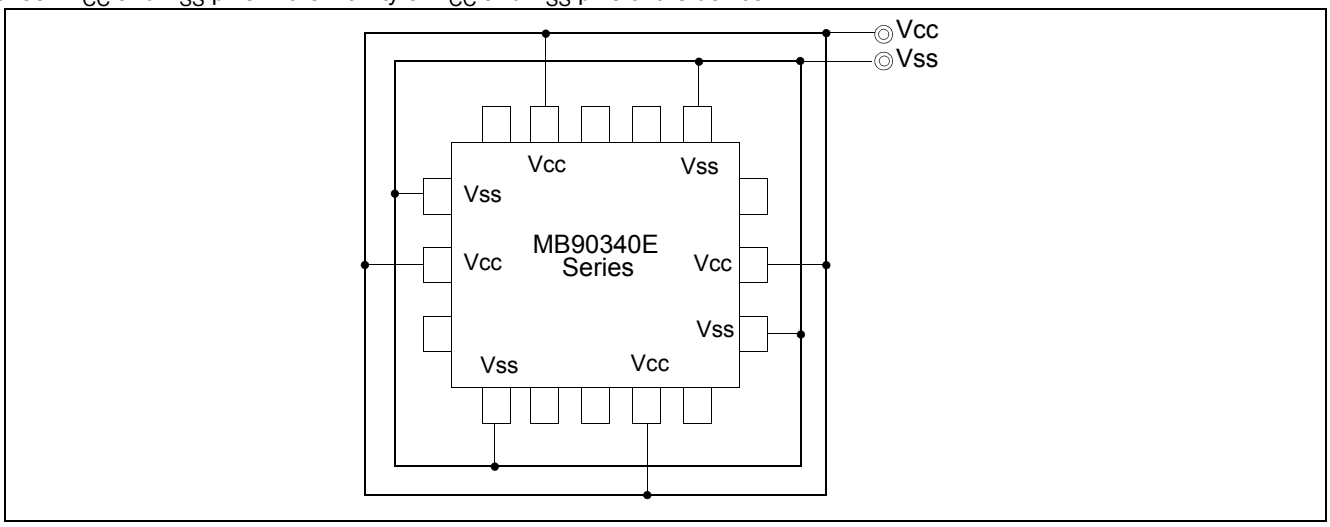
Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 kΩ or more.

3. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
Connect V_{CC} and V_{SS} pins to the device from the current supply source at a possibly low impedance.

- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



4. Mode Pins (MD0 to MD2)

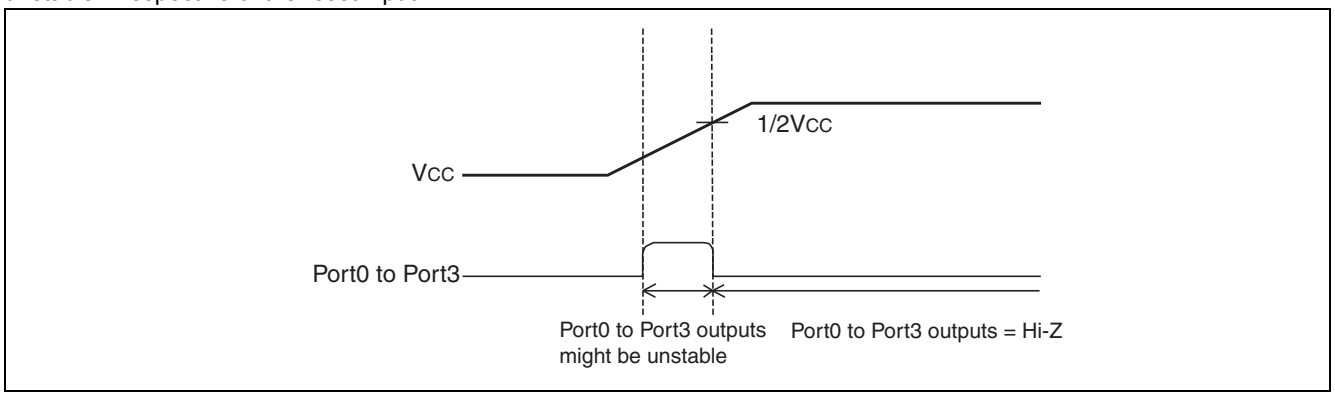
Connect the mode pins directly to V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

13.Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/60 MHz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

14.Port 0 to Port 3 Output During Power-on (External-bus Mode)

As shown below, when the power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable irrespective of the reset input.



15.Notes on Using the CAN Function

To use the CAN function, please set the DIRECT bit of the CAN Direct Mode Register (CDMR) to 1.

16.Flash Security Function (except for MB90F346E)

A security bit is located in the area of the flash memory.
If protection code 01_H is written in the security bit, the flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Refer to following table for the address of the security bit.

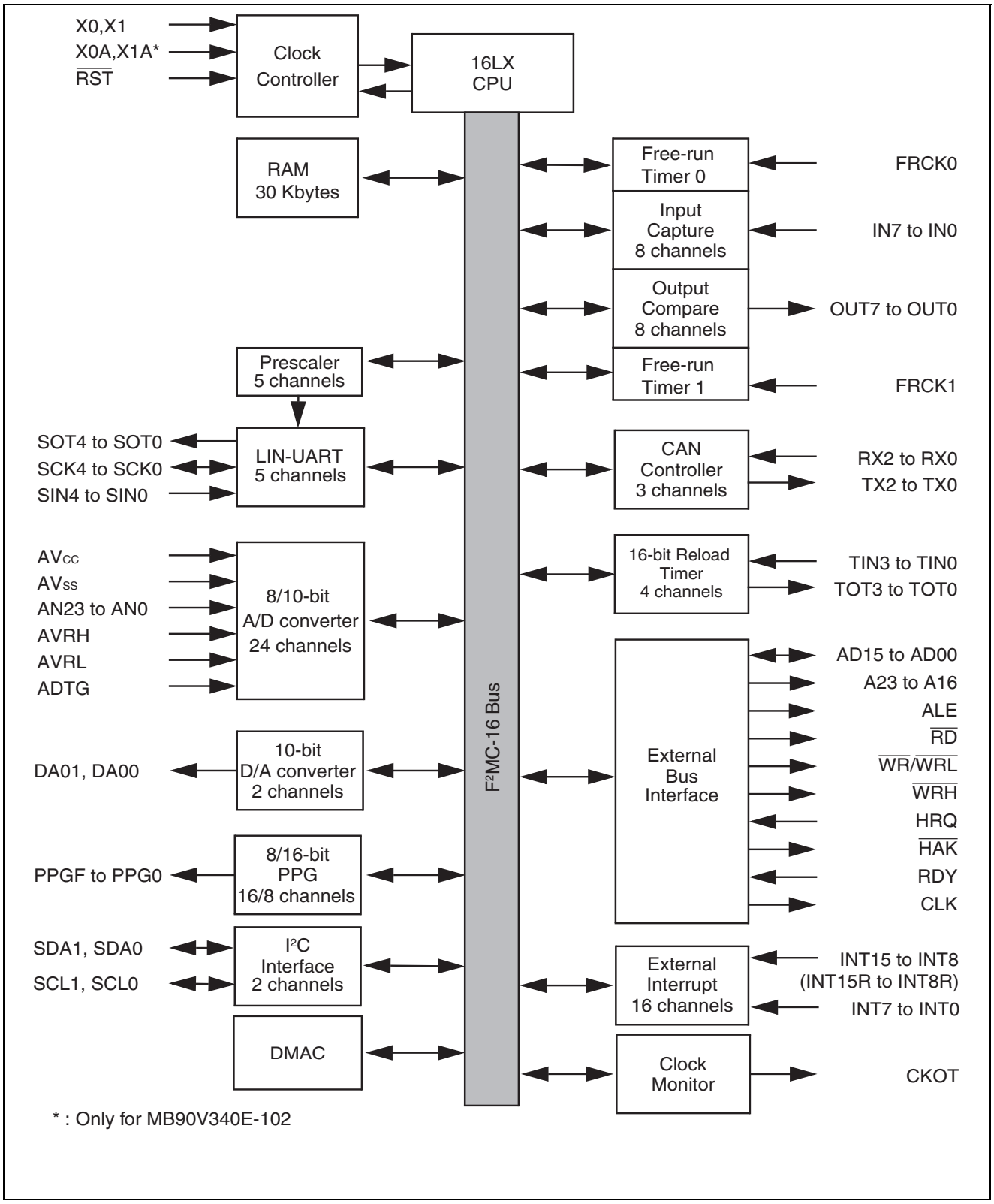
	Flash memory size	Address of the security bit
MB90F347E	Embedded 1 Mbit Flash Memory	$FE0001_H$
MB90F342E MB90F349E	Embedded 2 Mbits Flash Memory	$FC0001_H$
MB90F345E	Embedded 4 Mbits Flash Memory	$F80001_H$

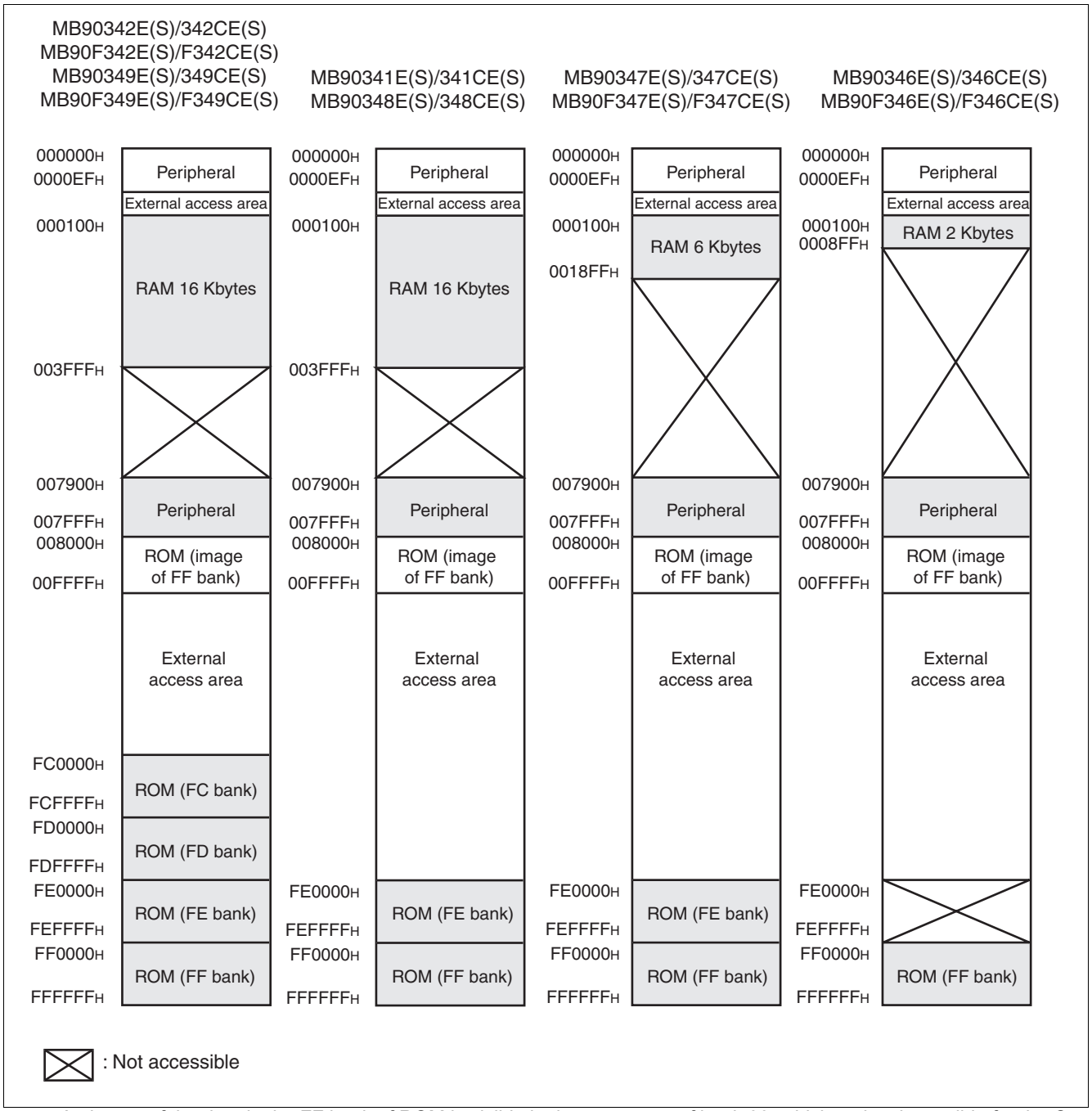
17.Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

6. Block Diagrams

- MB90V340E-101/102





Note: :An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.
For example, when the address $00C000_H$ is accessed, the data at $FFC000_H$ in ROM is actually accessed.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
As a result, the image between $FF8000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF7FFF_H$ is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
007924_H	Input Capture 2	IPCP2	R	Input Capture 2/3	$XXXXXXXX_B$
007925_H	Input Capture 2	IPCP2	R		$XXXXXXXX_B$
007926_H	Input Capture 3	IPCP3	R		$XXXXXXXX_B$
007927_H	Input Capture 3	IPCP3	R		$XXXXXXXX_B$
007928_H	Input Capture 4	IPCP4	R	Input Capture 4/5	$XXXXXXXX_B$
007929_H	Input Capture 4	IPCP4	R		$XXXXXXXX_B$
$00792A_H$	Input Capture 5	IPCP5	R		$XXXXXXXX_B$
$00792B_H$	Input Capture 5	IPCP5	R		$XXXXXXXX_B$
$00792C_H$	Input Capture 6	IPCP6	R	Input Capture 6/7	$XXXXXXXX_B$
$00792D_H$	Input Capture 6	IPCP6	R		$XXXXXXXX_B$
$00792E_H$	Input Capture 7	IPCP7	R		$XXXXXXXX_B$
$00792F_H$	Input Capture 7	IPCP7	R		$XXXXXXXX_B$
007930_H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	$XXXXXXXX_B$
007931_H	Output Compare 0	OCCP0	R/W		$XXXXXXXX_B$
007932_H	Output Compare 1	OCCP1	R/W		$XXXXXXXX_B$
007933_H	Output Compare 1	OCCP1	R/W		$XXXXXXXX_B$
007934_H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	$XXXXXXXX_B$
007935_H	Output Compare 2	OCCP2	R/W		$XXXXXXXX_B$
007936_H	Output Compare 3	OCCP3	R/W		$XXXXXXXX_B$
007937_H	Output Compare 3	OCCP3	R/W		$XXXXXXXX_B$
007938_H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	$XXXXXXXX_B$
007939_H	Output Compare 4	OCCP4	R/W		$XXXXXXXX_B$
$00793A_H$	Output Compare 5	OCCP5	R/W		$XXXXXXXX_B$
$00793B_H$	Output Compare 5	OCCP5	R/W		$XXXXXXXX_B$
$00793C_H$	Output Compare 6	OCCP6	R/W	Output Compare 6/7	$XXXXXXXX_B$
$00793D_H$	Output Compare 6	OCCP6	R/W		$XXXXXXXX_B$
$00793E_H$	Output Compare 7	OCCP7	R/W		$XXXXXXXX_B$
$00793F_H$	Output Compare 7	OCCP7	R/W		$XXXXXXXX_B$
007940_H	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000_B
007941_H	Timer Data 0	TCDT0	R/W		00000000_B
007942_H	Timer Control Status 0	TCCSL0	R/W		00000000_B
007943_H	Timer Control Status 0	TCCSH0	R/W		$0XXXXXXX_B$
007944_H	Timer Data 1	TCDT1	R/W	Free-run Timer 1	00000000_B
007945_H	Timer Data 1	TCDT1	R/W		00000000_B
007946_H	Timer Control Status 1	TCCSL1	R/W		00000000_B
007947_H	Timer Control Status 1	TCCSH1	R/W		$0XXXXXXX_B$

(Continued)

List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A40_H$	$007C40_H$	ID Register 8	IDR8	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A41_H$	$007C41_H$				
$007A42_H$	$007C42_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A43_H$	$007C43_H$				
$007A44_H$	$007C44_H$	ID Register 9	IDR9	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A45_H$	$007C45_H$				
$007A46_H$	$007C46_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A47_H$	$007C47_H$				
$007A48_H$	$007C48_H$	ID Register 10	IDR10	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A49_H$	$007C49_H$				
$007A4A_H$	$007C4A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4B_H$	$007C4B_H$				
$007A4C_H$	$007C4C_H$	ID Register 11	IDR11	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4D_H$	$007C4D_H$				
$007A4E_H$	$007C4E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4F_H$	$007C4F_H$				
$007A50_H$	$007C50_H$	ID Register 12	IDR12	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A51_H$	$007C51_H$				
$007A52_H$	$007C52_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A53_H$	$007C53_H$				
$007A54_H$	$007C54_H$	ID Register 13	IDR13	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A55_H$	$007C55_H$				
$007A56_H$	$007C56_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A57_H$	$007C57_H$				
$007A58_H$	$007C58_H$	ID Register 14	IDR14	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A59_H$	$007C59_H$				
$007A5A_H$	$007C5A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5B_H$	$007C5B_H$				
$007A5C_H$	$007C5C_H$	ID Register 15	IDR15	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5D_H$	$007C5D_H$				
$007A5E_H$	$007C5E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5F_H$	$007C5F_H$				

10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI^{2}OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC$_H$	—	—
INT9 instruction	N	—	#09	FFFFD8$_H$	—	—
Exception	N	—	#10	FFFFD4$_H$	—	—
CAN 0 RX	N	—	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N	—	#12	FFFFCC$_H$		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4$_H$		
CAN 2 RX / I^{2}C0	N	—	#15	FFFFC0$_H$	ICR02	0000B2$_H$
CAN 2 TX/NS	N	—	#16	FFFFBC$_H$		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8$_H$	ICR03	0000B3$_H$
16-bit Reload Timer 1	Y1	1	#18	FFFFB4$_H$		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit Reload Timer 3	Y1	—	#20	FFFFAC$_H$		
PPG 0/1/4/5	N	—	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG 2/3/6/7	N	—	#22	FFFFA4$_H$		
PPG 8/9/C/D	N	—	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG A/B/E/F	N	—	#24	FFFF9C$_H$		
Time Base Timer	N	—	#25	FFFF98$_H$	ICR07	0000B7$_H$
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94$_H$		
Watch Timer	N	—	#27	FFFF90$_H$	ICR08	0000B8$_H$
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C$_H$		
A/D Converter	Y1	5	#29	FFFF88$_H$	ICR09	0000B9$_H$
Free-run Timer 0 / Free-run Timer 1	N	—	#30	FFFF84$_H$		
Input Capture 4/5 / I^{2}C1	Y1	6	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C$_H$		
Input Capture 0 to 3	Y1	8	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output Compare 2/3/6/7	Y1	9	#34	FFFF74$_H$		
UART 0 RX	Y2	10	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART 0 TX	Y1	11	#36	FFFF6C$_H$		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64$_H$		

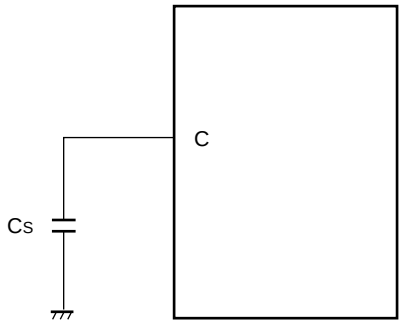
(Continued)

11.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.
Operating temperature	T_A	−40	—	+105	°C	

C Pin Connection Diagram

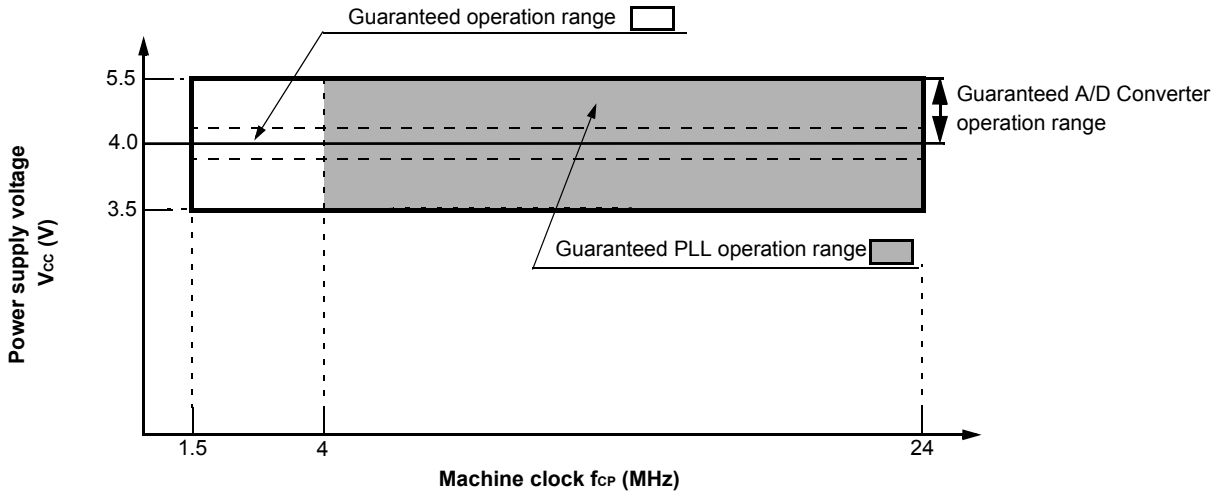


WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

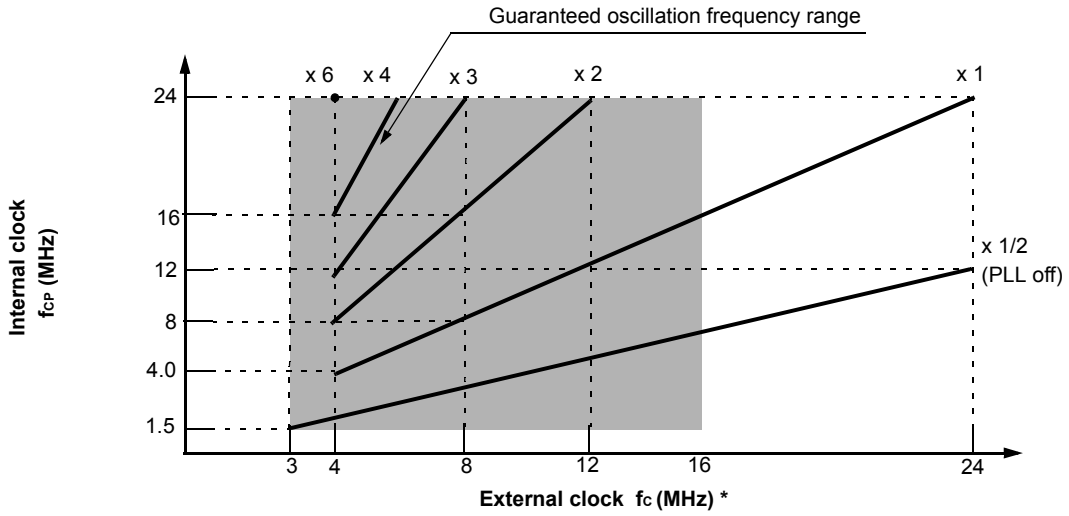
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Guaranteed PLL operation range



Guaranteed operation range of MB90340E series



* : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

11.8 Flash Memory Program/Erase Characteristics

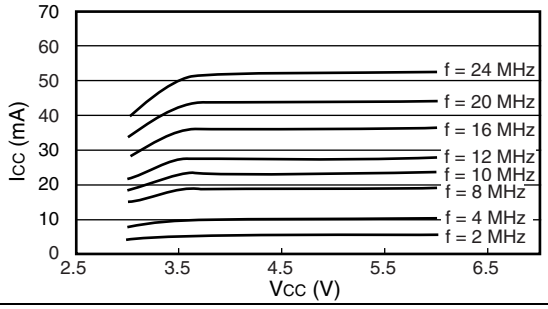
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25°C$ $V_{CC} = 5.0$ V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	µs	Except for the over head time of the system
Program/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average $T_A = +85°C$	20	—	—	year	*

* : This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85°C) .

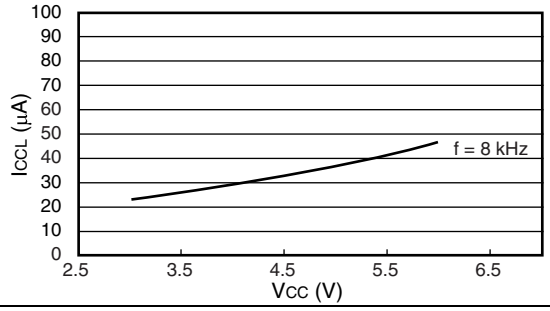
12. Example Characteristics

- MB90F346E, MB90F346ES, MB90F346CE, MB90F346CES

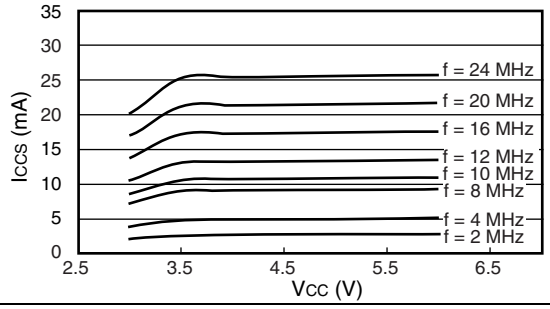
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



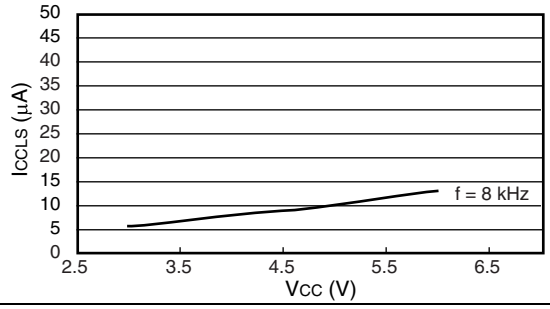
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



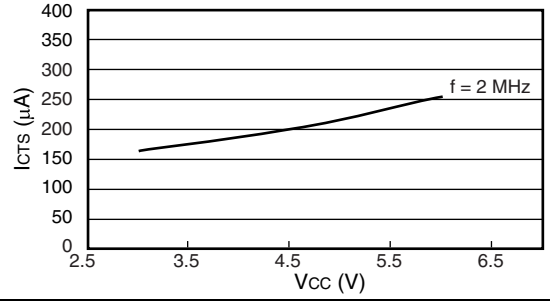
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



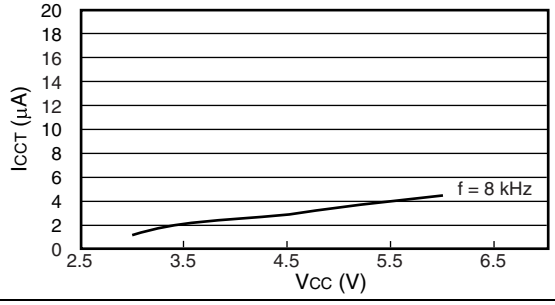
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



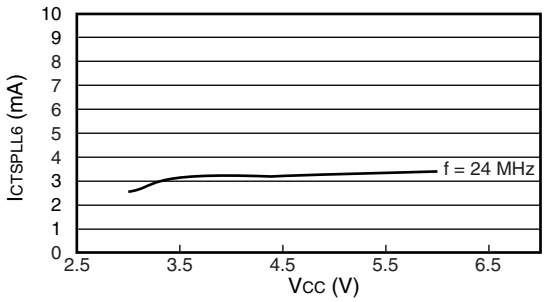
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



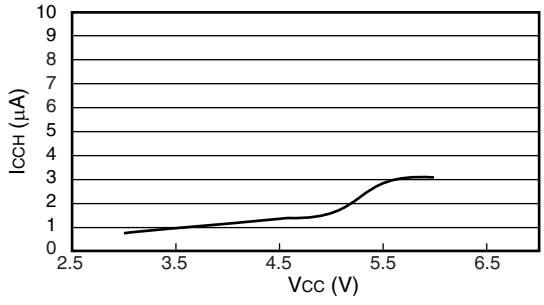
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency

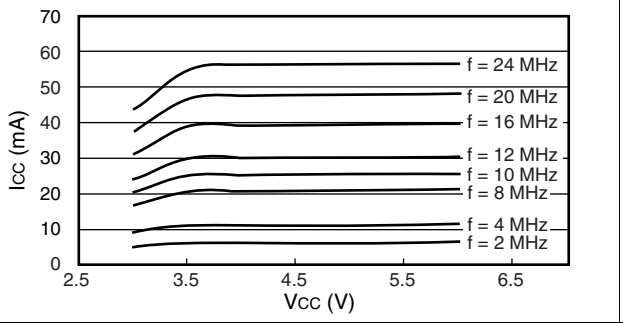


$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

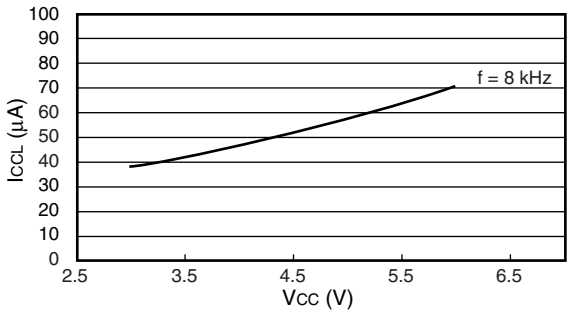


■ MB90F349E, MB90F349ES, MB90F349CE, MB90F349CES

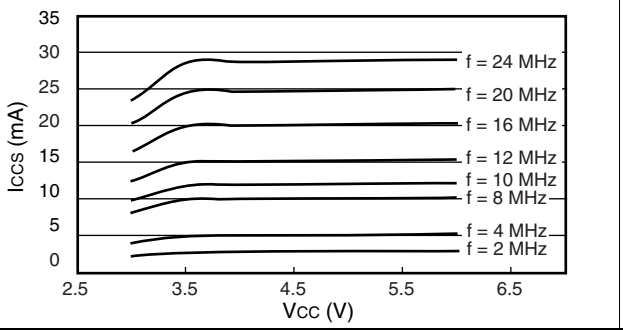
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



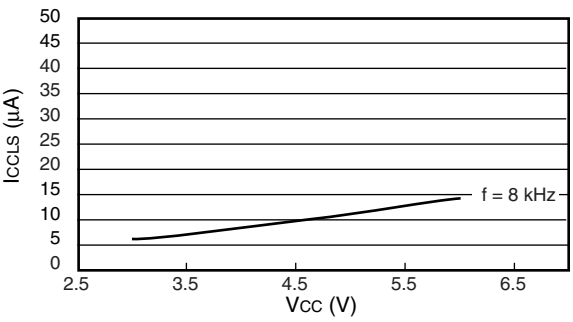
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



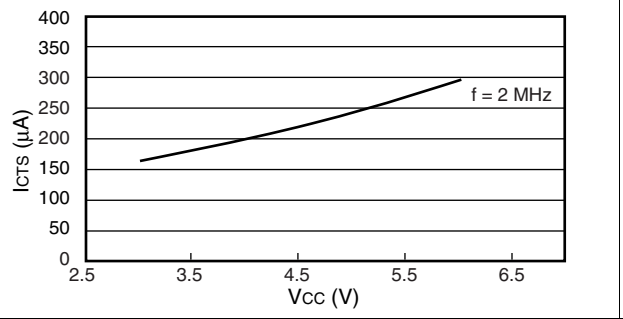
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



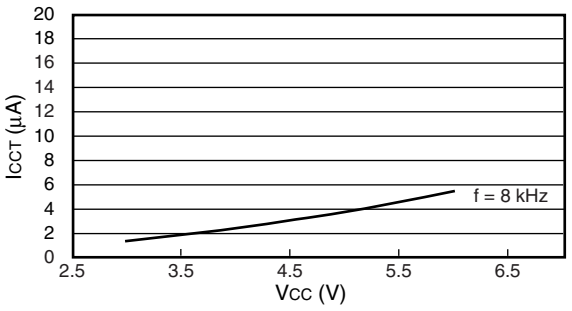
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



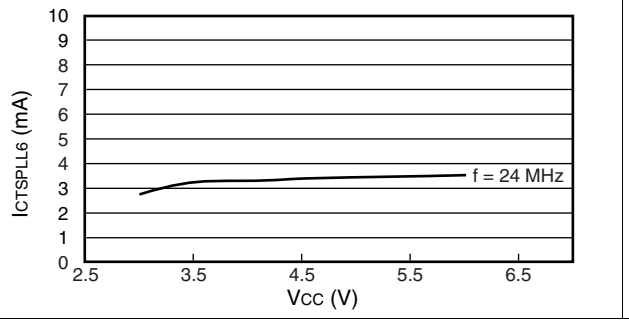
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



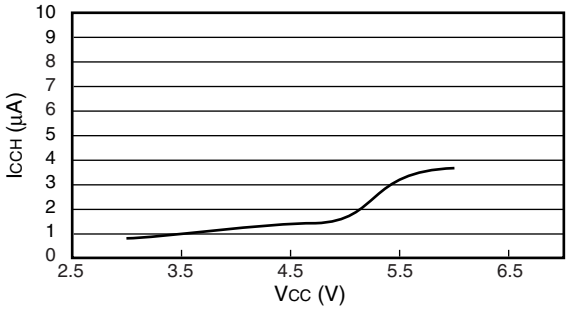
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency

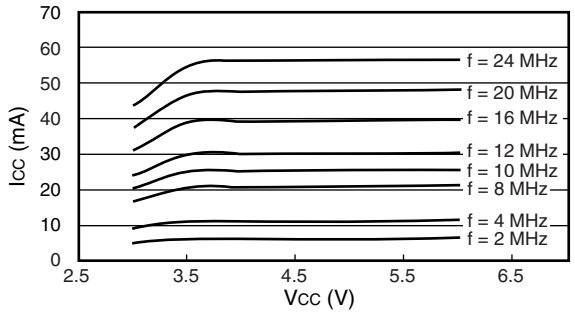


$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

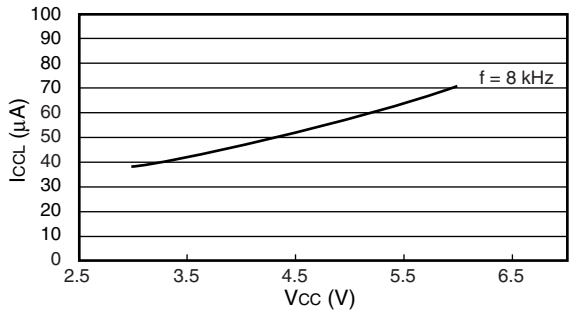


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

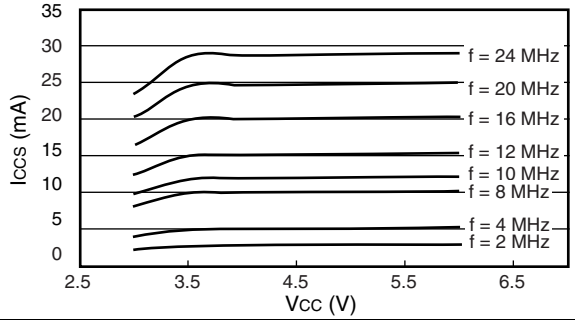
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



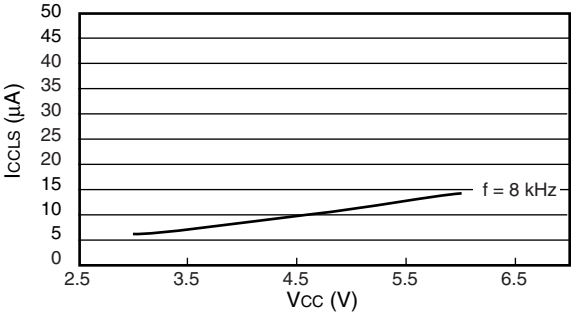
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



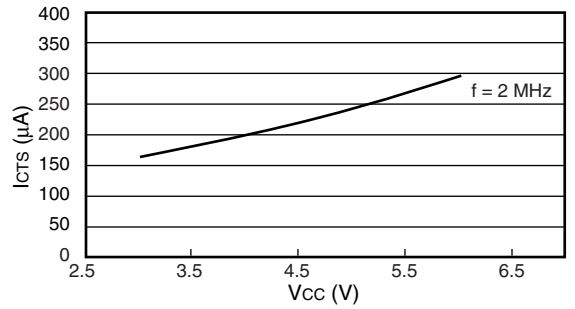
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



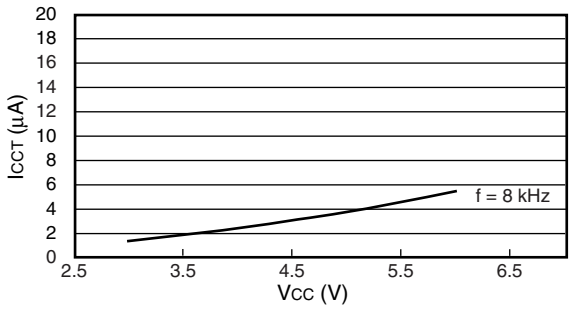
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



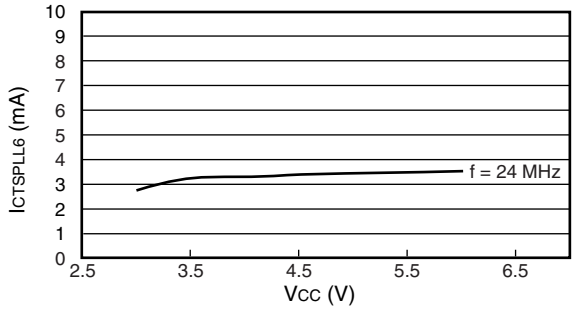
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



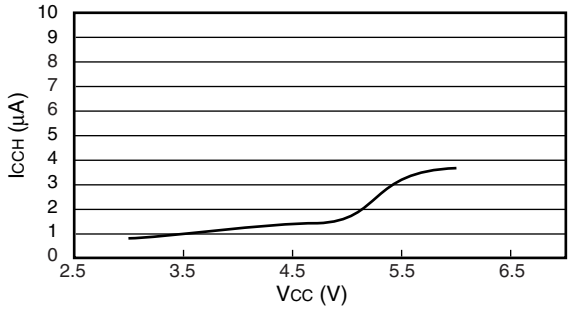
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped



Part number	Package	Remarks
MB90F347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F347ESPF		
MB90F347CEPF		
MB90F347CESPF		
MB90F347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F347ESPMC		
MB90F347CEPMC		
MB90F347CESPMC		
MB90F349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F349ESPF		
MB90F349CEPF		
MB90F349CESPF		
MB90F349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F349ESPMC		
MB90F349CEPMC		
MB90F349CESPMC		
MB90341EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90341ESPF		
MB90341CEPF		
MB90341CESPF		
MB90341EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90341ESPMC		
MB90341CEPMC		
MB90341CESPMC		
MB90342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90342ESPF		
MB90342CEPF		
MB90342CESPF		
MB90342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90342ESPMC		
MB90342CEPMC		
MB90342CESPMC		

(Continued)