



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

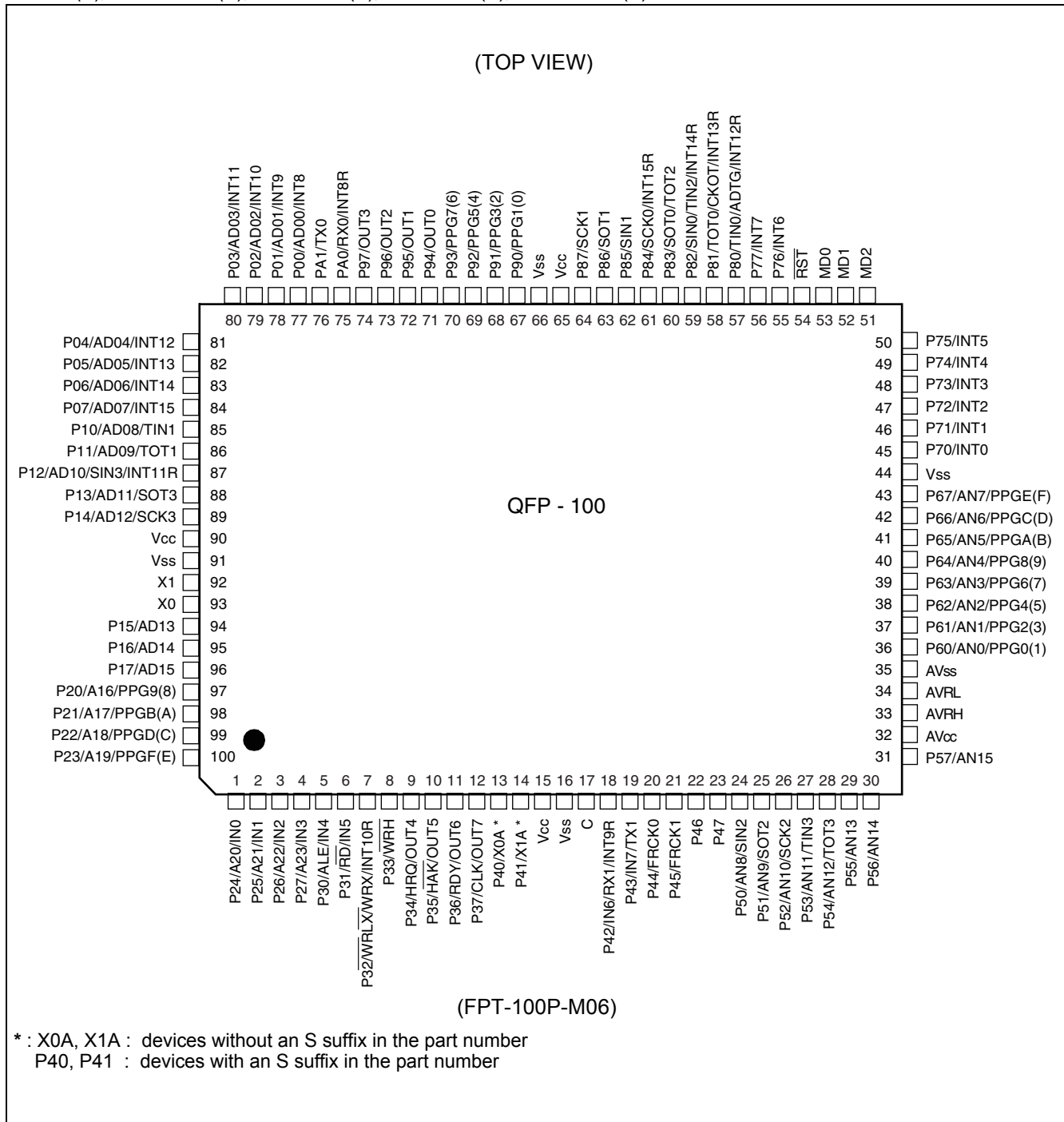
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-601e1

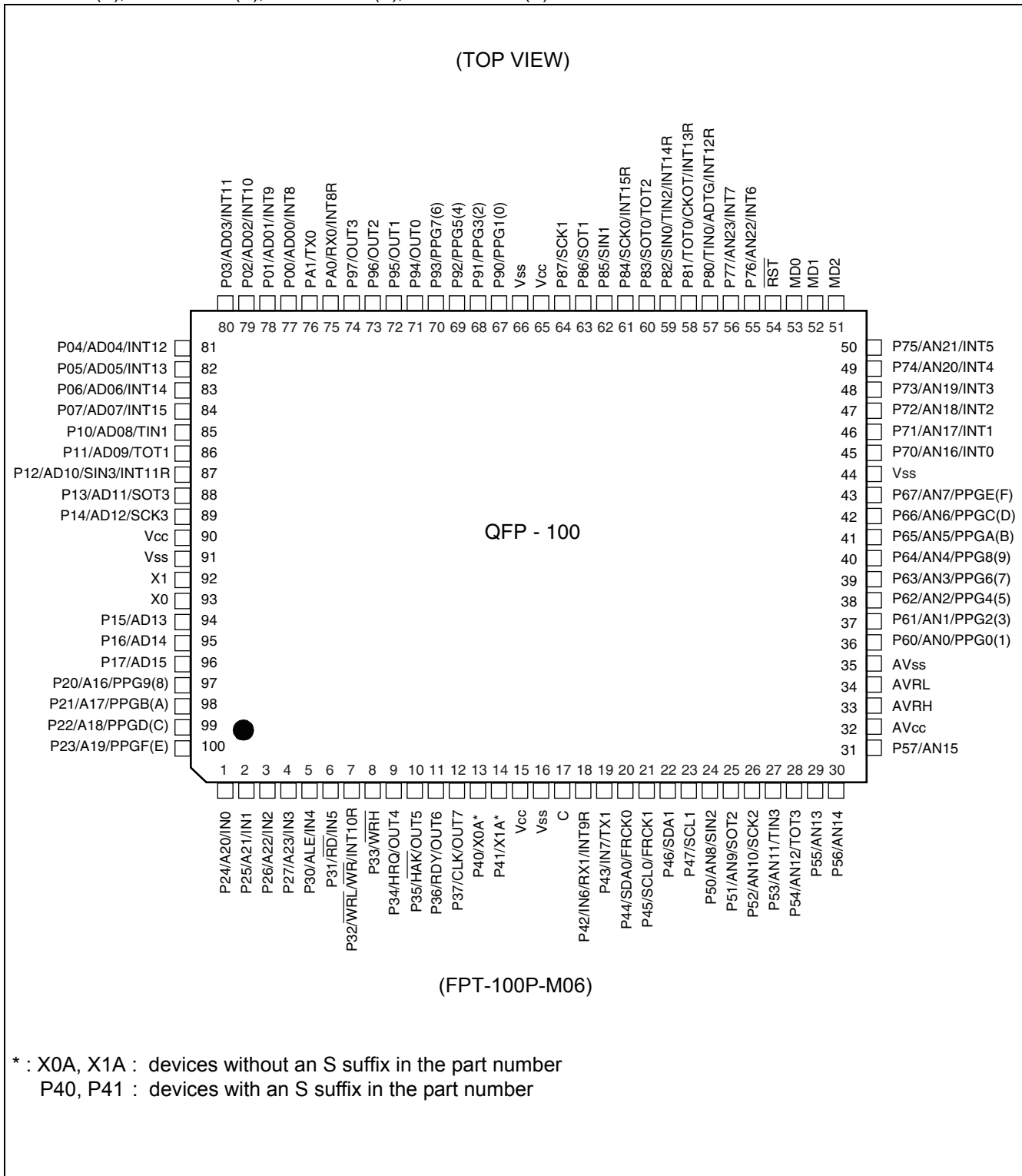
2. Pin Assignments

■ MB90341E(S), MB90342E(S), MB90F342E(S), MB90F345E(S), MB90346E(S), MB90F346E(S), MB90347E(S), MB90F347E(S), MB90348E(S), MB90349E(S), MB90F349E(S)



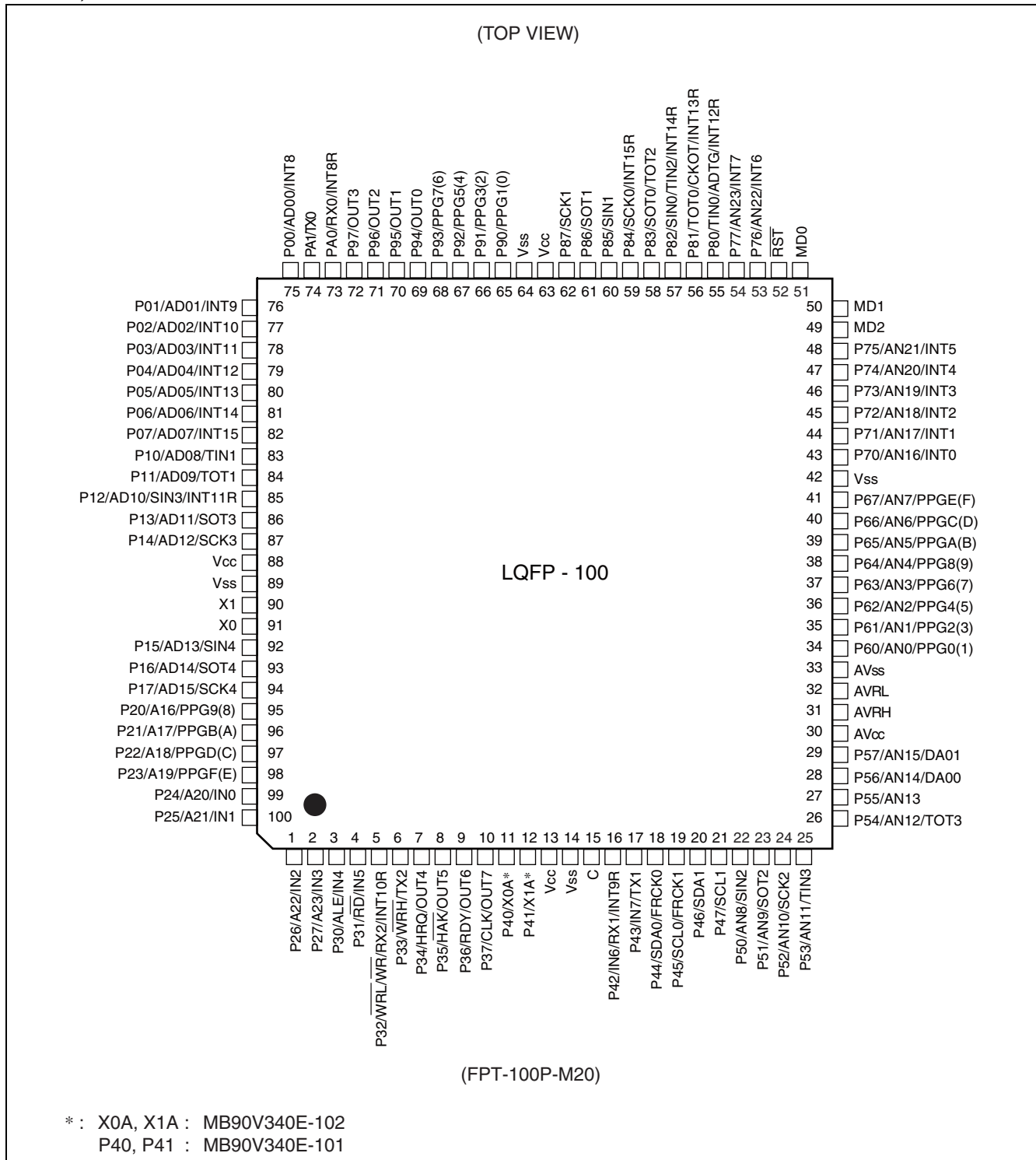
(Continued)

■ MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)



(Continued)

(Continued)



This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101)
		X0A, X1A	B	Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102)
15	13	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
16	14	V _{SS}	—	GND pin
17	15	C	K	This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 μF .
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture.
		RX1		RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only)
		INT9R		External interrupt request input pin

(Continued)

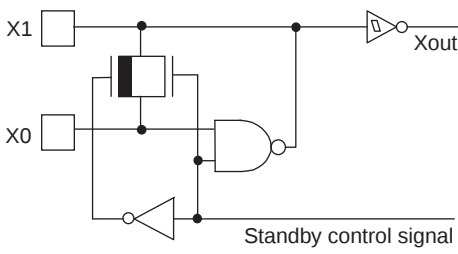
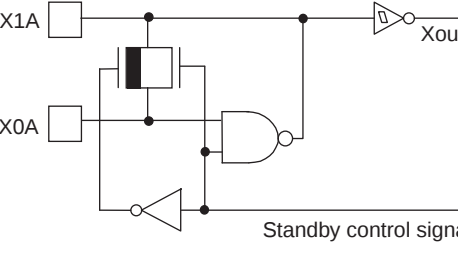
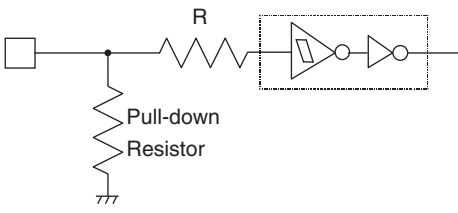
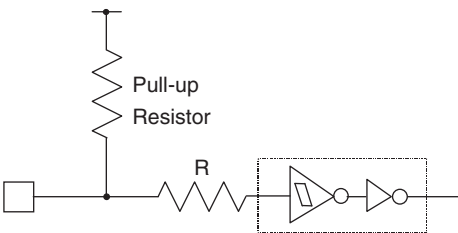
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV _{CC}	K	Analog power input pin for the A/D Converter

(Continued)

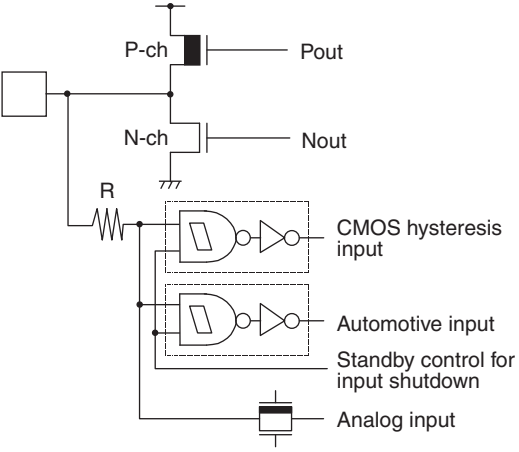
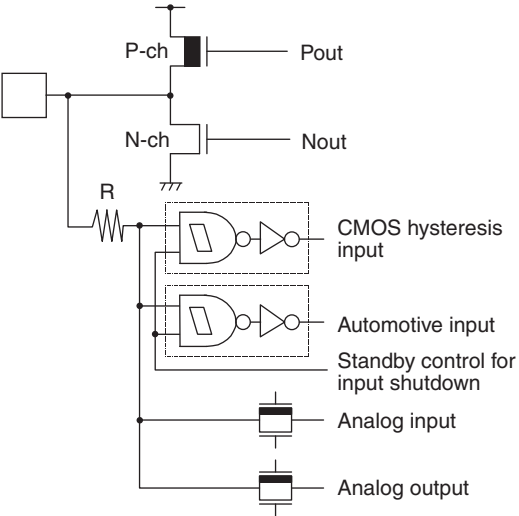
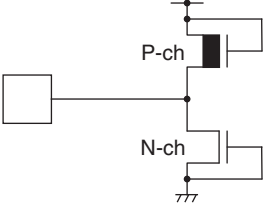
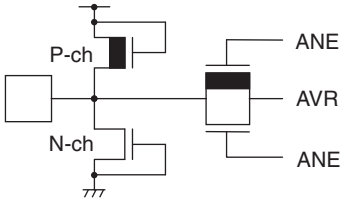
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
66	64	V _{SS}	—	GND pin
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pins
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pins
		OUT0 to OUT3		Waveform output pins for output compares. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin
76	74	PA1	F	General purpose I/O pin.
		TX0		TX Output pin for CAN0
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer

(Continued)

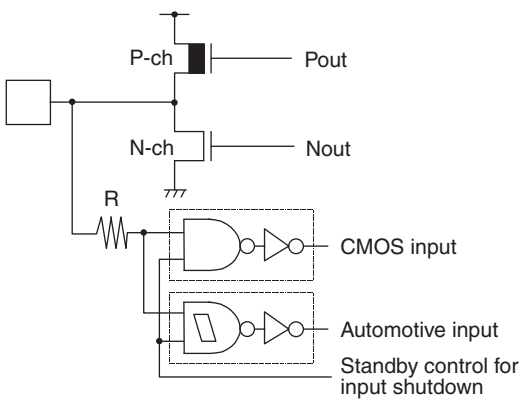
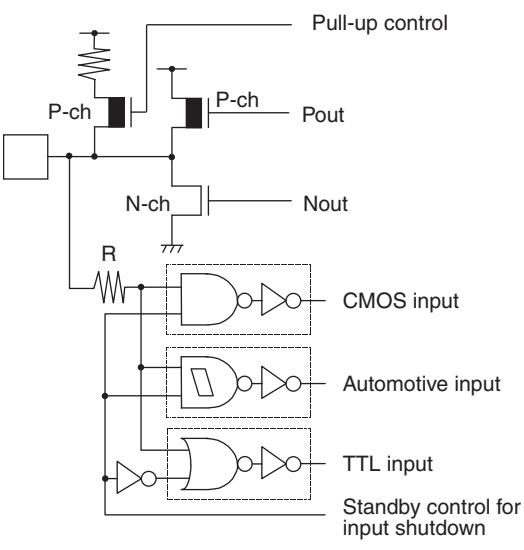
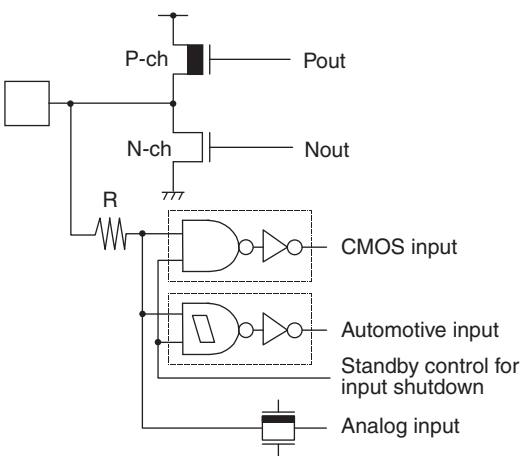
4. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		■ MASK ROM and evaluation products: CMOS hysteresis input pin ■ Flash memory products: CMOS input pin
D		MASK ROM and evaluation products: ■ CMOS hysteresis input pin ■ Pull-down resistor value: approx. 50 kΩ Flash memory products: ■ CMOS input pin ■ No pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ

(Continued)

Type	Circuit	Remarks
I		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
J		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ D/A analog output ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
K		Power supply input protection circuit
L		■ A/D converter reference voltage power supply input pin, with the protection circuit ■ Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH

(Continued)

Type	Circuit	Remarks
M		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
N		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) Programmable pull-up resistor: 50 kΩ approx
O		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input

5. Handling Devices

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC} , AV_{RH}) exceed the digital power-supply voltage.

2. Handling unused pins

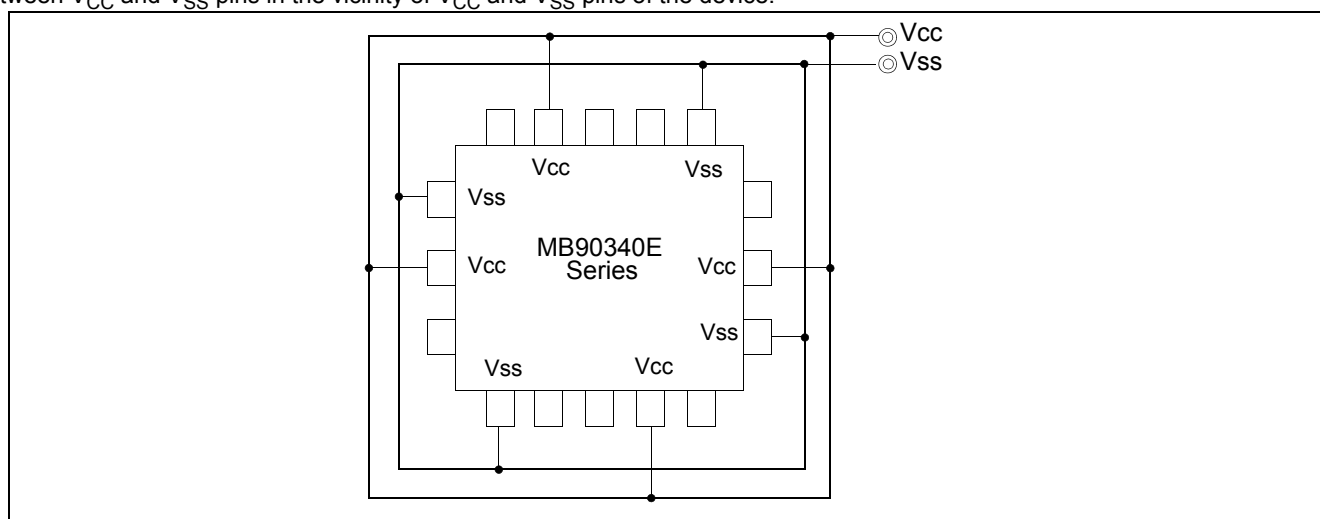
Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 k Ω or more.

3. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally. Connect V_{CC} and V_{SS} pins to the device from the current supply source at a possibly low impedance.

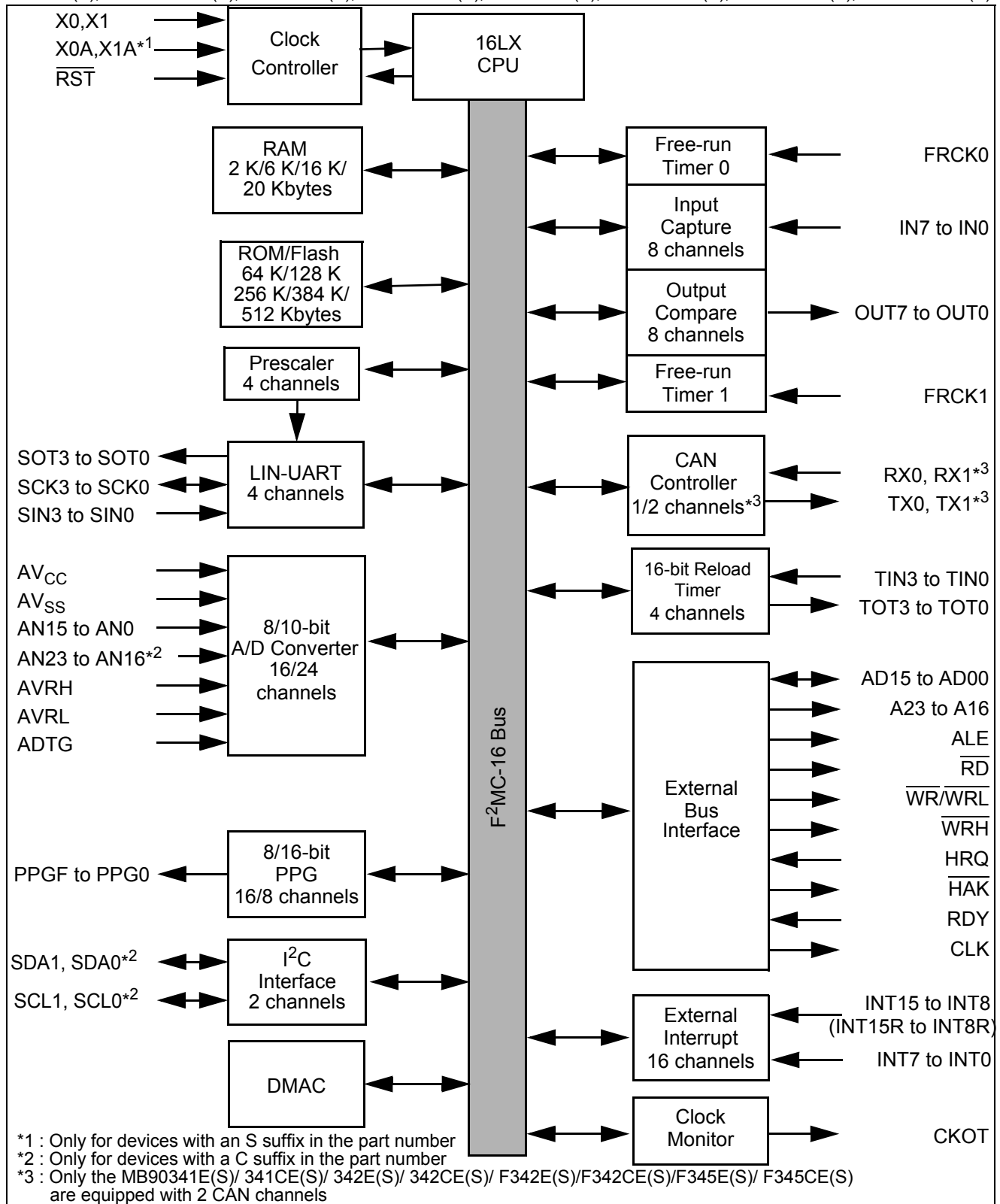
- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

■ MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)



8. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
000000 _H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX _B
000001 _H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX _B
000002 _H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX _B
000003 _H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX _B
000004 _H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX _B
000005 _H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX _B
000006 _H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX _B
000007 _H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX _B
000008 _H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX _B
000009 _H	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXXX _B
00000A _H	Port A Data Register	PDRA	R/W	Port A	XXXXXXXX _B
00000B _H	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	1111111 _B
00000C _H	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	1111111 _B
00000D _H	Port 7 Analog Input Enable Register	ADER7	R/W	Port 7, A/D	1111111 _B
00000E _H	Input Level Select Register 0	ILSR0	R/W	Ports	XXXXXXXX _B
00000F _H	Input Level Select Register 1	ILSR1	R/W	Ports	XXXX0XXX _B
000010 _H	Port 0 Direction Register	DDR0	R/W	Port 0	0000000 _B
000011 _H	Port 1 Direction Register	DDR1	R/W	Port 1	0000000 _B
000012 _H	Port 2 Direction Register	DDR2	R/W	Port 2	0000000 _B
000013 _H	Port 3 Direction Register	DDR3	R/W	Port 3	0000000 _B
000014 _H	Port 4 Direction Register	DDR4	R/W	Port 4	0000000 _B
000015 _H	Port 5 Direction Register	DDR5	R/W	Port 5	0000000 _B
000016 _H	Port 6 Direction Register	DDR6	R/W	Port 6	0000000 _B
000017 _H	Port 7 Direction Register	DDR7	R/W	Port 7	0000000 _B
000018 _H	Port 8 Direction Register	DDR8	R/W	Port 8	0000000 _B
000019 _H	Port 9 Direction Register	DDR9	R/W	Port 9	0000000 _B
00001A _H	Port A Direction Register	DDRA	R/W	Port A	00000100 _B
00001B _H	Reserved				
00001C _H	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	0000000 _B
00001D _H	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	0000000 _B
00001E _H	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	0000000 _B
00001F _H	Port 3 Pull-up Control Register	PUCR3	W, R/W	Port 3	0000000 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000020 _H	Serial Mode Register 0	SMR0	W,R/W	UART0	00000000 _B
000021 _H	Serial Control Register 0	SCR0	W,R/W		00000000 _B
000022 _H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000 _B
000023 _H	Serial Status Register 0	SSR0	R,R/W		00001000 _B
000024 _H	Extended Communication Control Register 0	ECCR0	R,W, R/W		000000XX _B
000025 _H	Extended Status/Control Register 0	ESCR0	R/W		00000100 _B
000026 _H	Baud Rate Generator Register 00	BGR00	R/W		00000000 _B
000027 _H	Baud Rate Generator Register 01	BGR01	R/W		00000000 _B
000028 _H	Serial Mode Register 1	SMR1	W,R/W	UART1	00000000 _B
000029 _H	Serial Control Register 1	SCR1	W,R/W		00000000 _B
00002A _H	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000 _B
00002B _H	Serial Status Register 1	SSR1	R,R/W		00001000 _B
00002C _H	Extended Communication Control Register 1	ECCR1	R,W, R/W		000000XX _B
00002D _H	Extended Status/Control Register 1	ESCR1	R/W		00000100 _B
00002E _H	Baud Rate Generator Register 10	BGR10	R/W		00000000 _B
00002F _H	Baud Rate Generator Register 11	BGR11	R/W		00000000 _B
000030 _H	PPG 0 Operation Mode Control Register	PPGC0	W,R/W	16-bit PPG 0/1	0X000XX1 _B
000031 _H	PPG 1 Operation Mode Control Register	PPGC1	W,R/W		0X000001 _B
000032 _H	PPG 0/PPG 1 Count Clock Select Register	PPG01	R/W		000000X0 _B
000033 _H	Reserved				
000034 _H	PPG 2 Operation Mode Control Register	PPGC2	W,R/W	16-bit PPG 2/3	0X000XX1 _B
000035 _H	PPG 3 Operation Mode Control Register	PPGC3	W,R/W		0X000001 _B
000036 _H	PPG 2/PPG 3 Count Clock Select Register	PPG23	R/W		000000X0 _B
000037 _H	Reserved				
000038 _H	PPG 4 Operation Mode Control Register	PPGC4	W,R/W	16-bit PPG 4/5	0X000XX1 _B
000039 _H	PPG 5 Operation Mode Control Register	PPGC5	W,R/W		0X000001 _B
00003A _H	PPG 4/PPG 5 Clock Select Register	PPG45	R/W		000000X0 _B
00003B _H	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000 _B
00003C _H	PPG 6 Operation Mode Control Register	PPGC6	W,R/W	16-bit PPG 6/7	0X000XX1 _B
00003D _H	PPG 7 Operation Mode Control Register	PPGC7	W,R/W		0X000001 _B
00003E _H	PPG 6/PPG 7 Count Clock Control Register	PPG67	R/W		000000X0 _B
00003F _H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007900 _H	Reload Register L0	PRL0	R/W	16-bit PPG 0/1	XXXXXXXX _B
007901 _H	Reload Register H0	PRLH0	R/W		XXXXXXXX _B
007902 _H	Reload Register L1	PRL1	R/W		XXXXXXXX _B
007903 _H	Reload Register H1	PRLH1	R/W		XXXXXXXX _B
007904 _H	Reload Register L2	PRL2	R/W	16-bit PPG 2/3	XXXXXXXX _B
007905 _H	Reload Register H2	PRLH2	R/W		XXXXXXXX _B
007906 _H	Reload Register L3	PRL3	R/W		XXXXXXXX _B
007907 _H	Reload Register H3	PRLH3	R/W		XXXXXXXX _B
007908 _H	Reload Register L4	PRL4	R/W	16-bit PPG 4/5	XXXXXXXX _B
007909 _H	Reload Register H4	PRLH4	R/W		XXXXXXXX _B
00790A _H	Reload Register L5	PRL5	R/W		XXXXXXXX _B
00790B _H	Reload Register H5	PRLH5	R/W		XXXXXXXX _B
00790C _H	Reload Register L6	PRL6	R/W	16-bit PPG 6/7	XXXXXXXX _B
00790D _H	Reload Register H6	PRLH6	R/W		XXXXXXXX _B
00790E _H	Reload Register L7	PRL7	R/W		XXXXXXXX _B
00790F _H	Reload Register H7	PRLH7	R/W		XXXXXXXX _B
007910 _H	Reload Register L8	PRL8	R/W	16-bit PPG 8/9	XXXXXXXX _B
007911 _H	Reload Register H8	PRLH8	R/W		XXXXXXXX _B
007912 _H	Reload Register L9	PRL9	R/W		XXXXXXXX _B
007913 _H	Reload Register H9	PRLH9	R/W		XXXXXXXX _B
007914 _H	Reload Register LA	PRLA	R/W	16-bit PPG A/B	XXXXXXXX _B
007915 _H	Reload Register HA	PRLHA	R/W		XXXXXXXX _B
007916 _H	Reload Register LB	PRLB	R/W		XXXXXXXX _B
007917 _H	Reload Register HB	PRLHB	R/W		XXXXXXXX _B
007918 _H	Reload Register LC	PRLC	R/W	16-bit PPG C/D	XXXXXXXX _B
007919 _H	Reload Register HC	PRLHC	R/W		XXXXXXXX _B
00791A _H	Reload Register LD	PRLD	R/W		XXXXXXXX _B
00791B _H	Reload Register HD	PRLHD	R/W		XXXXXXXX _B
00791C _H	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	XXXXXXXX _B
00791D _H	Reload Register HE	PRLHE	R/W		XXXXXXXX _B
00791E _H	Reload Register LF	PRLLF	R/W		XXXXXXXX _B
00791F _H	Reload Register HF	PRLHF	R/W		XXXXXXXX _B
007920 _H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
007921 _H	Input Capture 0	IPCP0	R		XXXXXXXX _B
007922 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
007923 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007948 _H	Timer 0/Reload 0	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX _B
007949 _H			R/W		XXXXXXXX _B
00794A _H	Timer 1/Reload 1	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX _B
00794B _H			R/W		XXXXXXXX _B
00794C _H	Timer 2/Reload 2	TMR2/TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX _B
00794D _H			R/W		XXXXXXXX _B
00794E _H	Timer 3/Reload 3	TMR3/TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX _B
00794F _H			R/W		XXXXXXXX _B
007950 _H	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000 _B
007951 _H	Serial Control Register 3	SCR3	W,R/W		00000000 _B
007952 _H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000 _B
007953 _H	Serial Status Register 3	SSR3	R,R/W		00001000 _B
007954 _H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XX _B
007955 _H	Extended Status Control Register	ESCR3	R/W		00000100 _B
007956 _H	Baud Rate Generator Register 30	BGR30	R/W		00000000 _B
007957 _H	Baud Rate Generator Register 31	BGR31	R/W		00000000 _B
007958 _H	Serial Mode Register 4	SMR4	W,R/W	UART4	00000000 _B
007959 _H	Serial Control Register 4	SCR4	W,R/W		00000000 _B
00795A _H	Reception/Transmission Data Register 4	RDR4/TDR4	R/W		00000000 _B
00795B _H	Serial Status Register 4	SSR4	R,R/W		00001000 _B
00795C _H	Extended Communication Control Register 4	ECCR4	R,W, R/W		000000XX _B
00795D _H	Extended Status Control Register	ESCR4	R/W		00000100 _B
00795E _H	Baud Rate Generator Register 40	BGR40	R/W		00000000 _B
00795F _H	Baud Rate Generator Register 41	BGR41	R/W		00000000 _B
007960 _H to 00796B _H	Reserved				
00796C _H	Clock Output Enable Register	CLKR	R/W	Clock Monitor	XXXX0000 _B
00796D _H	Reserved				
00796E _H	CAN Direct Mode Register	CDMR	R/W	CAN Clock sync	XXXXXXX0 _B
00796F _H	CAN Switch Register	CANSWR	R/W	CAN 0/1	XXXXXXX0 _B

(Continued)

11.3 DC Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{IHS}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{IHA}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected
	V_{IHS}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHI}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{ILA}	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if Automotive input levels are selected
	V_{ILT}	—	—	$V_{SS} - 0.3$	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILI}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	V_{OHI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	V_{OL}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Output L voltage	V_{OLI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 3.0\text{ mA}$	—	—	0.4	V	

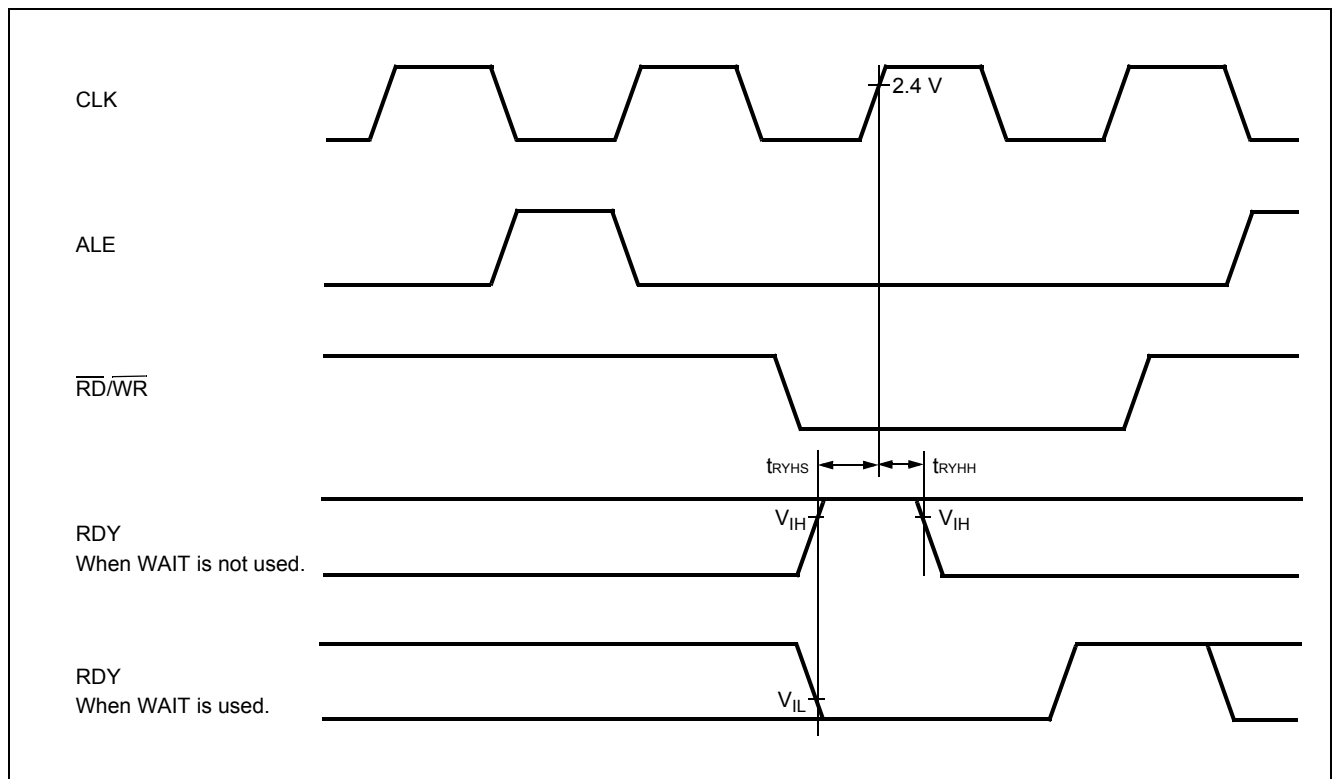
(Continued)

11.4.7 Ready Input Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	$f_{CP} = 16\text{ MHz}$
				32	—	ns	$f_{CP} = 24\text{ MHz}$
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note: : If the RDY setup time is insufficient, use the auto-ready function.

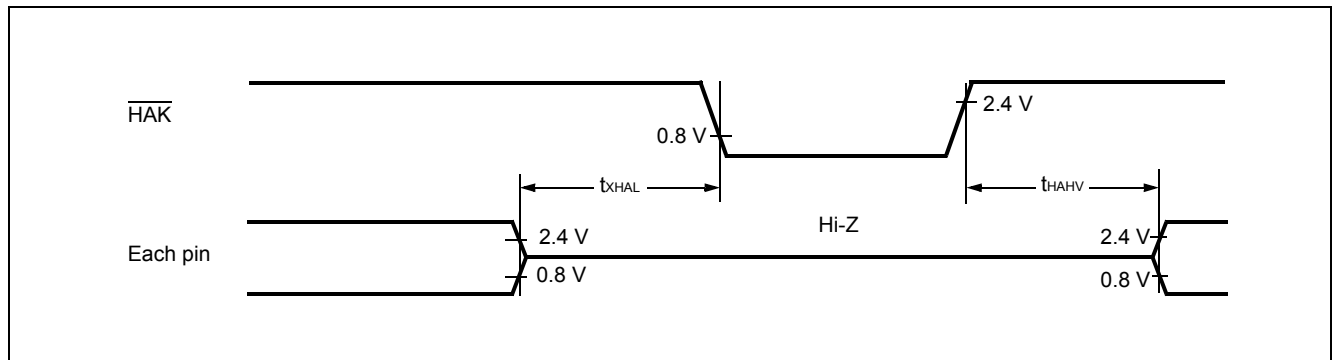


11.4.8 Hold Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Pin floating $\rightarrow \overline{\text{HAK}} \downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	t_{CP}	ns
$\overline{\text{HAK}} \uparrow$ time $\rightarrow$ Pin valid time	t_{HAHV}	$\overline{\text{HAK}}$	—	t_{CP}	$2 t_{CP}$	ns

Note: : There is more than 1 cycle from when HRQ reads in until the $\overline{\text{HAK}}$ is changed.



11.4.13 I²C Timing

(T_A = -40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V)

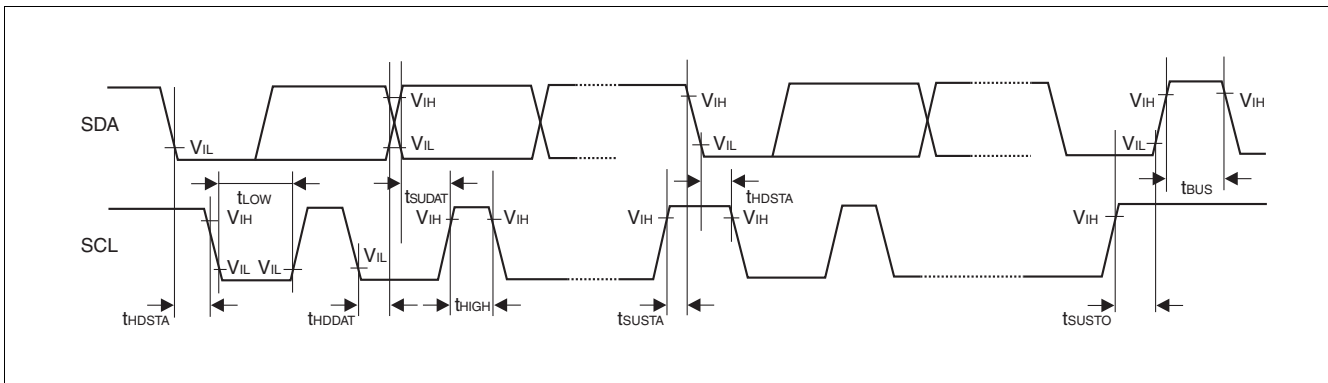
Parameter	Symbol	Condition	Standard-mode		Fast-mode* ¹		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	R = 1.7 kΩ ₂ C = 50 pF* ²	0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t _{HDSTA}		4.0	—	0.6	—	μs
"L" width of the SCL clock	t _{LOW}		4.7	—	1.3	—	μs
"H" width of the SCL clock	t _{HIGH}		4.0	—	0.6	—	μs
Set-up time (repeated) START condition SCL ↑ → SDA ↓	t _{SUSTA}		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}		0	3.45* ³	0	0.9* ⁴	μs
Data set-up time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t _{SUSTO}		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t _{BUS}		4.7	—	1.3	—	μs

*1: For use at over 100 kHz, set the machine clock to at least 6 MHz.

*2: R, C: Pull-up resistor and load capacitor of the SCL and SDA lines.

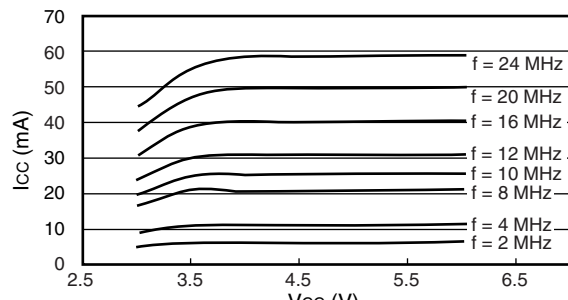
*3: The maximum t_{HDDAT} meets the requirement that it does not extend the "L" width (t_{LOW}) of the SCL signal.

*4: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.

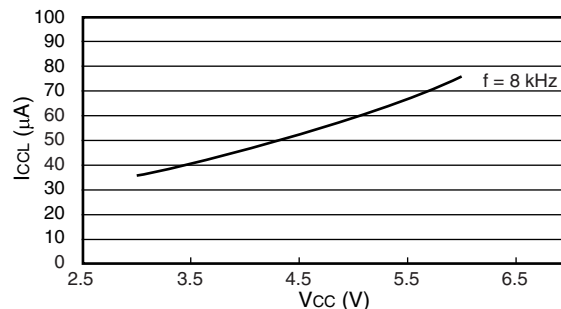


■ MB90F345E, MB90F345ES, MB90F345CE, MB90F345CES

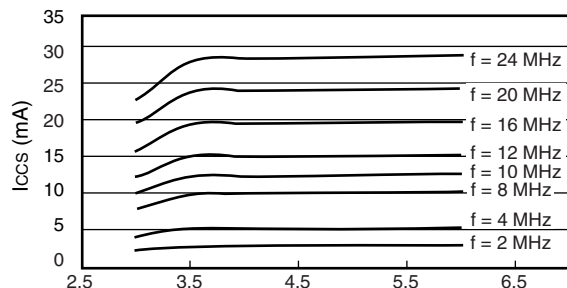
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



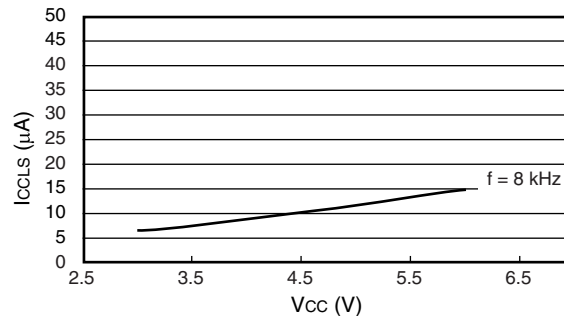
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



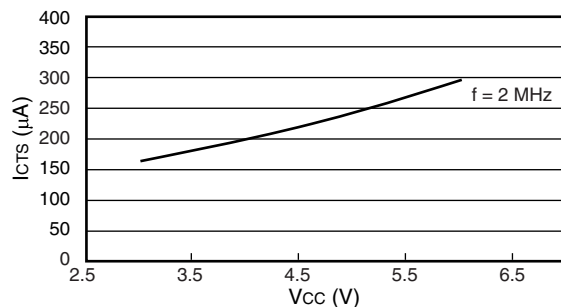
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



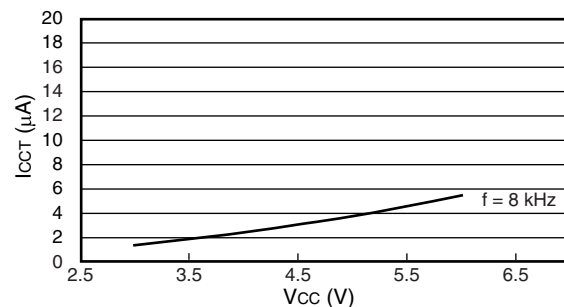
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



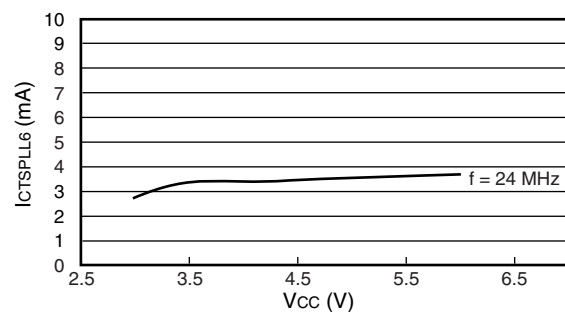
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped

