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What is "[Embedded - Microcontrollers](#)"?

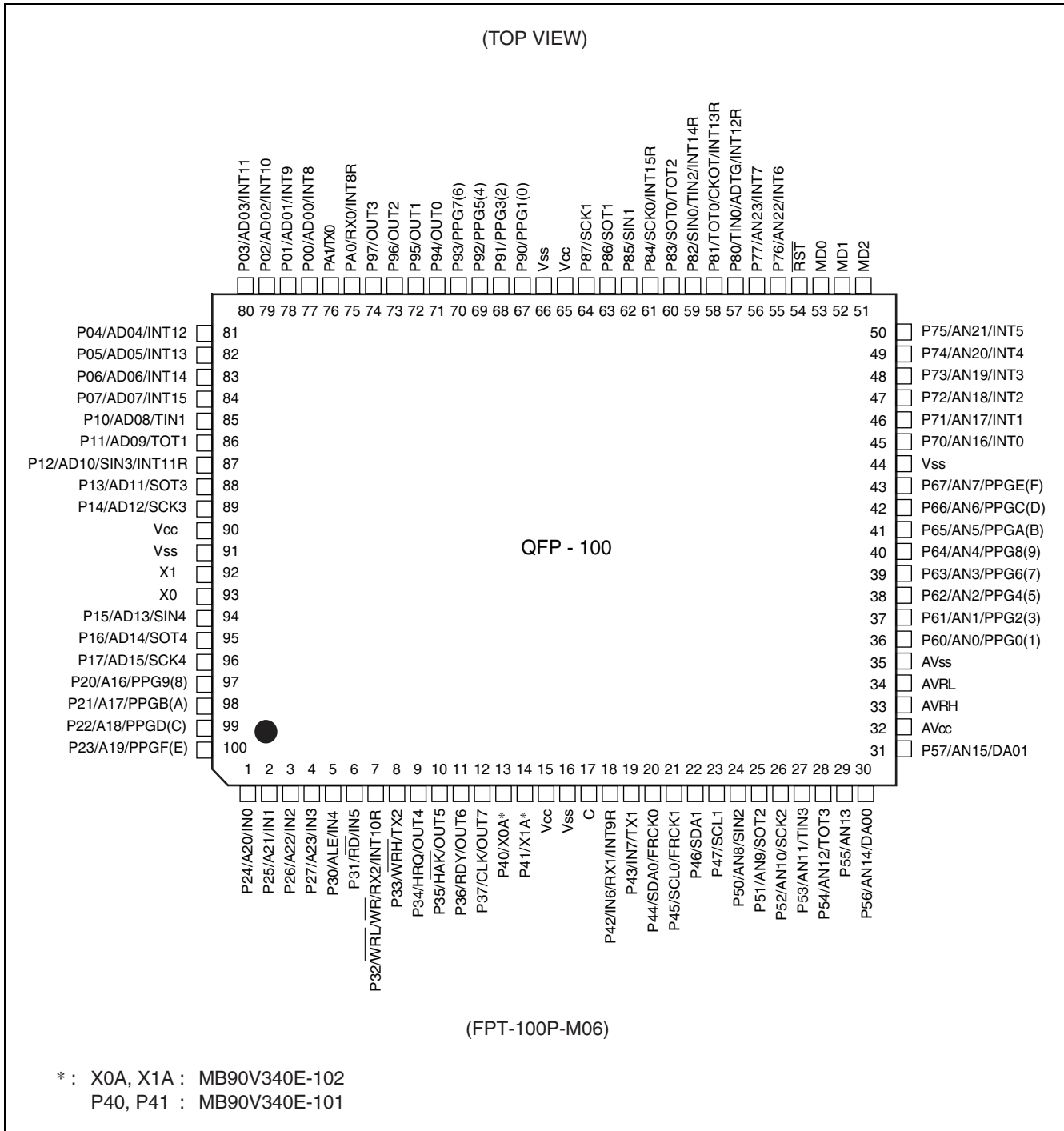
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

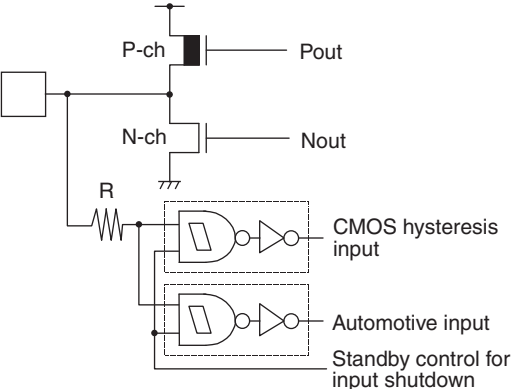
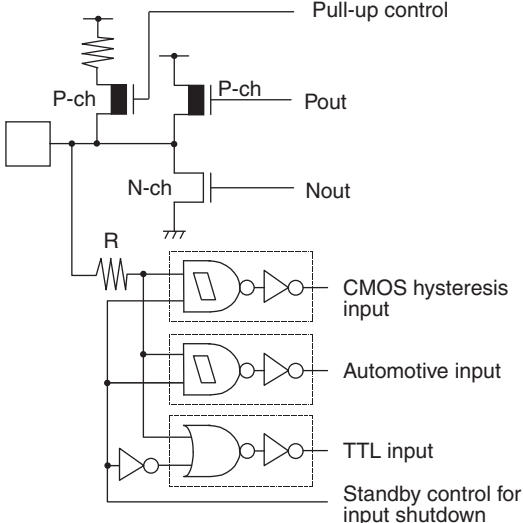
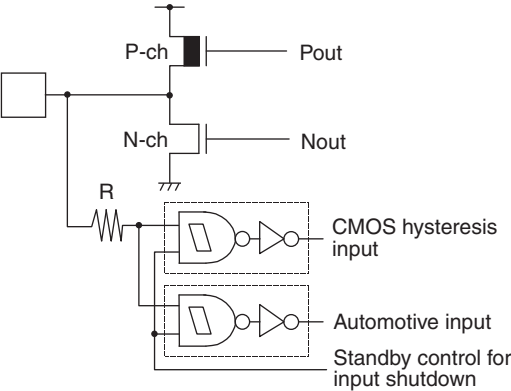
Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-612e1

■ MB90V340E-101/MB90V340E-102



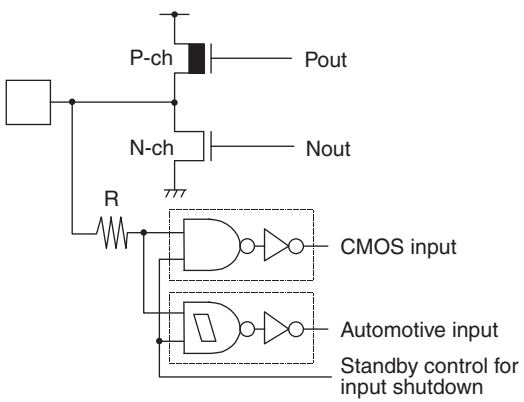
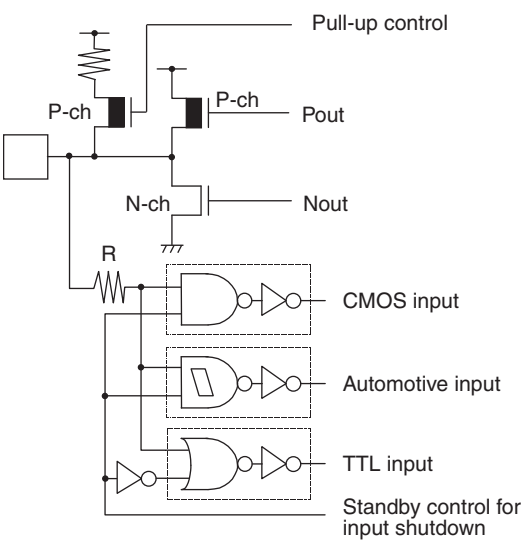
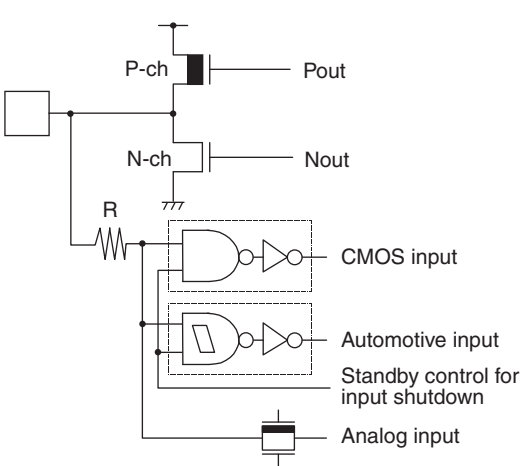
This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

(Continued)

Type	Circuit	Remarks
F		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
G		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) ■ Programmable pull-up resistor: 50 kΩ approx.
H		■ CMOS level output ($I_{OL} = 3 \text{ mA}$, $I_{OH} = -3 \text{ mA}$) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)

(Continued)

(Continued)

Type	Circuit	Remarks
M		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
N		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) Programmable pull-up resistor: 50 kΩ approx
O		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input

5. Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , $AVRH$, $AVRL$) and analog inputs ($AN0$ to $AN23$) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed $AVRH$ or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

6. Connection of Unused A/D Converter Pins when the A/D Converter is Used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

7. Crystal Oscillator Circuit

The X0, X1 pins and X0A, X1A pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

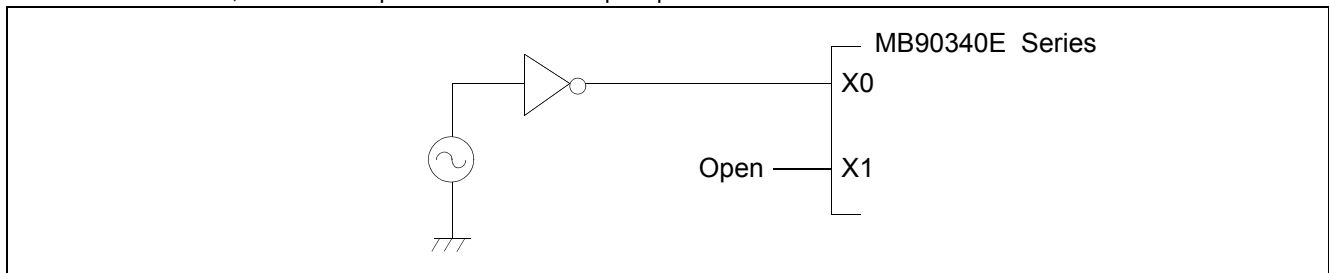
For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

8. Pull-up/down resistors

The MB90340E Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

9. Using external clock

To use an external clock, drive the X0 pin and leave the X1 pin open.



10. Precautions when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

11. Notes on operation in PLL clock mode

If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

12. Notes on Power-On

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50 μ s or more (0.2 V to 2.7 V)

MB90342E(S)/342CE(S)
MB90F342E(S)/F342CE(S)
MB90349E(S)/349CE(S)
MB90F349E(S)/F349CE(S)

MB90341E(S)/341CE(S)
MB90348E(S)/348CE(S)

MB90347E(S)/347CE(S)
MB90F347E(S)/F347CE(S)

MB90346E(S)/346CE(S)
MB90F346E(S)/F346CE(S)

000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral
	External access area		External access area		External access area		External access area
000100H		000100H		000100H	RAM 6 Kbytes	000100H	RAM 2 Kbytes
	RAM 16 Kbytes		RAM 16 Kbytes	0018FFH		0008FFH	
003FFFH		003FFFH					
007900H		007900H		007900H		007900H	
007FFFH	Peripheral	007FFFH	Peripheral	007FFFH	Peripheral	007FFFH	Peripheral
008000H		008000H		008000H		008000H	
00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)
	External access area		External access area		External access area		External access area
FC0000H							
FCFFFFH	ROM (FC bank)						
FD0000H							
FDFFFFH	ROM (FD bank)						
FE0000H		FE0000H		FE0000H		FE0000H	
FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	
FF0000H		FF0000H		FF0000H		FF0000H	
FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)

 : Not accessible

Note: :An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.

For example, when the address 00C000_H is accessed, the data at FFC000_H in ROM is actually accessed.

The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.

As a result, the image between FF8000_H and FFFFFFF_H is visible in bank 00, while the image between FF0000_H and FF7FFF_H is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
000060 _H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000 _B
000061 _H	Timer Control Status 0	TMCSR0	R/W		XXXX0000 _B
000062 _H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000 _B
000063 _H	Timer Control Status 1	TMCSR1	R/W		XXXX0000 _B
000064 _H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000 _B
000065 _H	Timer Control Status 2	TMCSR2	R/W		XXXX0000 _B
000066 _H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000 _B
000067 _H	Timer Control Status 3	TMCSR3	R/W		XXXX0000 _B
000068 _H	A/D Control Status 0	ADCS0	R/W	A/D Converter	000XXXX0 _B
000069 _H	A/D Control Status 1	ADCS1	R/W		0000000X _B
00006A _H	A/D Data 0	ADCR0	R		00000000 _B
00006B _H	A/D Data 1	ADCR1	R		XXXXXX00 _B
00006C _H	ADC Setting 0	ADSR0	R/W		00000000 _B
00006D _H	ADC Setting 1	ADSR1	R/W		00000000 _B
00006E _H	Reserved				
00006F _H	ROM Mirror Function Select	ROMM	W	ROM Mirror	XXXXXXXX1 _B
000070 _H to 00008F _H	Reserved for CAN Controller 0/1. Refer to “CAN Controllers”				
000090 _H to 00009A _H	Reserved				
00009B _H	DMA Descriptor Channel Specified Register	DCSR	R/W	DMA	00000000 _B
00009C _H	DMA Status L Register	DSRL	R/W		00000000 _B
00009D _H	DMA Status H Register	DSRH	R/W		00000000 _B
00009E _H	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000 _B
00009F _H	Delayed Interrupt Trigger/Release Register	DIRR	R/W	Delayed Interrupt	XXXXXXXX0 _B
0000A0 _H	Low-power Mode Control Register	LPMCR	W,R/W	Low Power Control Circuit	00011000 _B
0000A1 _H	Clock Selection Register	CKSCR	R,R/W	Low Power Control Circuit	11111100 _B
0000A2 _H , 0000A3 _H	Reserved				
0000A4 _H	DMA Stop Status Register	DSSR	R/W	DMA	00000000 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0000A5 _H	Automatic Ready Function Select Register	ARSR	W	External Memory Access	0011XX00 _B
0000A6 _H	External Address Output Control Register	HACR	W		00000000 _B
0000A7 _H	Bus Control Signal Selection Register	ECSR	W		0000000X _B
0000A8 _H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXXX11 _B
0000A9 _H	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	1XX00100 _B
0000AA _H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 _B
0000AB _H	Reserved				
0000AC _H	DMA Enable L Register	DERL	R/W	DMA	00000000 _B
0000AD _H	DMA Enable H Register	DERH	R/W		00000000 _B
0000AE _H	Flash Control Status Register (Flash memory devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000 _B
0000AF _H	Reserved				
0000B0 _H	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111 _B
0000B1 _H	Interrupt Control Register 01	ICR01	W,R/W		00000111 _B
0000B2 _H	Interrupt Control Register 02	ICR02	W,R/W		00000111 _B
0000B3 _H	Interrupt Control Register 03	ICR03	W,R/W		00000111 _B
0000B4 _H	Interrupt Control Register 04	ICR04	W,R/W		00000111 _B
0000B5 _H	Interrupt Control Register 05	ICR05	W,R/W		00000111 _B
0000B6 _H	Interrupt Control Register 06	ICR06	W,R/W		00000111 _B
0000B7 _H	Interrupt Control Register 07	ICR07	W,R/W		00000111 _B
0000B8 _H	Interrupt Control Register 08	ICR08	W,R/W		00000111 _B
0000B9 _H	Interrupt Control Register 09	ICR09	W,R/W		00000111 _B
0000BA _H	Interrupt Control Register 10	ICR10	W,R/W		00000111 _B
0000BB _H	Interrupt Control Register 11	ICR11	W,R/W		00000111 _B
0000BC _H	Interrupt Control Register 12	ICR12	W,R/W		00000111 _B
0000BD _H	Interrupt Control Register 13	ICR13	W,R/W		00000111 _B
0000BE _H	Interrupt Control Register 14	ICR14	W,R/W		00000111 _B
0000BF _H	Interrupt Control Register 15	ICR15	W,R/W		00000111 _B
0000C0 _H	D/A Converter Data 0	DAT0	R/W	D/A Converter	XXXXXXXX _B
0000C1 _H	D/A Converter Data 1	DAT1	R/W		XXXXXXXX _B
0000C2 _H	D/A Control 0	DACR0	R/W		XXXXXXXX0 _B
0000C3 _H	D/A Control 1	DACR1	R/W		XXXXXXXX0 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007924 _H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
007925 _H	Input Capture 2	IPCP2	R		XXXXXXXX _B
007926 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007927 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007928 _H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
007929 _H	Input Capture 4	IPCP4	R		XXXXXXXX _B
00792A _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
00792B _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
00792C _H	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
00792D _H	Input Capture 6	IPCP6	R		XXXXXXXX _B
00792E _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
00792F _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
007930 _H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
007931 _H	Output Compare 0	OCCP0	R/W		XXXXXXXX _B
007932 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007933 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007934 _H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
007935 _H	Output Compare 2	OCCP2	R/W		XXXXXXXX _B
007936 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007937 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007938 _H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX _B
007939 _H	Output Compare 4	OCCP4	R/W		XXXXXXXX _B
00793A _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793B _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793C _H	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX _B
00793D _H	Output Compare 6	OCCP6	R/W		XXXXXXXX _B
00793E _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
00793F _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
007940 _H	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000 _B
007941 _H	Timer Data 0	TCDT0	R/W		00000000 _B
007942 _H	Timer Control Status 0	TCCSL0	R/W		00000000 _B
007943 _H	Timer Control Status 0	TCCSH0	R/W		0XXXXXXXX _B
007944 _H	Timer Data 1	TCDT1	R/W	Free-run Timer 1	00000000 _B
007945 _H	Timer Data 1	TCDT1	R/W		00000000 _B
007946 _H	Timer Control Status 1	TCCSL1	R/W		00000000 _B
007947 _H	Timer Control Status 1	TCCSH1	R/W		0XXXXXXXX _B

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List of Message Buffers (DLC Registers and Data Registers) (2)

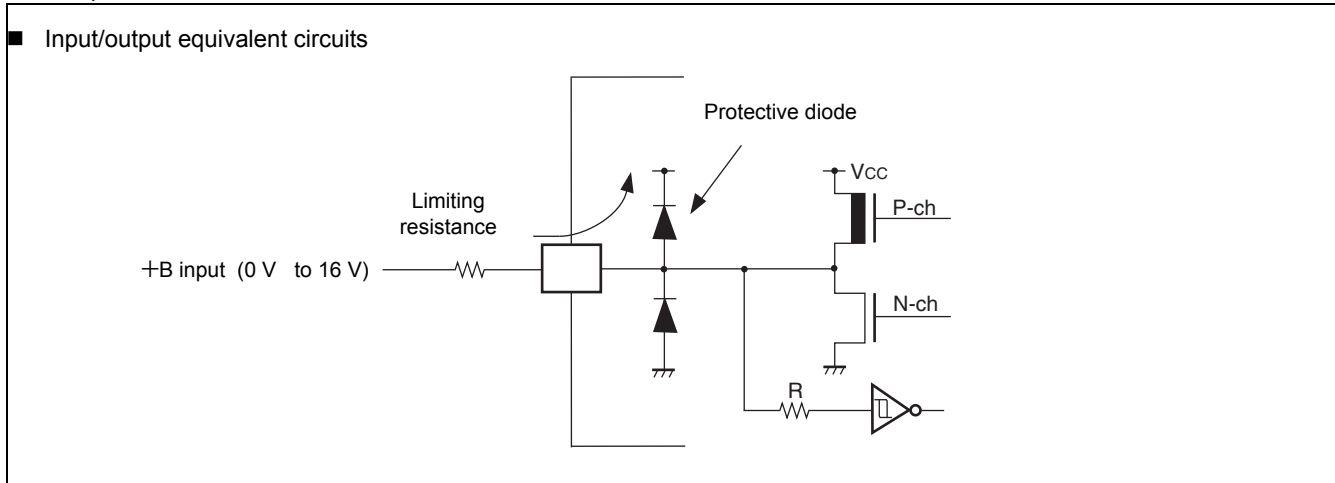
Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A80 _H to 007A87 _H	007C80 _H to 007C87 _H	Data Register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B
007A88 _H to 007A8F _H	007C88 _H to 007C8F _H	Data Register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
007A90 _H to 007A97 _H	007C90 _H to 007C97 _H	Data Register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
007A98 _H to 007A9F _H	007C98 _H to 007C9F _H	Data Register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
007AA0 _H to 007AA7 _H	007CA0 _H to 007CA7 _H	Data Register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
007AA8 _H to 007AAF _H	007CA8 _H to 007CAF _H	Data Register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
007AB0 _H to 007AB7 _H	007CB0 _H to 007CB7 _H	Data Register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
007AB8 _H to 007ABF _H	007CB8 _H to 007CBF _H	Data Register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
007AC0 _H to 007AC7 _H	007CC0 _H to 007CC7 _H	Data Register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
007AC8 _H to 007ACF _H	007CC8 _H to 007CCF _H	Data Register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
007AD0 _H to 007AD7 _H	007CD0 _H to 007CD7 _H	Data Register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
007AD8 _H to 007ADF _H	007CD8 _H to 007CDF _H	Data Register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
007AE0 _H to 007AE7 _H	007CE0 _H to 007CE7 _H	Data Register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
007AE8 _H to 007AEF _H	007CE8 _H to 007CEF _H	Data Register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B

List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007AF0 _H to 007AF7 _H	007CF0 _H to 007CF7 _H	Data Register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
007AF8 _H to 007AFF _H	007CF8 _H to 007CFF _H	Data Register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

(Continued)

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:



*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

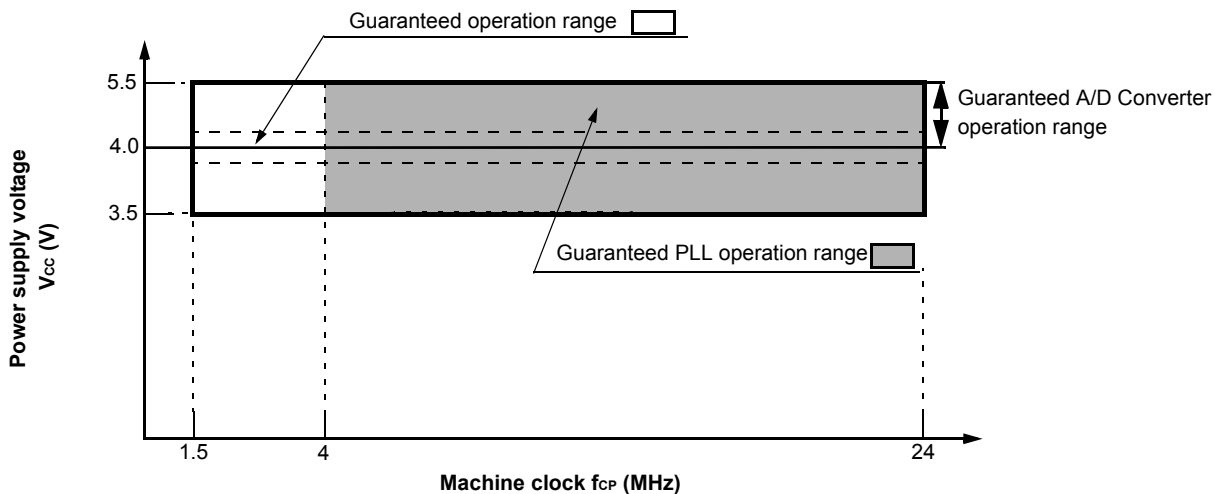
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($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

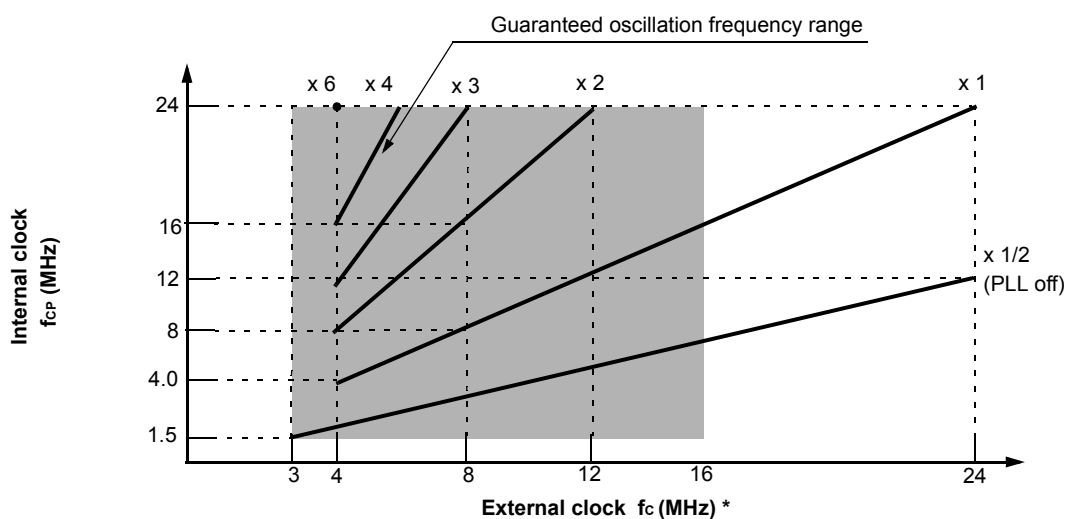
Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	—	$V_{CC} = 5.5\text{ V}$, $V_{SS} < V_I < V_{CC}$	-1	—	+1	μA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	—	25	50	100	$\text{k}\Omega$	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	$\text{k}\Omega$	Except Flash memory devices
Power supply current*	I_{CC}	V_{CC}	$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At normal operation.	—	55	70	mA	
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At writing Flash memory.	—	70	85	mA	Flash memory devices
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At erasing Flash memory.	—	75	90	mA	Flash memory devices
	I_{CCS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, In Sleep mode.	—	25	35	mA	
	I_{CTS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 2 MHz, In Main Timer mode	—	0.3	0.8	mA	
	$I_{CTSPLL6}$		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, In PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In sub operation $T_A = +25^{\circ}\text{C}$	—	70	140	μA	
	I_{CCLS}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In sub sleep $T_A = +25^{\circ}\text{C}$	—	20	50	μA	
	I_{CCT}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In watch mode $T_A = +25^{\circ}\text{C}$	—	10	35	μA	
	I_{CCH}		$V_{CC} = 5.0\text{ V}$, In Stop mode, $T_A = +25^{\circ}\text{C}$	—	7	25	μA	
Input capacitance	C_{IN}	Other than C, AV_{CC} , AV_{SS} , $AVRH$, $AVRL$, V_{CC} , V_{SS}	—	—	5	15	pF	

* : The power supply current is measured with an external clock.

Guaranteed PLL operation range



Guaranteed operation range of MB90340E series

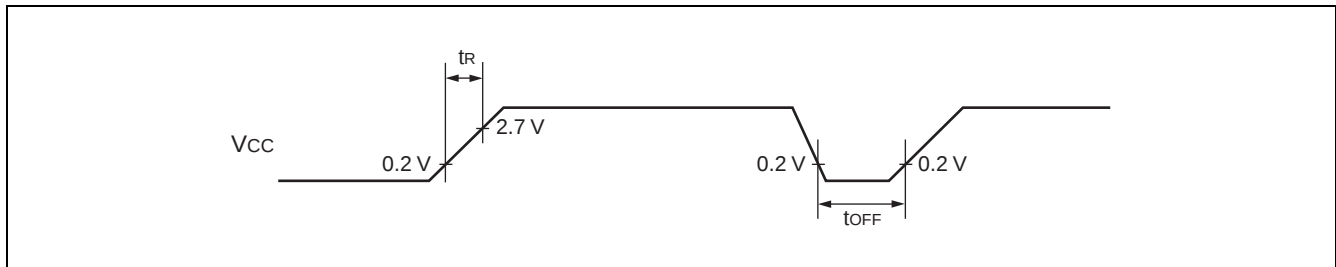


* : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

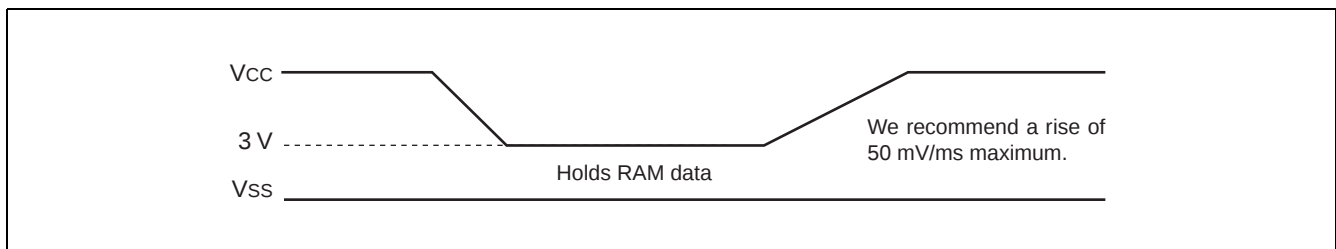
11.4.3 Power On Reset

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}	—	1	—	ms	Waiting time until power-on



Note: : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



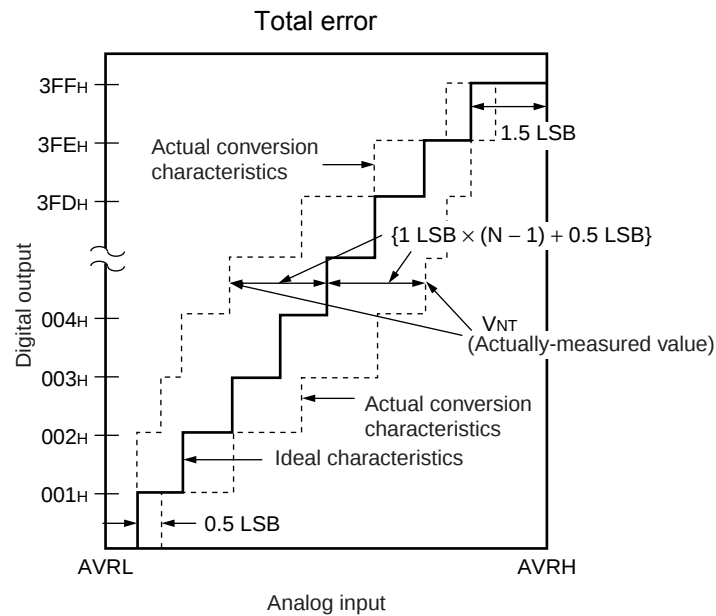
11.4.4 Clock Output Timing

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	$f_{CP} = 16\text{ MHz}$
				41.67	—	ns	$f_{CP} = 24\text{ MHz}$
CLK $\uparrow \rightarrow$ CLK $\downarrow$	t_{CHCL}	CLK	—	20	—	ns	$f_{CP} = 16\text{ MHz}$
				13	—	ns	$f_{CP} = 24\text{ MHz}$

11.6 Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by the A/D converter.
- Non linearity error : The deviation between the actual conversion characteristics and a line that joins the zero-transition line ("00 0000 0000" $\leftrightarrow$ "00 0000 0001") to the full-scale transition line ("11 1111 1110" $\leftrightarrow$ "11 1111 1111").
- Differential linearity error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} [\text{LSB}]$$

$$1 \text{ LSB (Ideal value)} = \frac{AVRH - AVRL}{1024} [\text{V}]$$

N : Value of the digital output from the A/D converter

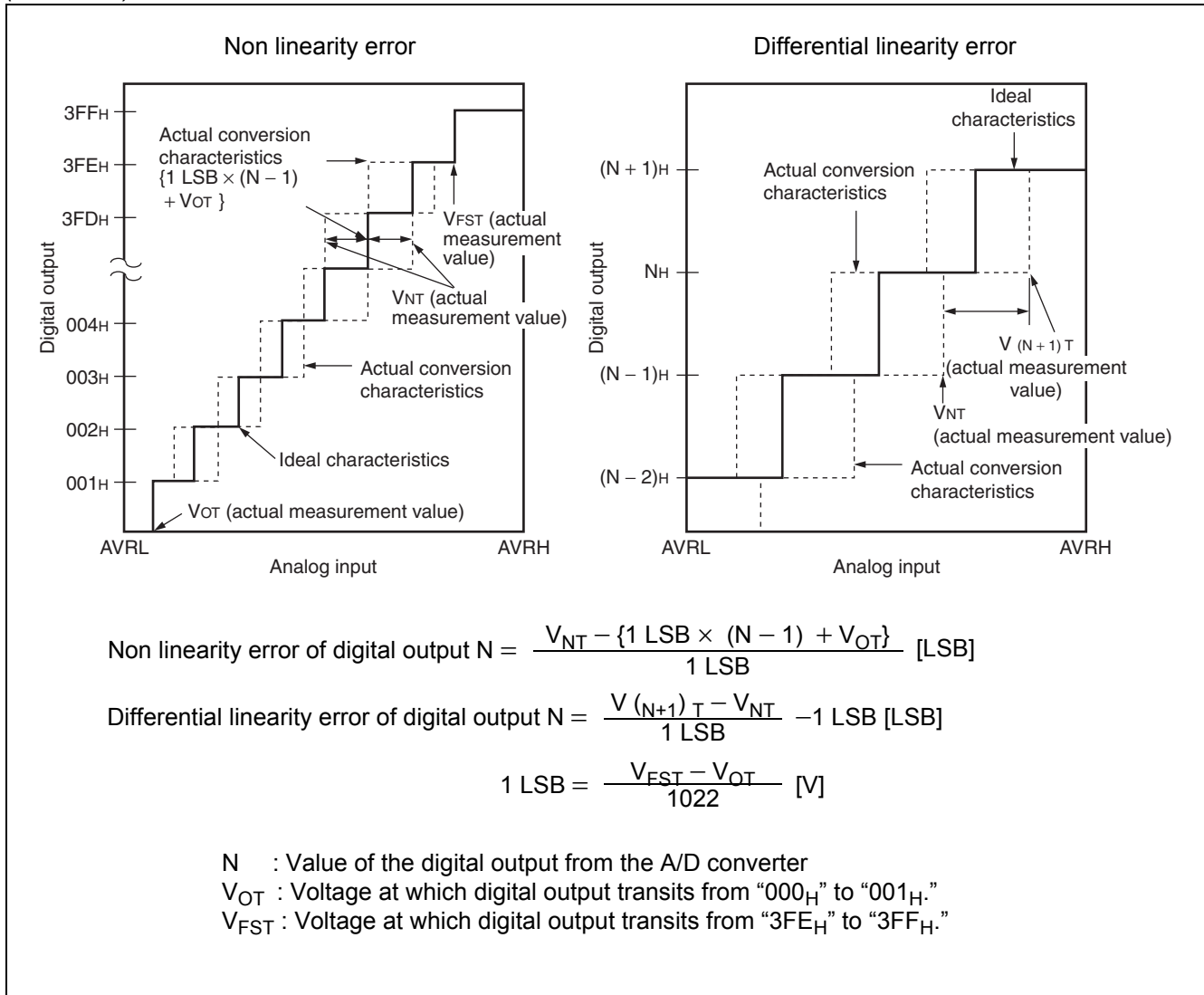
V_{OT} (Ideal value) = $AVRL + 0.5 \text{ LSB} [\text{V}]$

V_{FST} (Ideal value) = $AVRH - 1.5 \text{ LSB} [\text{V}]$

V_{NT} : A voltage at which the digital output transitions from $(N - 1)_H$ to N_H .

(Continued)

(Continued)



11.7 Notes on A/D Converter Section

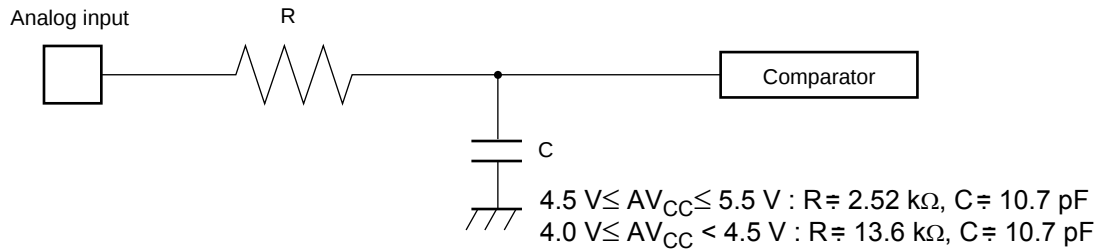
Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower (4.0 V ≤ AV_{CC} ≤ 5.5 V,
sampling period = 0.5 μs)

If an external capacitor is used, in consideration of the capacitive voltage dividing effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor be several thousand times greater than the capacitance of the internal capacitor.

If the output impedance of the external circuit is too high, a sampling period for an analog voltage may be insufficient.

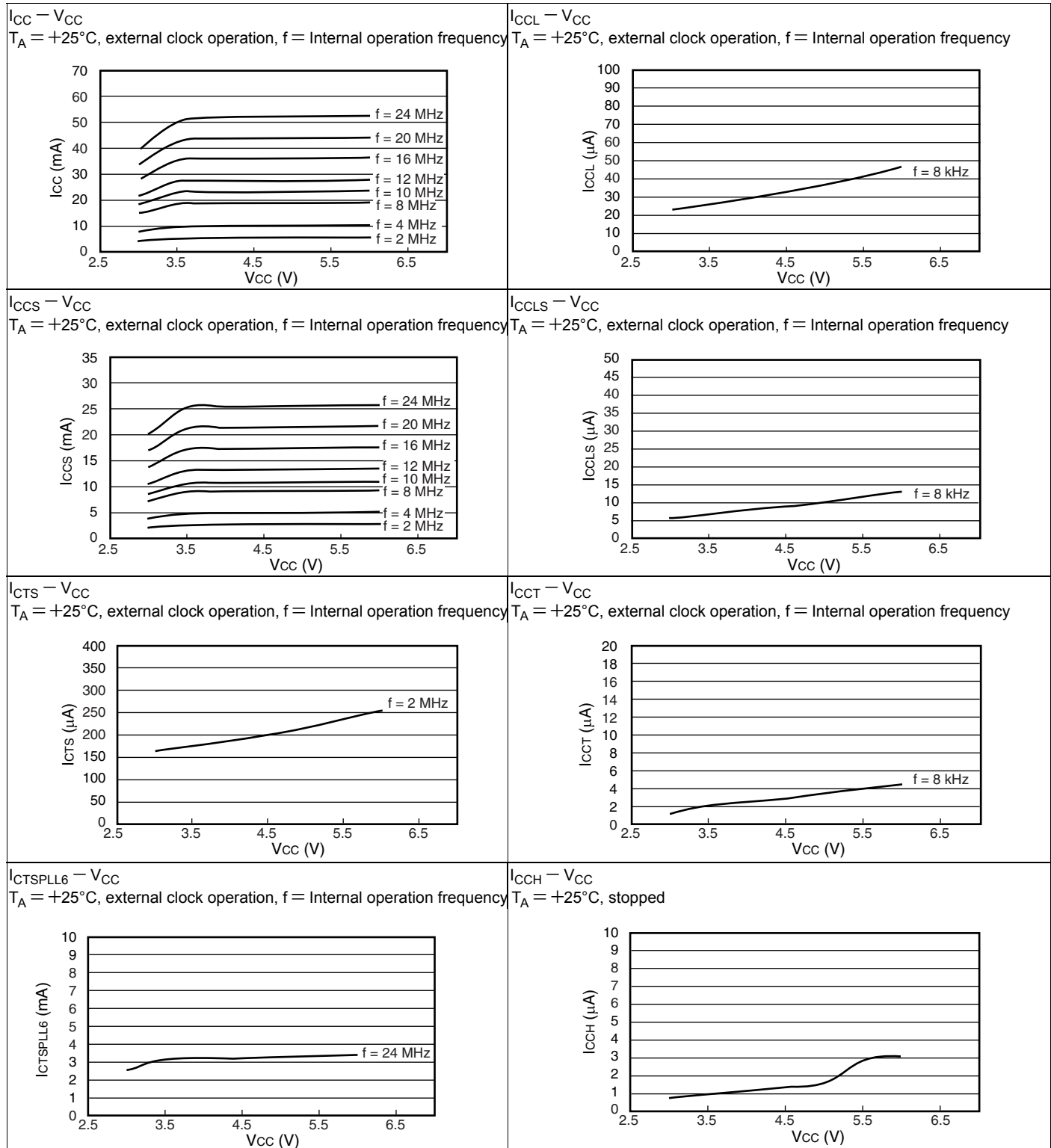
• Analog input circuit model



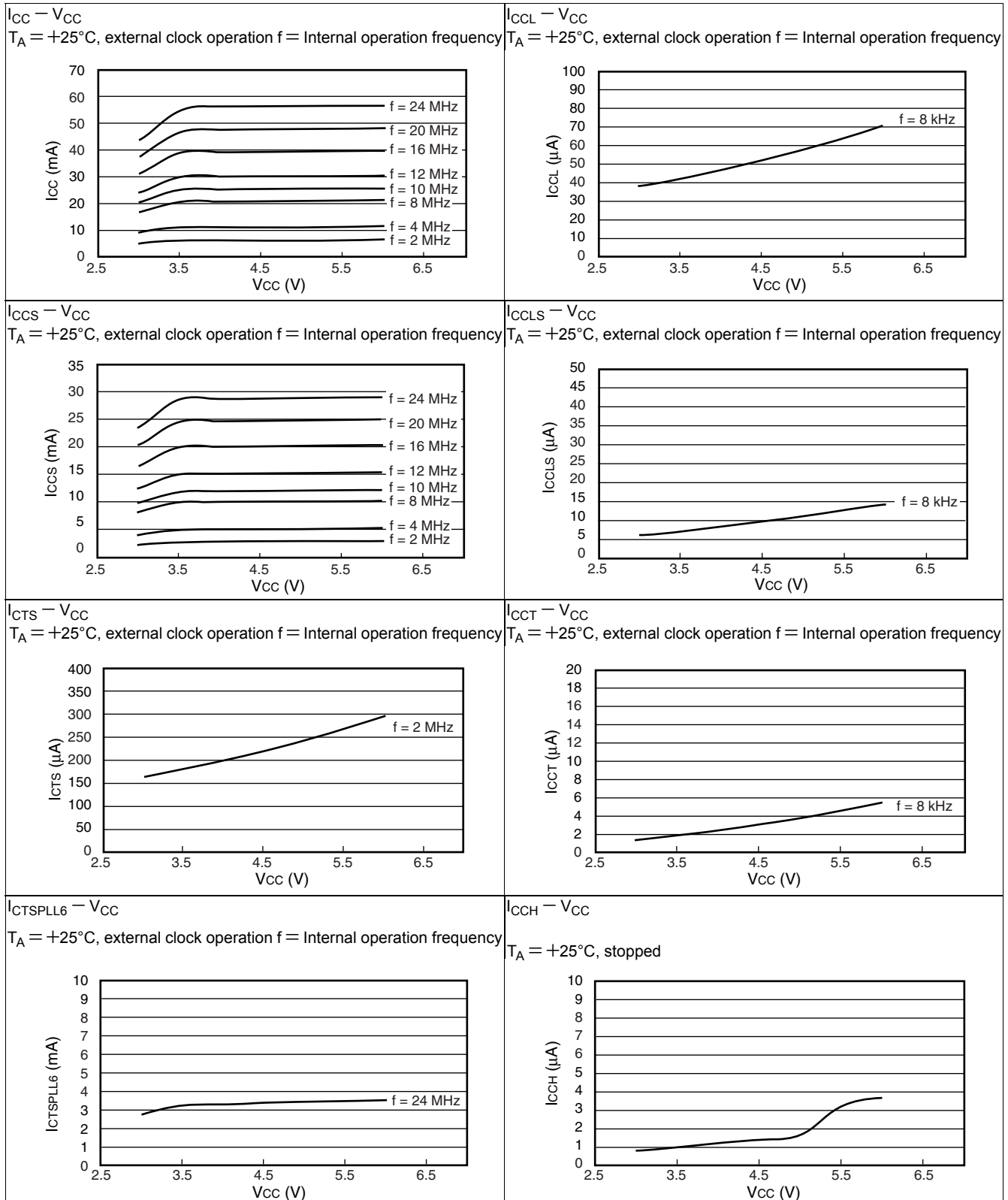
Note: : Use the values in the figure only as a guideline.

12. Example Characteristics

■ MB90F346E, MB90F346ES, MB90F346CE, MB90F346CES



■ MB90F349E, MB90F349ES, MB90F349CE, MB90F349CES



15. Major Changes

Spanision Publication Number: DS07-13747-4E

Page	Section	Change Results
—	—	Deleted the part numbers; MB90F343E(S), MB90F343CE(S)
51	Electrical Characteristics Absolute Maximum Ratings	Added “*6” in remark for “L” level maximum output current and “H” level maximum output current. Added “*7” in remark for “L” level average output current and “H” level average output current. Added “*8” in remark for “L” level average overall output current and “H” level average overall output current.
52		Added as follows. “*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.” “*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.” “*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.”

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90340E Series F2MC-16LX 16-bit Microcontroller Datasheet Document Number: 002-04498				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	08/23/2010	Migrated to Cypress and assigned document number 002-04498. No change to document contents or format.
*A	5221535	AKIH	05/04/2016	Updated to Cypress template