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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

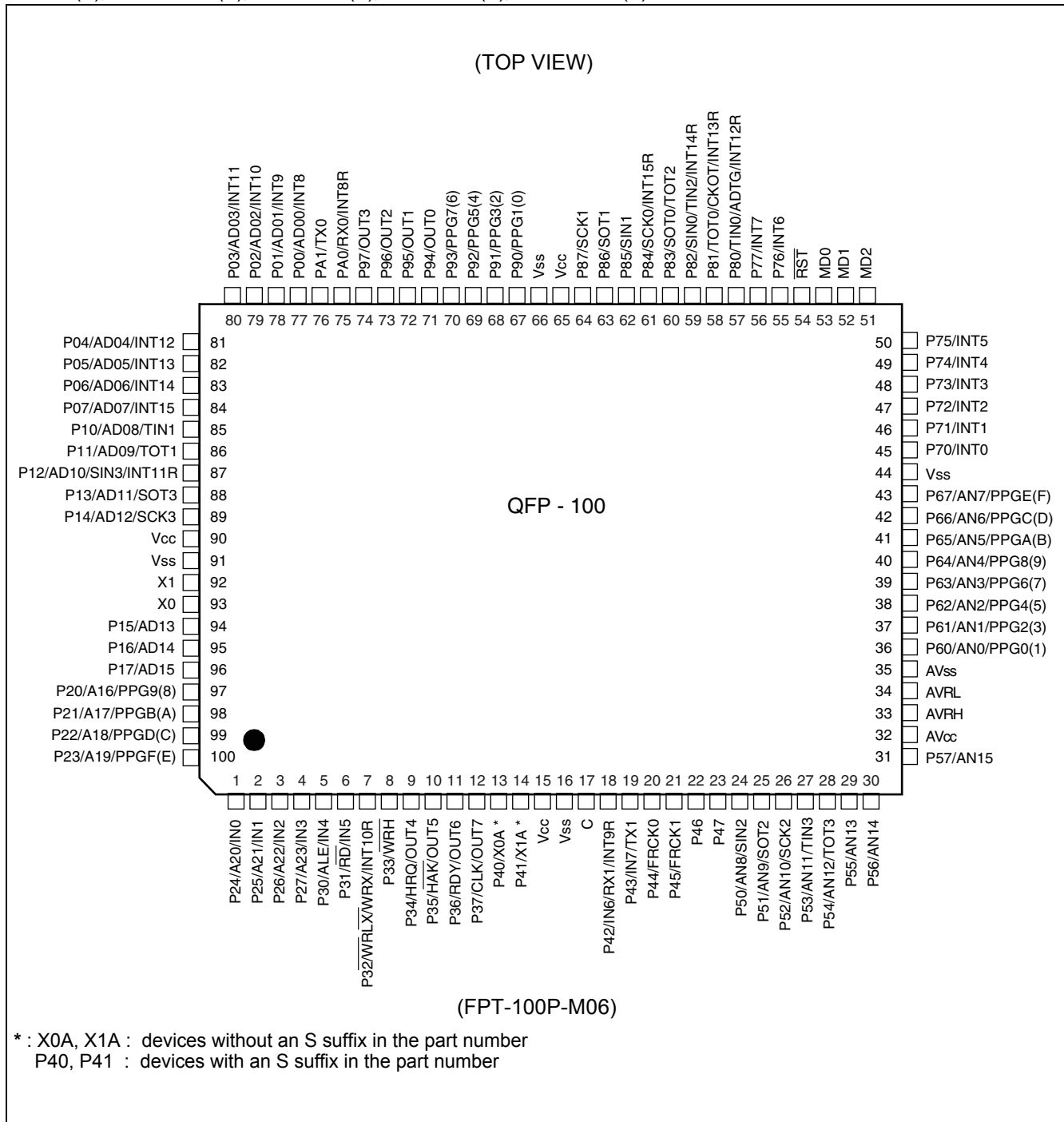
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-625e1

2. Pin Assignments

■ MB90341E(S), MB90342E(S), MB90F342E(S), MB90F345E(S), MB90346E(S), MB90F346E(S), MB90347E(S), MB90F347E(S), MB90348E(S), MB90349E(S), MB90F349E(S)



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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101)
		X0A, X1A	B	Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102)
15	13	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
16	14	V _{SS}	—	GND pin
17	15	C	K	This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 μF .
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture.
		RX1		RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only)
		INT9R		External interrupt request input pin

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV _{CC} .
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter
35	33	AV _{SS}	K	Analog GND pin for the A/D Converter
36 to 43	34 to 41	P60 to P67	I	General purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
44	42	V _{SS}	—	GND pin
45 to 50	43 to 48	P70 to P75	I	General purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT0 to INT5		External interrupt request input pins
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	RST	E	Reset input pin
55, 56	53, 54	P76, P77	I	General purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT6, INT7		External interrupt request input pins
57	55	P80	F	General purpose I/O pin.
		TIN0		Event input pin for the reload timer
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin
58	56	P81	F	General purpose I/O pin.
		TOT0		Output pin for the reload timer
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin
59	57	P82	M	General purpose I/O pin.
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer
		INT14R		External interrupt request input pin
60	58	P83	F	General purpose I/O pin.
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
86	84	P11	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer
87	85	P12	N	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin
88	86	P13	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
89	87	P14	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3
90	88	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
91	89	V _{SS}	—	GND pin
92	90	X1	A	Main clock output pin
93	91	X0		Main clock input pin
94	92	P15	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
95	93	P16	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.

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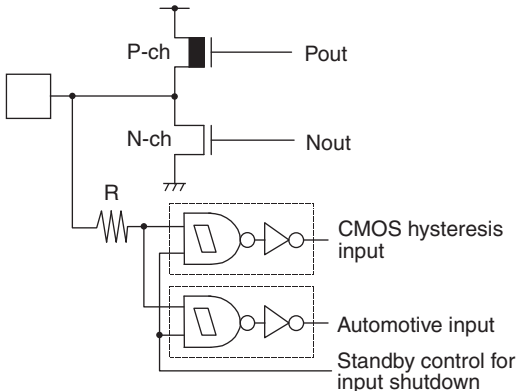
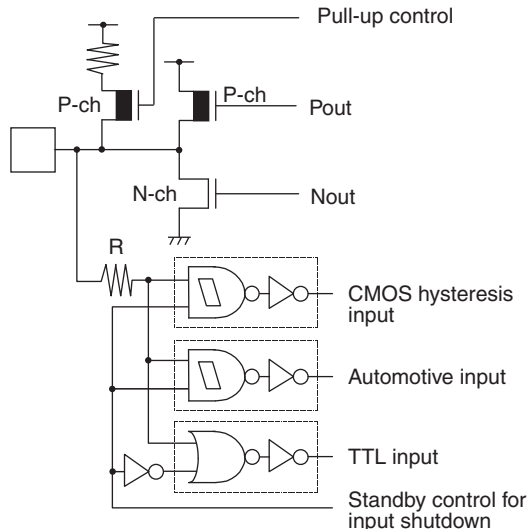
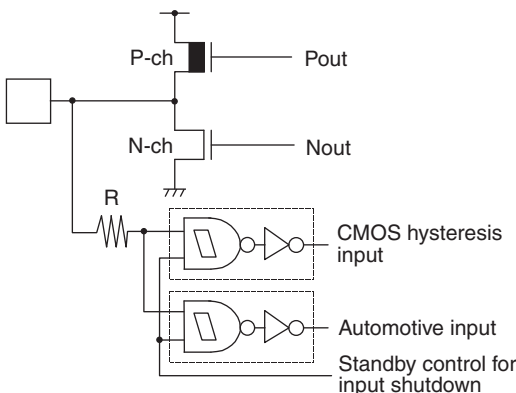
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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
96	94	P17	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
97 to 100	95 to 98	P20 to P23	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9, PPGB, PP GD, PPGF		Output pins for PPGs

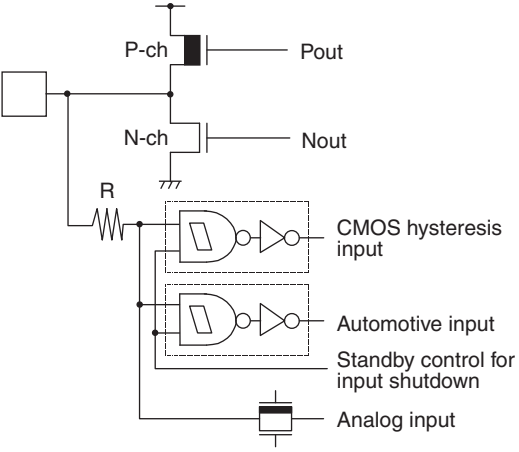
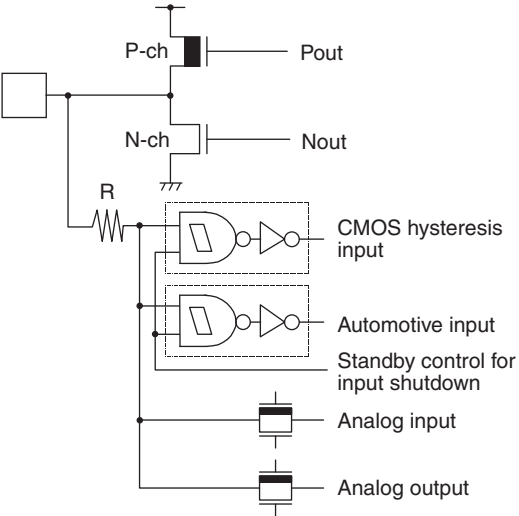
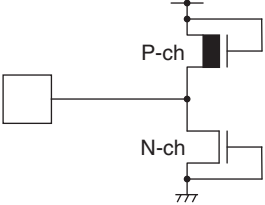
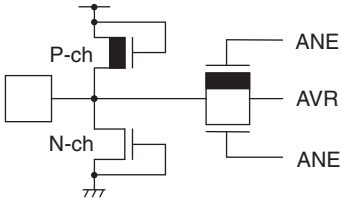
1 : FPT-100P-M06

2 : FPT-100P-M20

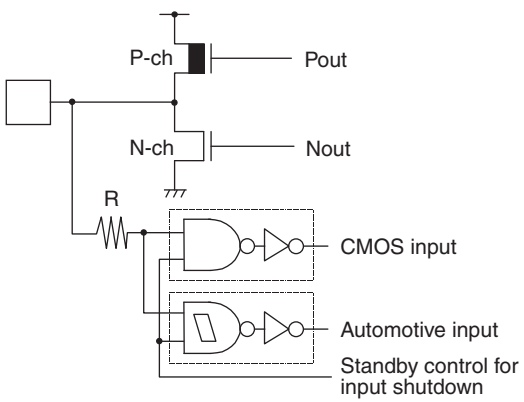
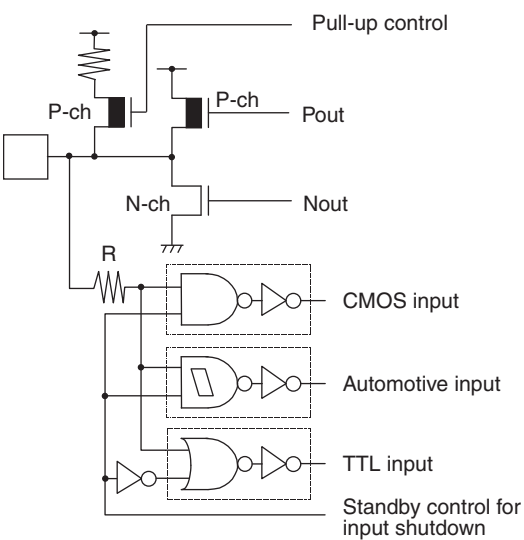
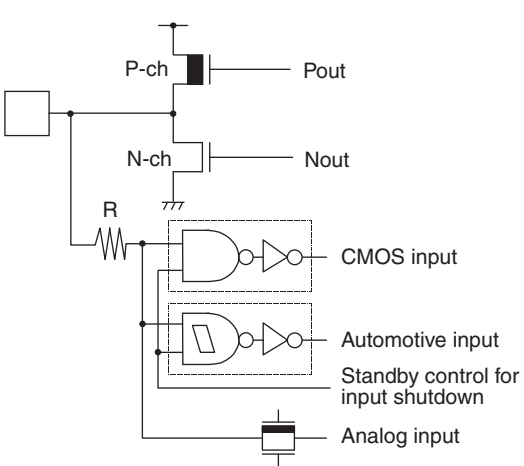
3 : For I/O circuit type, refer to "I/O Circuit Type".

Type	Circuit	Remarks
F		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
G		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) ■ Programmable pull-up resistor: 50 kΩ approx.
H		■ CMOS level output ($I_{OL} = 3 \text{ mA}$, $I_{OH} = -3 \text{ mA}$) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)

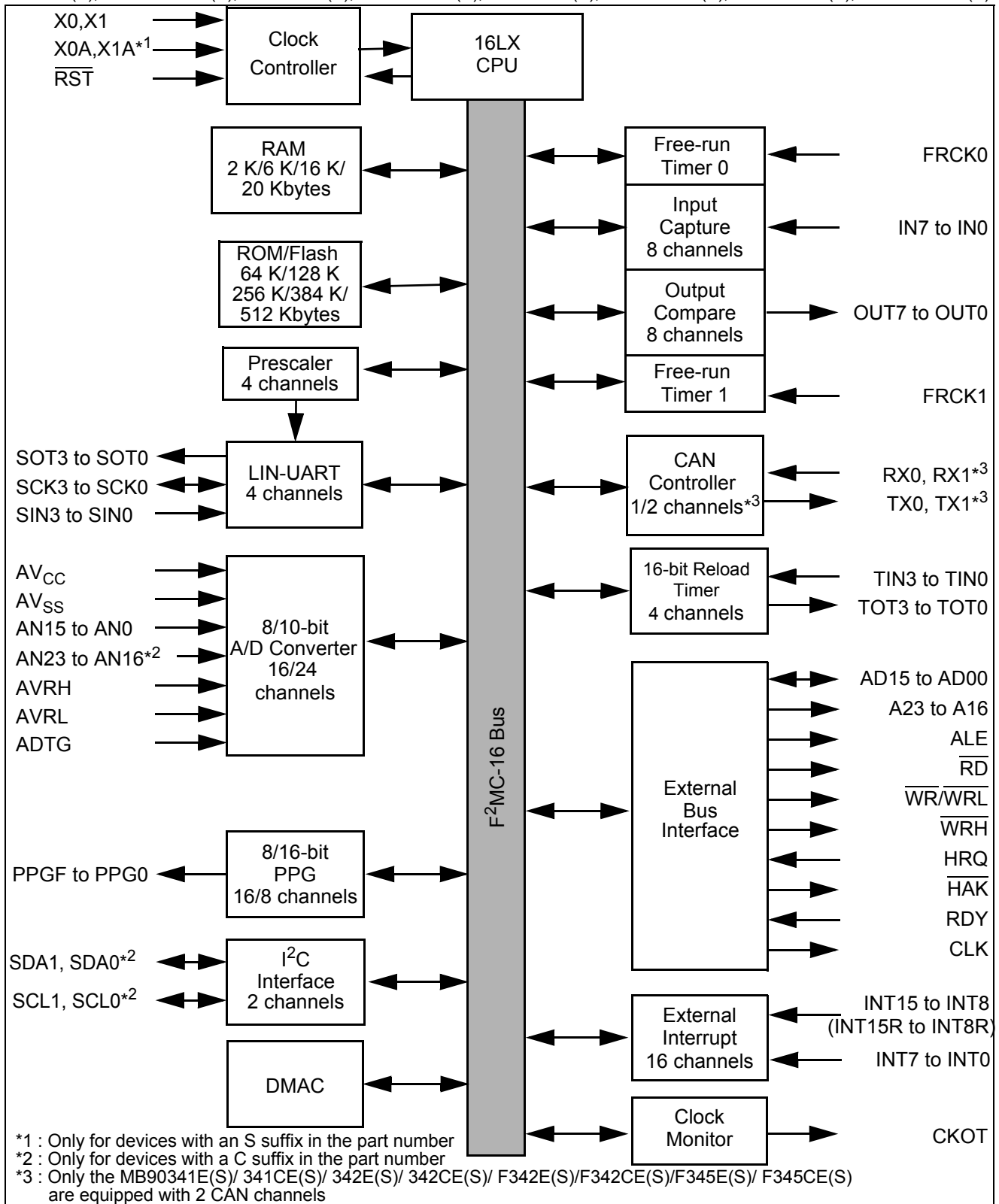
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Type	Circuit	Remarks
I		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
J		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ D/A analog output ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
K		Power supply input protection circuit
L		■ A/D converter reference voltage power supply input pin, with the protection circuit ■ Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH

(Continued)

Type	Circuit	Remarks
M		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
N		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) Programmable pull-up resistor: 50 kΩ approx
O		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input

■ MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)



Address	Register	Abbreviation	Access	Resource name	Initial value
000040 _H	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	0X000XX1 _B
000041 _H	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		0X000001 _B
000042 _H	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		000000X0 _B
000043 _H	Reserved				
000044 _H	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	0X000XX1 _B
000045 _H	PPG B Operation Mode Control Register	PPGCB	W,R/W		0X000001 _B
000046 _H	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		000000X0 _B
000047 _H	Reserved				
000048 _H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	0X000XX1 _B
000049 _H	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001 _B
00004A _H	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		000000X0 _B
00004B _H	Reserved				
00004C _H	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	0X000XX1 _B
00004D _H	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001 _B
00004E _H	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		000000X0 _B
00004F _H	Reserved				
000050 _H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000 _B
000051 _H	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XX _B
000052 _H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000 _B
000053 _H	Input Capture Edge 2/3	ICE23	R		XXXXXXXX _B
000054 _H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000 _B
000055 _H	Input Capture Edge 4/5	ICE45	R		XXXXXXXX _B
000056 _H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000 _B
000057 _H	Input Capture Edge 6/7	ICE67	R/W, R		XXX000XX _B
000058 _H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00 _B
000059 _H	Output Compare Control Status 1	OCS1	R/W		0XX00000 _B
00005A _H	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00 _B
00005B _H	Output Compare Control Status 3	OCS3	R/W		0XX00000 _B
00005C _H	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00 _B
00005D _H	Output Compare Control Status 5	OCS5	R/W		0XX00000 _B
00005E _H	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00 _B
00005F _H	Output Compare Control Status 7	OCS7	R/W		0XX00000 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0000C4 _H , 0000C5 _H	Reserved				
0000C6 _H	External Interrupt Enable 0	ENIR0	R/W	External Interrupt 0	00000000 _B
0000C7 _H	External Interrupt Source 0	EIRR0	R/W		XXXXXXXX _B
0000C8 _H	External Interrupt Level Setting 0	ELVR0	R/W		00000000 _B
0000C9 _H	External Interrupt Level Setting 0	ELVR0	R/W		00000000 _B
0000CA _H	External Interrupt Enable 1	ENIR1	R/W	External Interrupt 1	00000000 _B
0000CB _H	External Interrupt Source 1	EIRR1	R/W		XXXXXXXX _B
0000CC _H	External Interrupt Level Setting 1	ELVR1	R/W		00000000 _B
0000CD _H	External Interrupt Level Setting 1	ELVR1	R/W		00000000 _B
0000CE _H	External Interrupt Source Select	EISSR	R/W		00000000 _B
0000CF _H	PLL/Sub clock Control Register	PSCCR	W	PLL	XXXX0000 _B
0000D0 _H	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	XXXXXXXX _B
0000D1 _H	DMA Buffer Address Pointer M Register	BAPM	R/W		XXXXXXXX _B
0000D2 _H	DMA Buffer Address Pointer H Register	BAPH	R/W		XXXXXXXX _B
0000D3 _H	DMA Control Register	DMACS	R/W		XXXXXXXX _B
0000D4 _H	I/O Register Address Pointer L Register	IOAL	R/W		XXXXXXXX _B
0000D5 _H	I/O Register Address Pointer H Register	IOAH	R/W		XXXXXXXX _B
0000D6 _H	Data Counter L Register	DCTL	R/W		XXXXXXXX _B
0000D7 _H	Data Counter H Register	DCTH	R/W		XXXXXXXX _B
0000D8 _H	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000 _B
0000D9 _H	Serial Control Register 2	SCR2	W,R/W		00000000 _B
0000DA _H	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000 _B
0000DB _H	Serial Status Register 2	SSR2	R,R/W		00001000 _B
0000DC _H	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XX _B
0000DD _H	Extended Status Control Register 2	ESCR2	R/W		00000100 _B
0000DE _H	Baud Rate Generator Register 20	BGR20	R/W		00000000 _B
0000DF _H	Baud Rate Generator Register 21	BGR21	R/W		00000000 _B
0000E0 _H to 0000EF _H	Reserved for CAN Controller 2. Refer to “CAN Controllers”				
0000F0 _H to 0000FF _H	External				

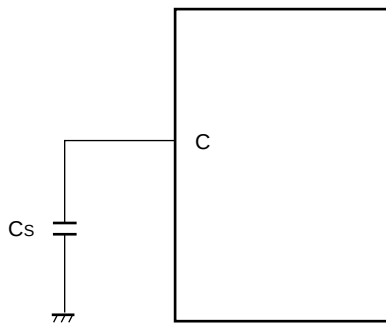
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11.2 Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	μF	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.
Operating temperature	T_A	-40	—	+105	$^{\circ}\text{C}$	

C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

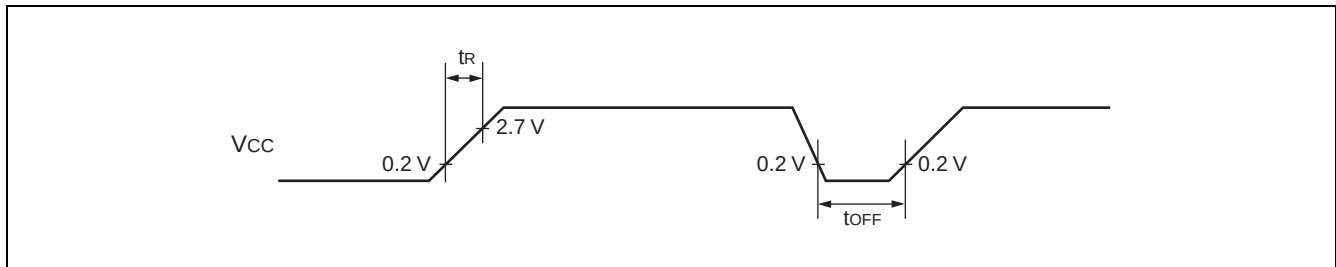
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

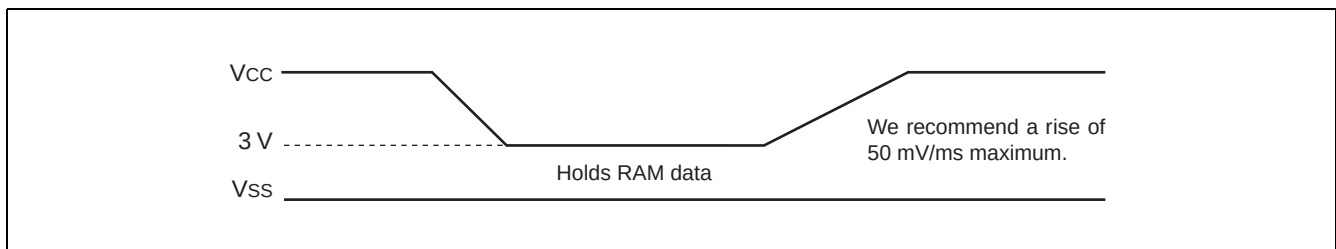
11.4.3 Power On Reset

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}	—	1	—	ms	Waiting time until power-on



Note: : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



11.4.4 Clock Output Timing

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

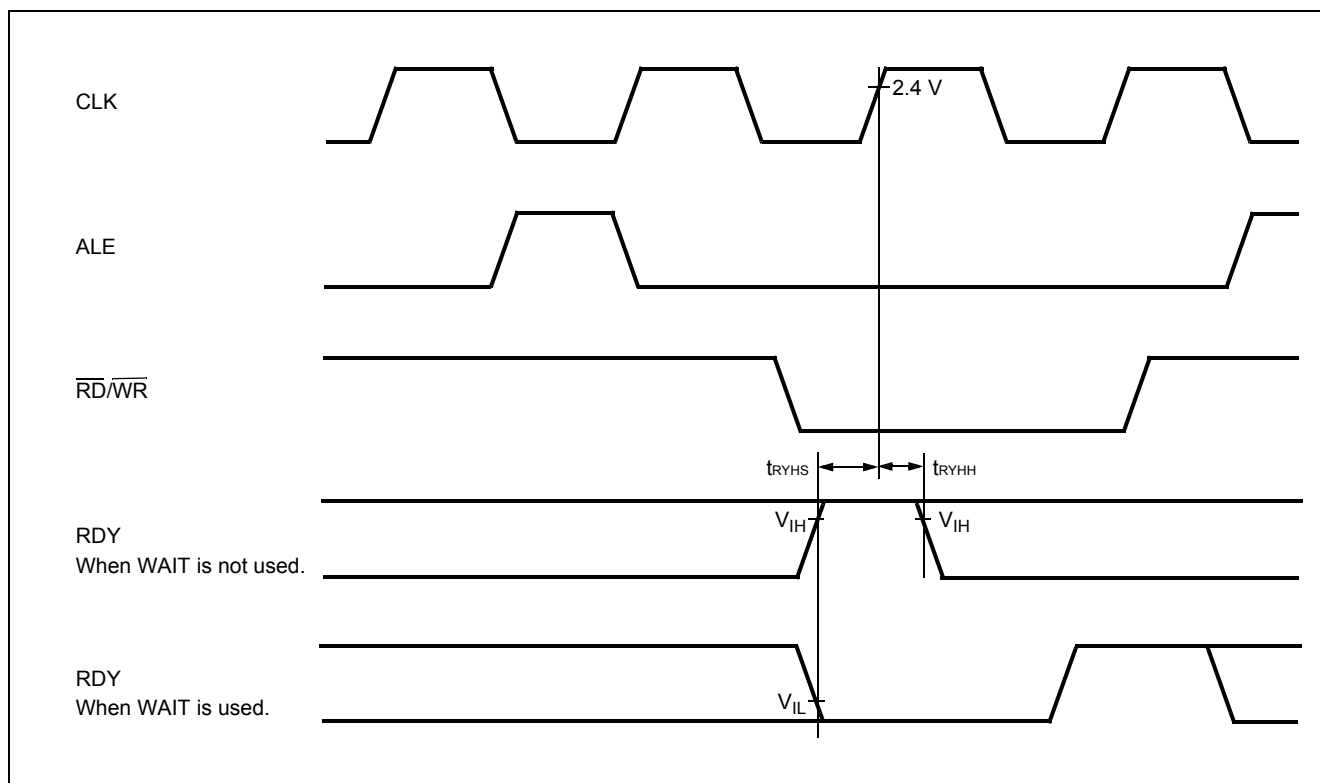
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	$f_{CP} = 16\text{ MHz}$
				41.67	—	ns	$f_{CP} = 24\text{ MHz}$
CLK $\uparrow \rightarrow$ CLK $\downarrow$	t_{CHCL}	CLK	—	20	—	ns	$f_{CP} = 16\text{ MHz}$
				13	—	ns	$f_{CP} = 24\text{ MHz}$

11.4.7 Ready Input Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	$f_{CP} = 16\text{ MHz}$
				32	—	ns	$f_{CP} = 24\text{ MHz}$
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note: : If the RDY setup time is insufficient, use the auto-ready function.

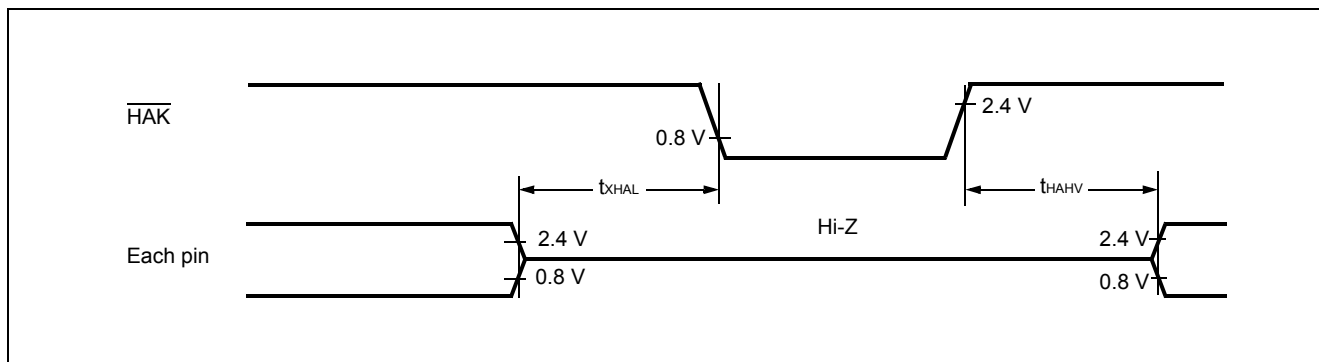


11.4.8 Hold Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Pin floating $\rightarrow \overline{\text{HAK}} \downarrow$ time	t_{XHAL}	$\overline{\text{HAK}}$	—	30	t_{CP}	ns
$\overline{\text{HAK}} \uparrow$ time $\rightarrow$ Pin valid time	t_{HAHV}	$\overline{\text{HAK}}$	—	t_{CP}	$2 t_{CP}$	ns

Note: : There is more than 1 cycle from when HRQ reads in until the $\overline{\text{HAK}}$ is changed.



11.4.9 LIN-UART0/1/2/3

■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

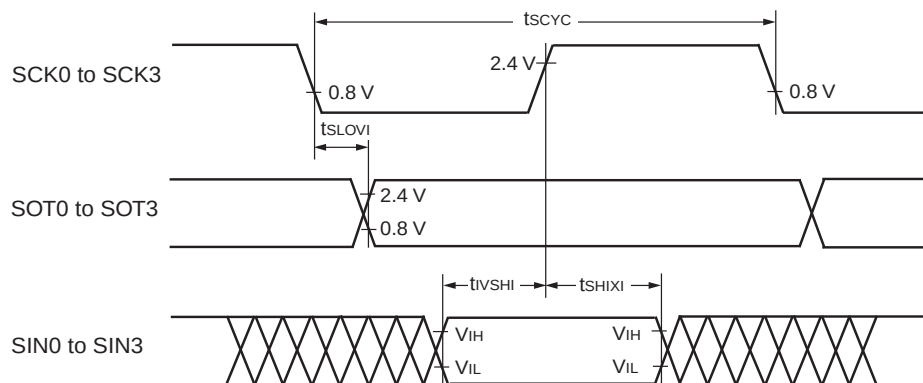
($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock "L" pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$3 t_{CP} - t_R$	—	ns
Serial clock "H" pulse width	t_{SLSH}	SCK0 to SCK3		$t_{CP} + 10$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	$2 t_{CP} + 60$	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SIN0 to SIN3		$t_{CP} + 30$	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

Note:

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

• Internal Shift Clock Mode



11.4.13 I²C Timing

(T_A = -40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V)

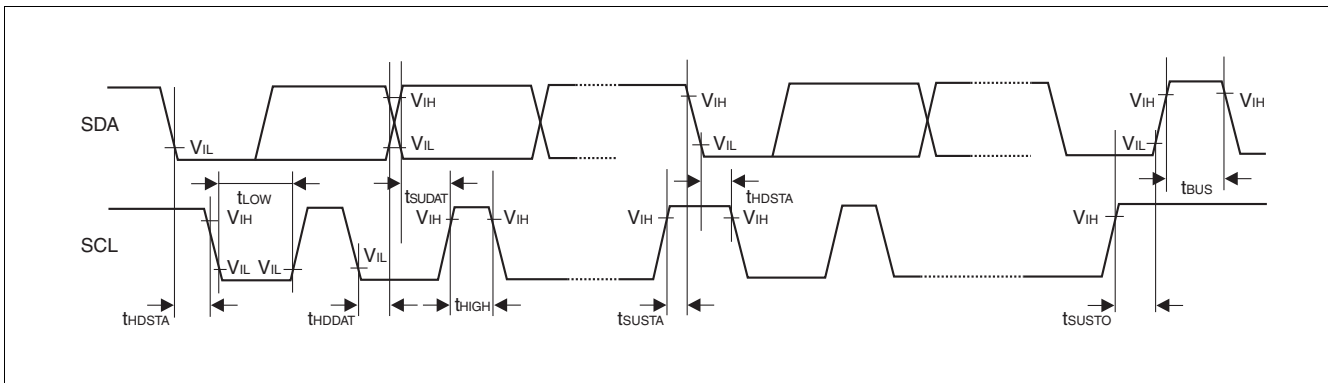
Parameter	Symbol	Condition	Standard-mode		Fast-mode* ¹		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	R = 1.7 kΩ ₂ C = 50 pF* ²	0	100	0	400	kHz
Hold time (repeated) START condition SDA ↓ → SCL ↓	t _{HDSTA}		4.0	—	0.6	—	μs
"L" width of the SCL clock	t _{LOW}		4.7	—	1.3	—	μs
"H" width of the SCL clock	t _{HIGH}		4.0	—	0.6	—	μs
Set-up time (repeated) START condition SCL ↑ → SDA ↓	t _{SUSTA}		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓ ↑	t _{HDDAT}		0	3.45* ³	0	0.9* ⁴	μs
Data set-up time SDA ↓ ↑ → SCL ↑	t _{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t _{SUSTO}		4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t _{BUS}		4.7	—	1.3	—	μs

*1: For use at over 100 kHz, set the machine clock to at least 6 MHz.

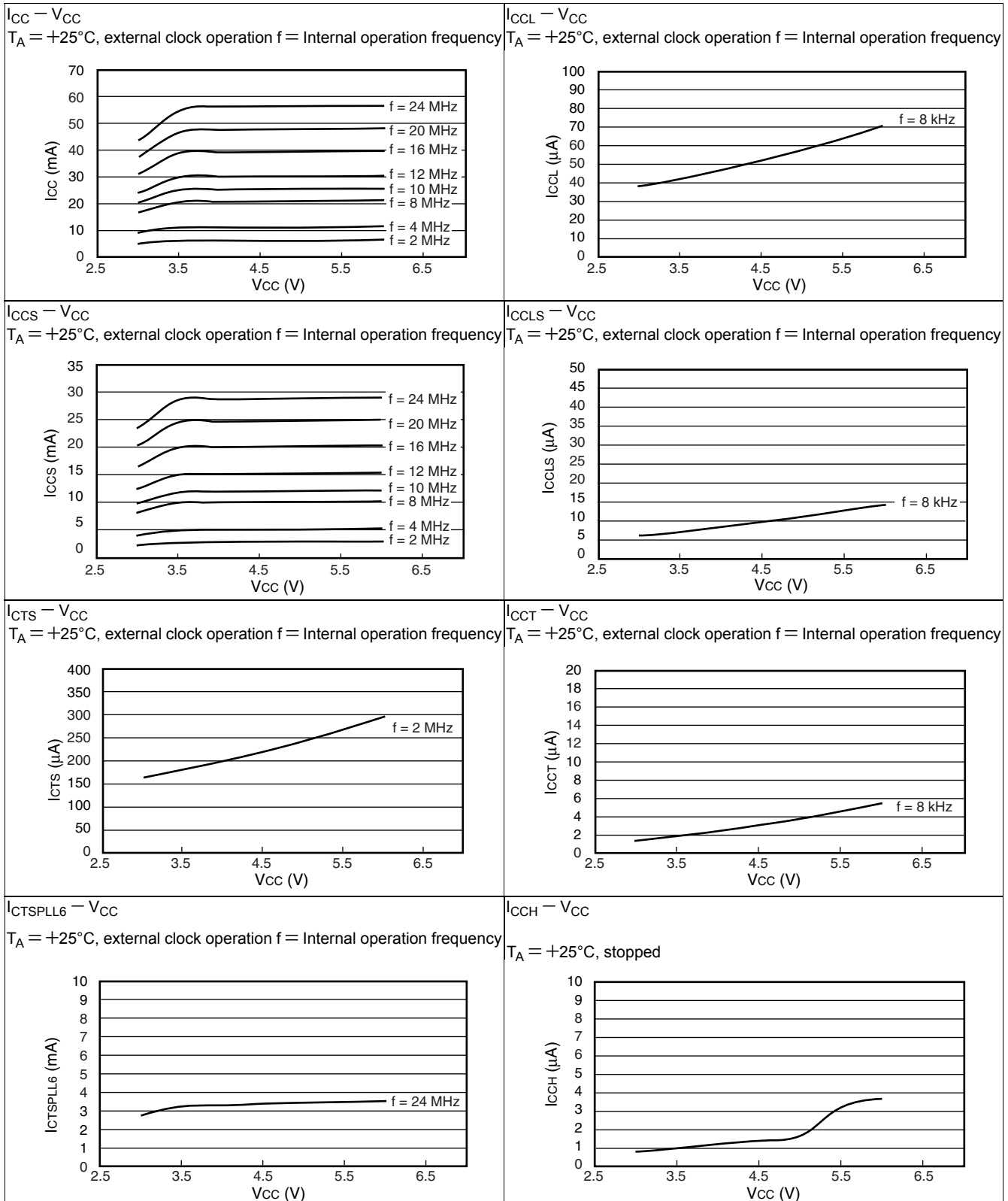
*2: R, C: Pull-up resistor and load capacitor of the SCL and SDA lines.

*3: The maximum t_{HDDAT} meets the requirement that it does not extend the "L" width (t_{LOW}) of the SCL signal.

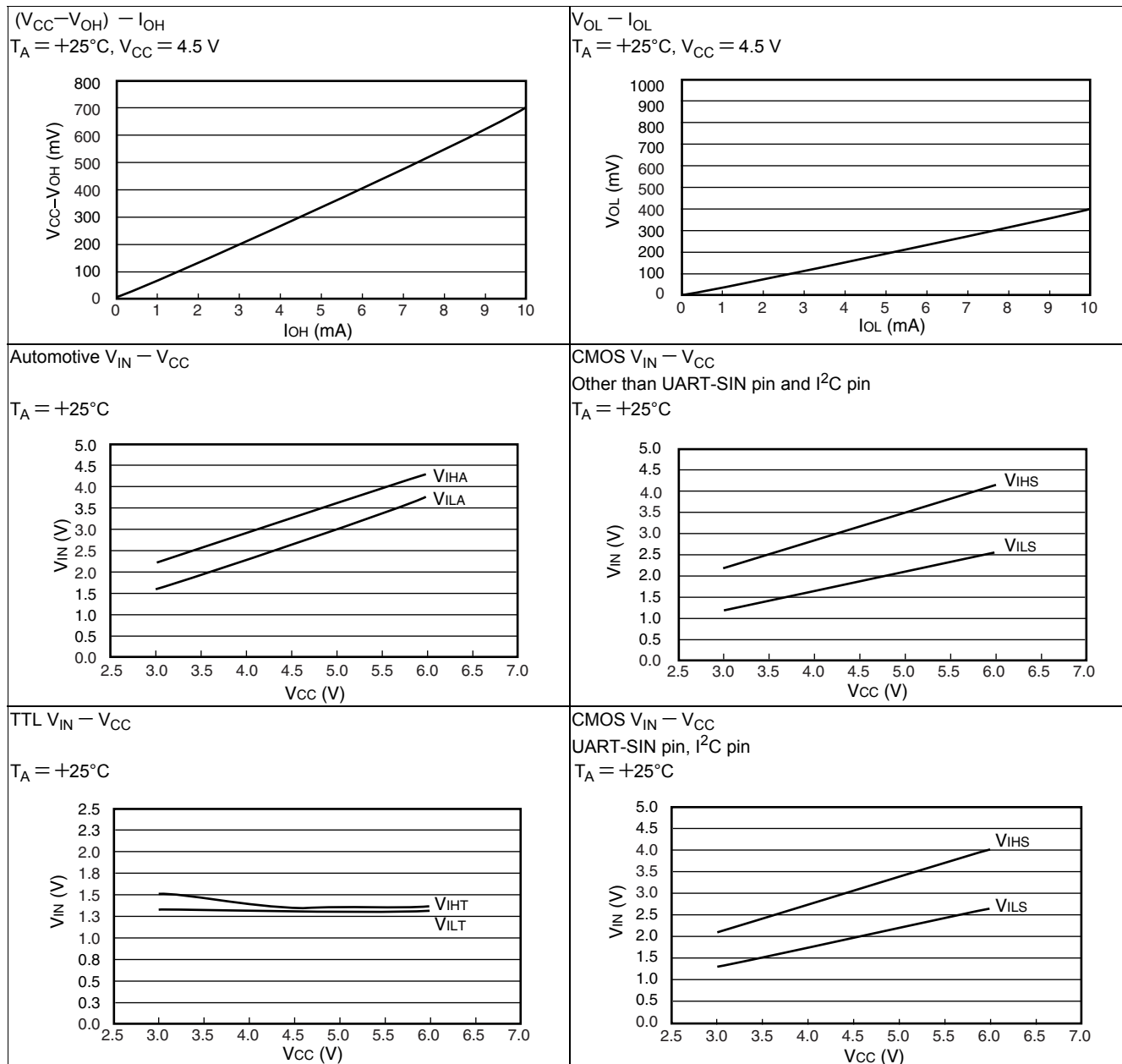
*4: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.



■ MB90F349E, MB90F349ES, MB90F349CE, MB90F349CES



■ I/O characteristics



(Continued)

Part number	Package	Remarks
MB90346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90346ESPF		
MB90346CEPF		
MB90346CESPF		
MB90346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90346ESPMC		
MB90346CEPMC		
MB90346CESPMC		
MB90347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90347ESPF		
MB90347CEPF		
MB90347CESPF		
MB90347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90347ESPMC		
MB90347CEPMC		
MB90347CESPMC		
MB90348EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90348ESPF		
MB90348CEPF		
MB90348CESPF		
MB90348EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90348ESPMC		
MB90348CEPMC		
MB90348CESPMC		
MB90349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90349ESPF		
MB90349CEPF		
MB90349CESPF		
MB90349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90349ESPMC		
MB90349CEPMC		
MB90349CESPMC		
MB90V340E-101CR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation
MB90V340E-102CR		