Infineon Technologies - MB90347ESPMC-GS-662E1 Datasheet

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What is "Embedded - Microcontrollers"?

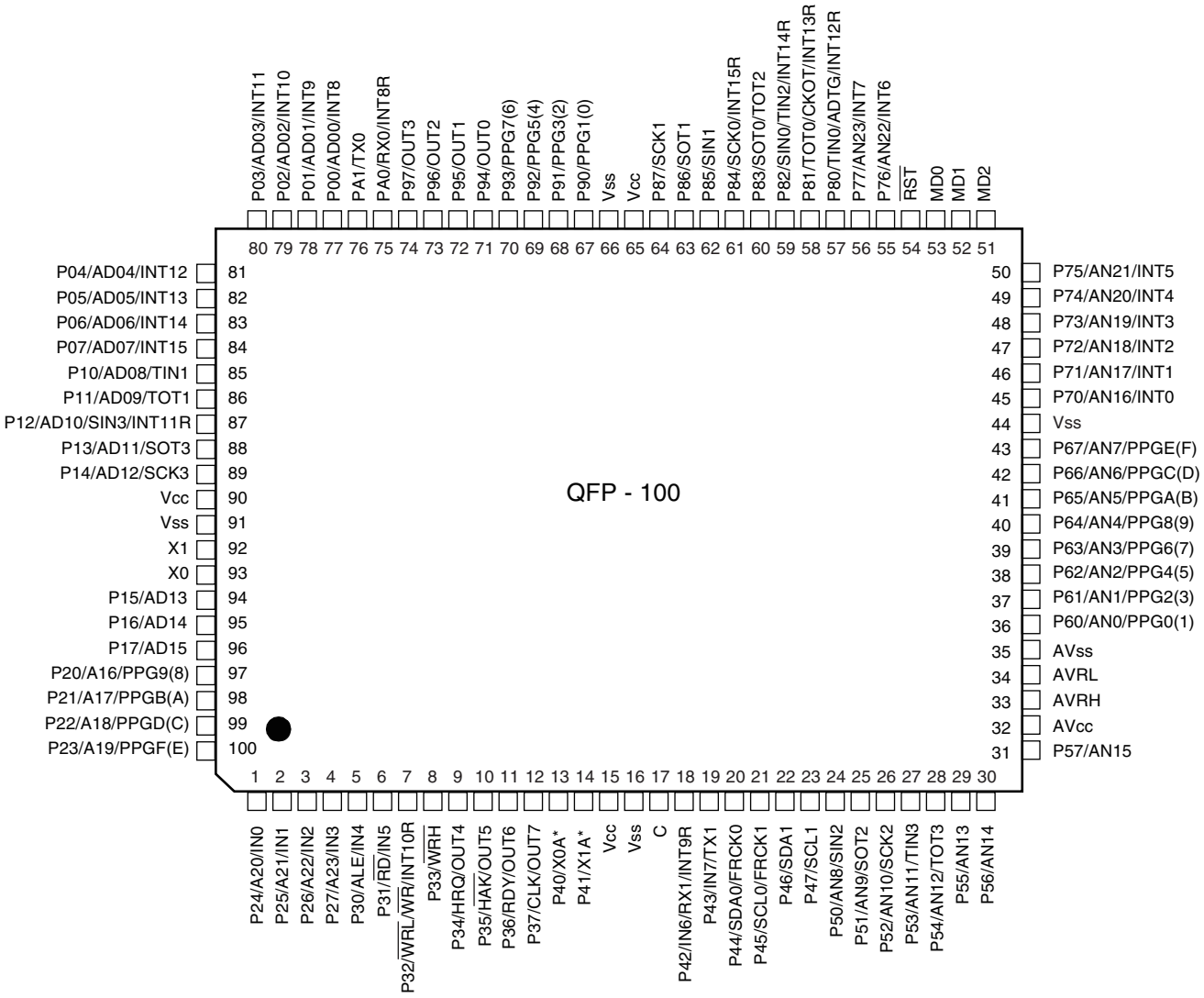
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-662e1

■ MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)

(TOP VIEW)



(FPT-100P-M06)

* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

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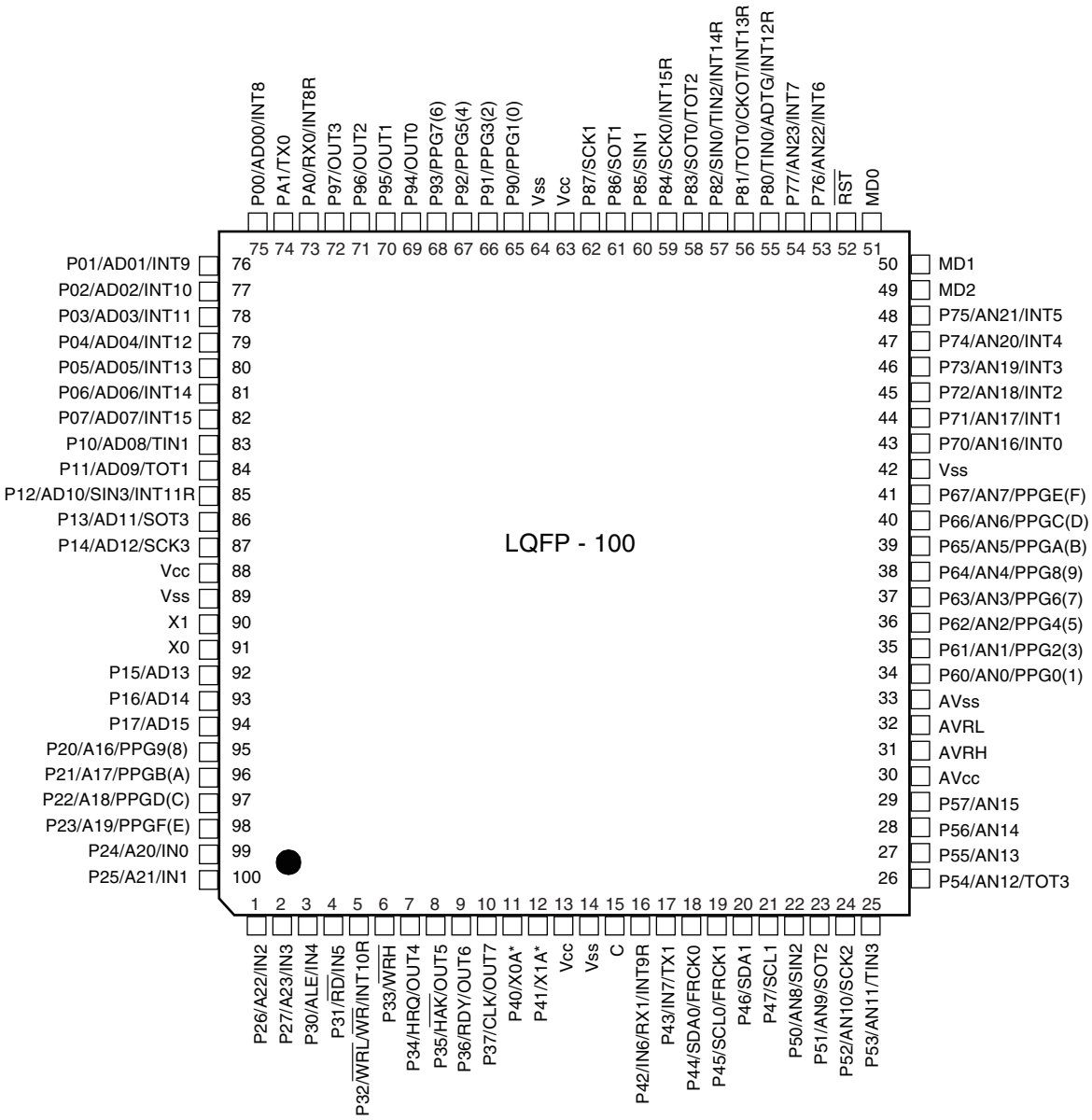
(TOP VIEW)



(FPT-100P-M20)

* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

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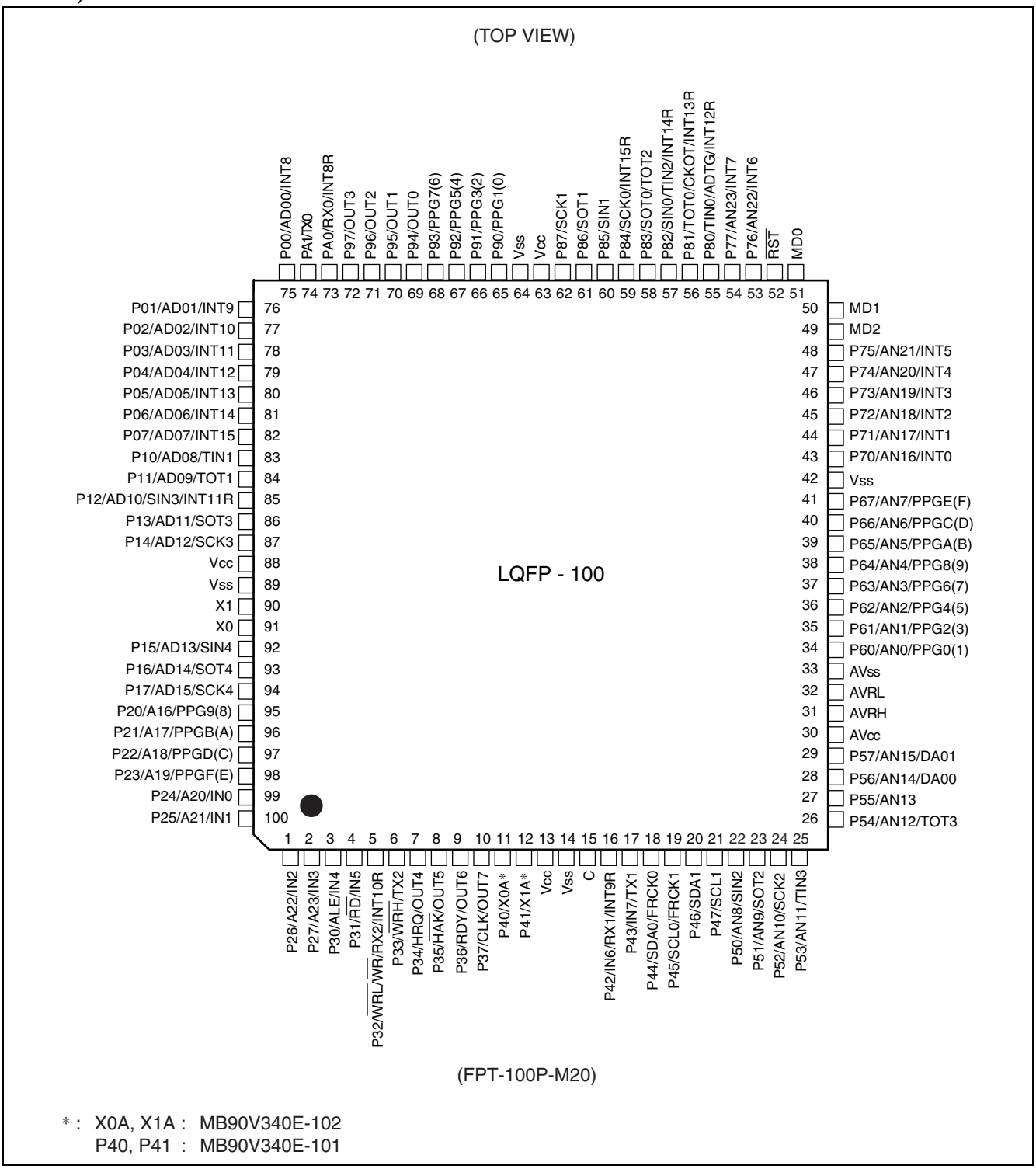
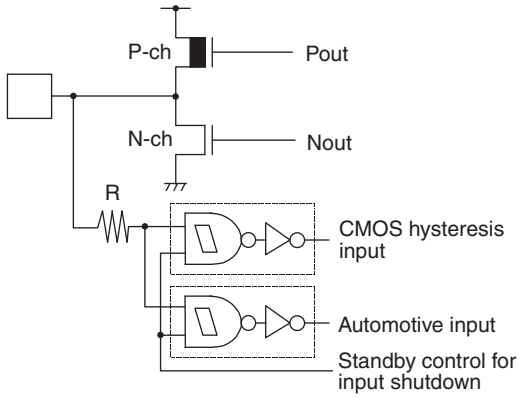
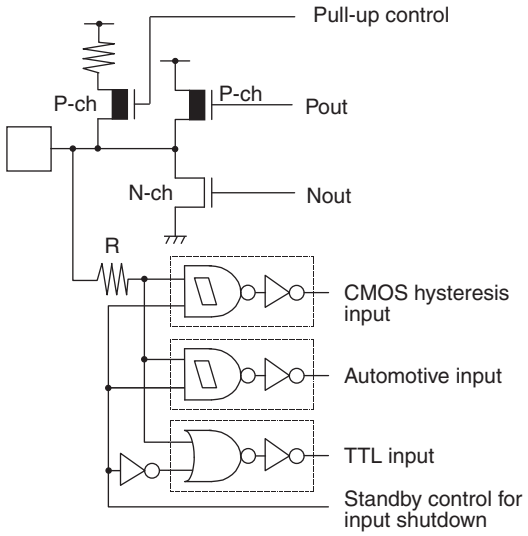
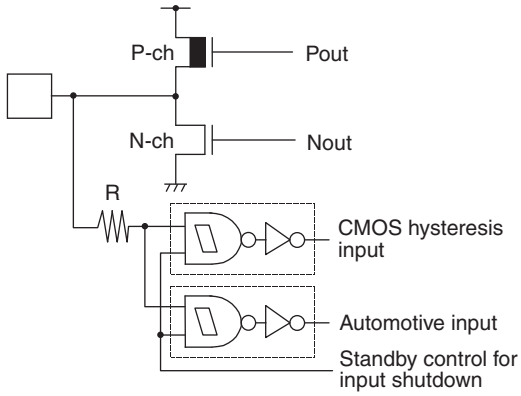


This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

Type	Circuit	Remarks
F		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
G		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) ■ Programmable pull-up resistor: 50 kΩ approx.
H		■ CMOS level output (I_{OL} = 3 mA, I_{OH} = –3 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)

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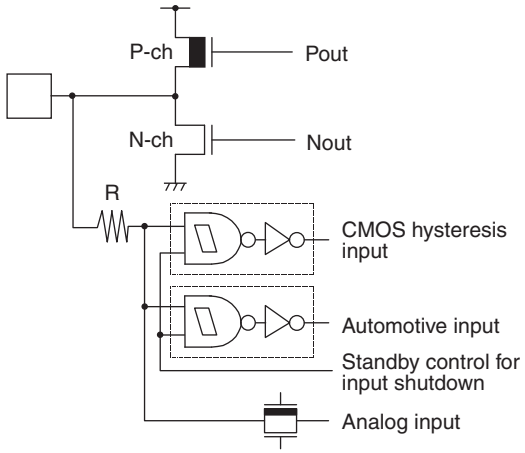
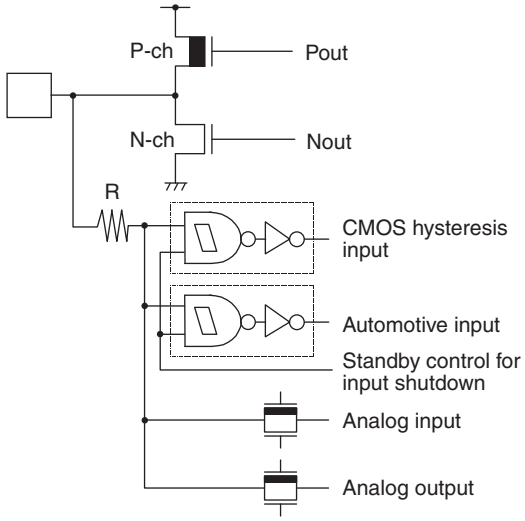
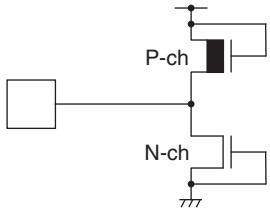
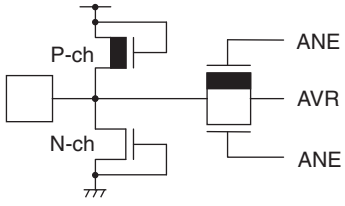
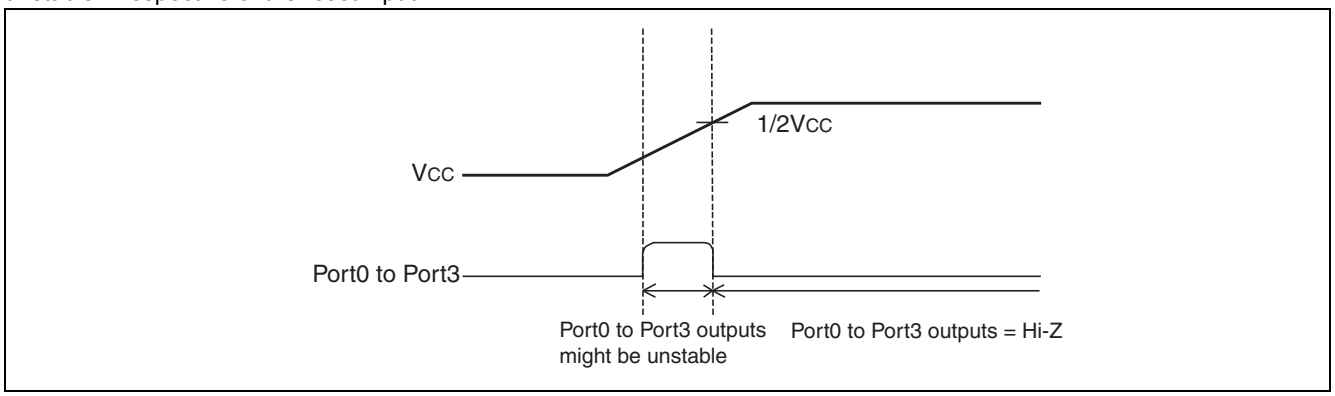
Type	Circuit	Remarks
I		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
J		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ D/A analog output ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
K		Power supply input protection circuit
L		■ A/D converter reference voltage power supply input pin, with the protection circuit ■ Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH

13.Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/60 MHz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

14.Port 0 to Port 3 Output During Power-on (External-bus Mode)

As shown below, when the power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable irrespective of the reset input.



15.Notes on Using the CAN Function

To use the CAN function, please set the DIRECT bit of the CAN Direct Mode Register (CDMR) to 1.

16.Flash Security Function (except for MB90F346E)

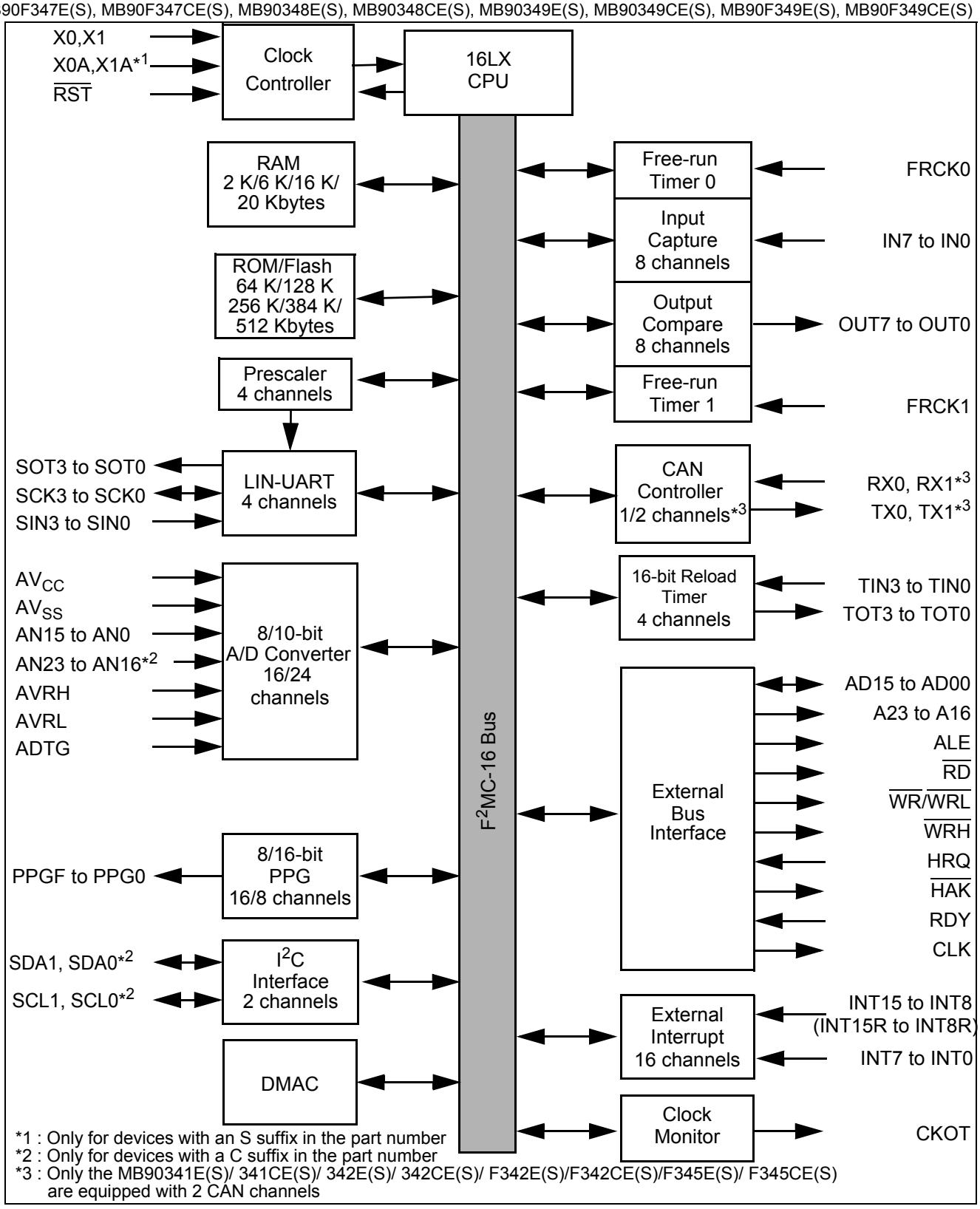
A security bit is located in the area of the flash memory.
If protection code 01_H is written in the security bit, the flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Refer to following table for the address of the security bit.

	Flash memory size	Address of the security bit
MB90F347E	Embedded 1 Mbit Flash Memory	$FE0001_H$
MB90F342E MB90F349E	Embedded 2 Mbits Flash Memory	$FC0001_H$
MB90F345E	Embedded 4 Mbits Flash Memory	$F80001_H$

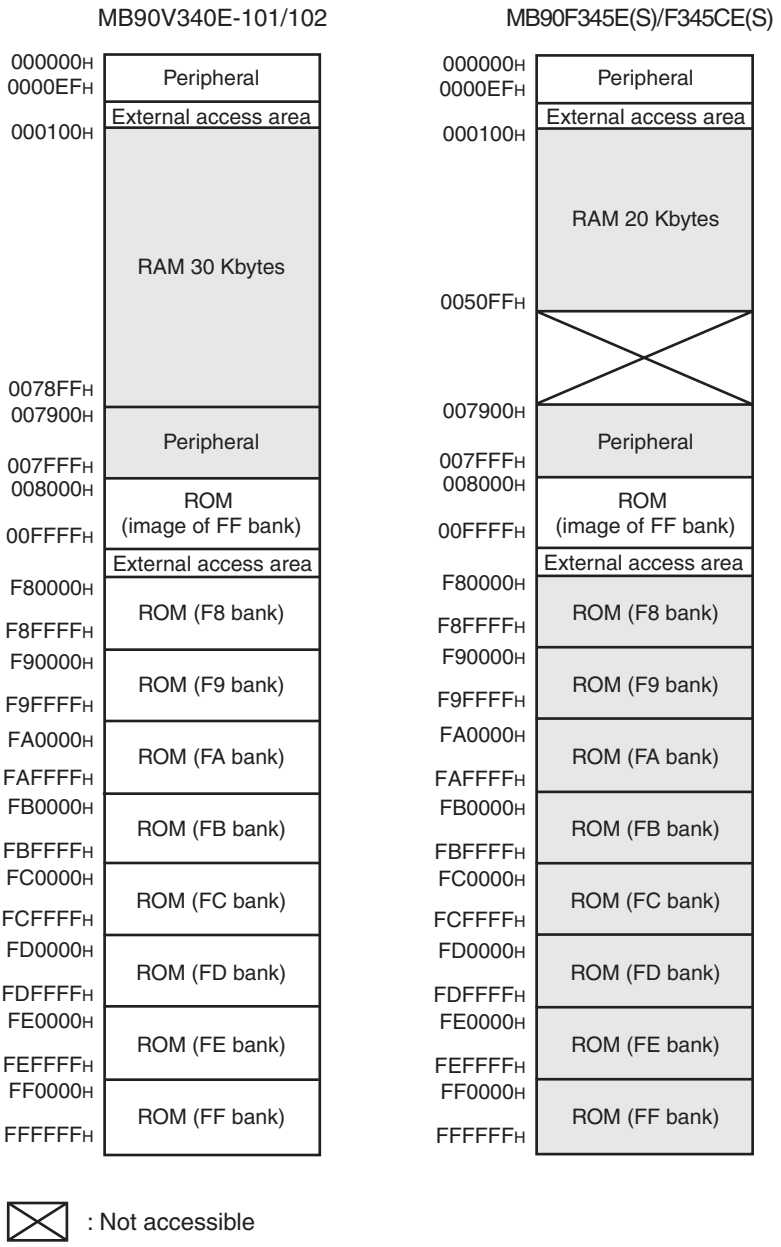
17.Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

■ MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)



7. Memory Map


MB90V340E-101/102
000000H
0000EFH
Peripheral
External access area
000100H
RAM 30 Kbytes
0078FFH
007900H
Peripheral
007FFFH
008000H
ROM
(image of FF bank)
00FFFFH
External access area
F80000H
ROM (F8 bank)
F8FFFFH
F90000H
ROM (F9 bank)
F9FFFFH
FA0000H
ROM (FA bank)
FAFFFFH
FB0000H
ROM (FB bank)
FBFFFFH
FC0000H
ROM (FC bank)
FCFFFFH
FD0000H
ROM (FD bank)
FDFFFFH
FE0000H
ROM (FE bank)
FEFFFFH
FF0000H
ROM (FF bank)
FFFFFFH
MB90F345E(S)/F345CE(S)
000000H
0000EFH
Peripheral
External access area
000100H
RAM 20 Kbytes
0050FFH
007900H
Peripheral
007FFFH
008000H
ROM
(image of FF bank)
00FFFFH
External access area
F80000H
ROM (F8 bank)
F8FFFFH
F90000H
ROM (F9 bank)
F9FFFFH
FA0000H
ROM (FA bank)
FAFFFFH
FB0000H
ROM (FB bank)
FBFFFFH
FC0000H
ROM (FC bank)
FCFFFFH
FD0000H
ROM (FD bank)
FDFFFFH
FE0000H
ROM (FE bank)
FEFFFFH
FF0000H
ROM (FF bank)
FFFFFFH
: Not accessible

Address	Register	Abbreviation	Access	Resource name	Initial value
007900_H	Reload Register L0	PRLL0	R/W	16-bit PPG 0/1	$XXXXXXXX_B$
007901_H	Reload Register H0	PRLH0	R/W		$XXXXXXXX_B$
007902_H	Reload Register L1	PRLL1	R/W		$XXXXXXXX_B$
007903_H	Reload Register H1	PRLH1	R/W		$XXXXXXXX_B$
007904_H	Reload Register L2	PRLL2	R/W	16-bit PPG 2/3	$XXXXXXXX_B$
007905_H	Reload Register H2	PRLH2	R/W		$XXXXXXXX_B$
007906_H	Reload Register L3	PRLL3	R/W		$XXXXXXXX_B$
007907_H	Reload Register H3	PRLH3	R/W		$XXXXXXXX_B$
007908_H	Reload Register L4	PRLL4	R/W	16-bit PPG 4/5	$XXXXXXXX_B$
007909_H	Reload Register H4	PRLH4	R/W		$XXXXXXXX_B$
$00790A_H$	Reload Register L5	PRLL5	R/W		$XXXXXXXX_B$
$00790B_H$	Reload Register H5	PRLH5	R/W		$XXXXXXXX_B$
$00790C_H$	Reload Register L6	PRLL6	R/W	16-bit PPG 6/7	$XXXXXXXX_B$
$00790D_H$	Reload Register H6	PRLH6	R/W		$XXXXXXXX_B$
$00790E_H$	Reload Register L7	PRLL7	R/W		$XXXXXXXX_B$
$00790F_H$	Reload Register H7	PRLH7	R/W		$XXXXXXXX_B$
007910_H	Reload Register L8	PRLL8	R/W	16-bit PPG 8/9	$XXXXXXXX_B$
007911_H	Reload Register H8	PRLH8	R/W		$XXXXXXXX_B$
007912_H	Reload Register L9	PRLL9	R/W		$XXXXXXXX_B$
007913_H	Reload Register H9	PRLH9	R/W		$XXXXXXXX_B$
007914_H	Reload Register LA	PRLLA	R/W	16-bit PPG A/B	$XXXXXXXX_B$
007915_H	Reload Register HA	PRLHA	R/W		$XXXXXXXX_B$
007916_H	Reload Register LB	PRLLB	R/W		$XXXXXXXX_B$
007917_H	Reload Register HB	PRLHB	R/W		$XXXXXXXX_B$
007918_H	Reload Register LC	PRLLC	R/W	16-bit PPG C/D	$XXXXXXXX_B$
007919_H	Reload Register HC	PRLHC	R/W		$XXXXXXXX_B$
$00791A_H$	Reload Register LD	PRLLD	R/W		$XXXXXXXX_B$
$00791B_H$	Reload Register HD	PRLHD	R/W		$XXXXXXXX_B$
$00791C_H$	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	$XXXXXXXX_B$
$00791D_H$	Reload Register HE	PRLHE	R/W		$XXXXXXXX_B$
$00791E_H$	Reload Register LF	PRLLF	R/W		$XXXXXXXX_B$
$00791F_H$	Reload Register HF	PRLHF	R/W		$XXXXXXXX_B$
007920_H	Input Capture 0	IPCP0	R	Input Capture 0/1	$XXXXXXXX_B$
007921_H	Input Capture 0	IPCP0	R		$XXXXXXXX_B$
007922_H	Input Capture 1	IPCP1	R		$XXXXXXXX_B$
007923_H	Input Capture 1	IPCP1	R		$XXXXXXXX_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007924_H	Input Capture 2	IPCP2	R	Input Capture 2/3	$XXXXXXXX_B$
007925_H	Input Capture 2	IPCP2	R		$XXXXXXXX_B$
007926_H	Input Capture 3	IPCP3	R		$XXXXXXXX_B$
007927_H	Input Capture 3	IPCP3	R		$XXXXXXXX_B$
007928_H	Input Capture 4	IPCP4	R	Input Capture 4/5	$XXXXXXXX_B$
007929_H	Input Capture 4	IPCP4	R		$XXXXXXXX_B$
$00792A_H$	Input Capture 5	IPCP5	R		$XXXXXXXX_B$
$00792B_H$	Input Capture 5	IPCP5	R		$XXXXXXXX_B$
$00792C_H$	Input Capture 6	IPCP6	R	Input Capture 6/7	$XXXXXXXX_B$
$00792D_H$	Input Capture 6	IPCP6	R		$XXXXXXXX_B$
$00792E_H$	Input Capture 7	IPCP7	R		$XXXXXXXX_B$
$00792F_H$	Input Capture 7	IPCP7	R		$XXXXXXXX_B$
007930_H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	$XXXXXXXX_B$
007931_H	Output Compare 0	OCCP0	R/W		$XXXXXXXX_B$
007932_H	Output Compare 1	OCCP1	R/W		$XXXXXXXX_B$
007933_H	Output Compare 1	OCCP1	R/W		$XXXXXXXX_B$
007934_H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	$XXXXXXXX_B$
007935_H	Output Compare 2	OCCP2	R/W		$XXXXXXXX_B$
007936_H	Output Compare 3	OCCP3	R/W		$XXXXXXXX_B$
007937_H	Output Compare 3	OCCP3	R/W		$XXXXXXXX_B$
007938_H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	$XXXXXXXX_B$
007939_H	Output Compare 4	OCCP4	R/W		$XXXXXXXX_B$
$00793A_H$	Output Compare 5	OCCP5	R/W		$XXXXXXXX_B$
$00793B_H$	Output Compare 5	OCCP5	R/W		$XXXXXXXX_B$
$00793C_H$	Output Compare 6	OCCP6	R/W	Output Compare 6/7	$XXXXXXXX_B$
$00793D_H$	Output Compare 6	OCCP6	R/W		$XXXXXXXX_B$
$00793E_H$	Output Compare 7	OCCP7	R/W		$XXXXXXXX_B$
$00793F_H$	Output Compare 7	OCCP7	R/W		$XXXXXXXX_B$
007940_H	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000_B
007941_H	Timer Data 0	TCDT0	R/W		00000000_B
007942_H	Timer Control Status 0	TCCSL0	R/W		00000000_B
007943_H	Timer Control Status 0	TCCSH0	R/W		$0XXXXXXX_B$
007944_H	Timer Data 1	TCDT1	R/W	Free-run Timer 1	00000000_B
007945_H	Timer Data 1	TCDT1	R/W		00000000_B
007946_H	Timer Control Status 1	TCCSL1	R/W		00000000_B
007947_H	Timer Control Status 1	TCCSH1	R/W		$0XXXXXXX_B$

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Interrupt cause	EI^{2}OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX / UART 4 RX	Y2	14	#39	$FFFF60_H$	ICR14	$0000BE_H$
UART 2 TX / UART 4 TX	Y1	15	#40	$FFFF5C_H$		
Flash Memory	N	——	#41	$FFFF58_H$	ICR15	$0000BF_H$
Delayed Interrupt	N	——	#42	$FFFF54_H$		

Y1 : Usable
Y2 : Usable, with EI^{2}OS stop function
N : Unusable

Note:
- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
- When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

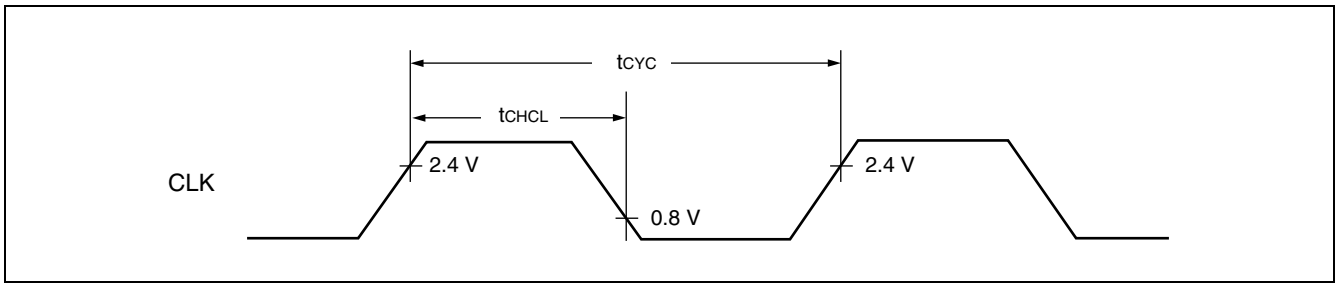
11.4 AC Characteristics

11.4.1 Clock Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP}≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	When using an oscillation circuit
			4	—	16	MHz	PLL multiplied by 1 When using an oscillation circuit
			4	—	12	MHz	PLL multiplied by 2 When using an oscillation circuit
			4	—	8	MHz	PLL multiplied by 3 When using an oscillation circuit
			4	—	6	MHz	PLL multiplied by 4 When using an oscillation circuit
			—	—	4	MHz	PLL multiplied by 6 When using an oscillation circuit
			3	—	24	MHz	When using an external clock*
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	µs	When using sub clock

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in “Relation between the external clock frequency and machine clock frequency”.


tCYC
tCHCL
CLK
2.4 V
2.4 V
0.8 V

11.4.9 LIN-UART0/1/2/3

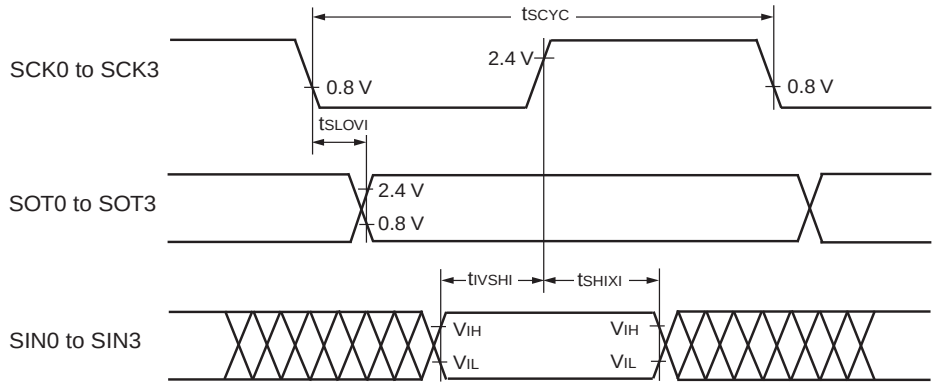
■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0**

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		−50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock “L” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “H” pulse width	t_{SLSH}	SCK0 to SCK3		t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SIN0 to SIN3		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

Note:
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

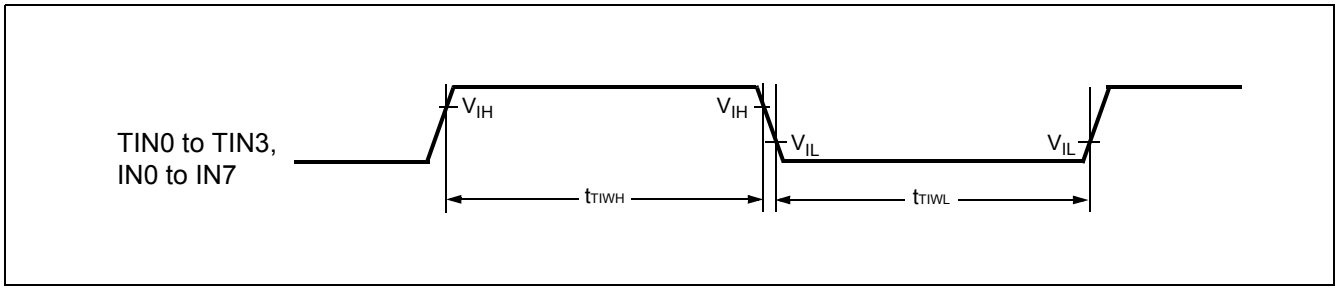
- Internal Shift Clock Mode



11.4.11 Timer Related Resource Input Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

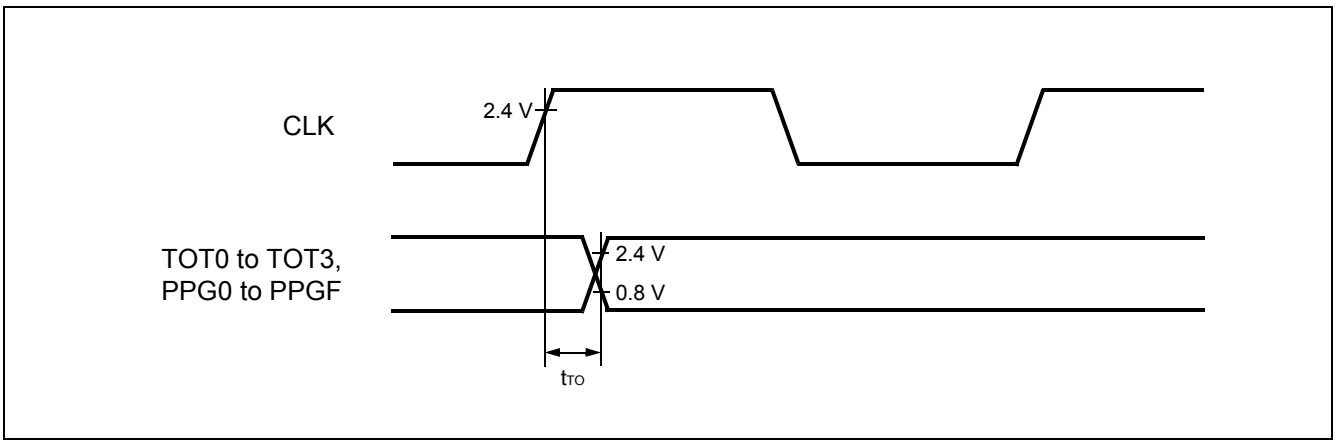
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN3, IN0 to IN7	—	4 t_{CP}	—	ns



11.4.12 Timer Related Resource Output Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns



11.5 A/D Converter

(T_A = −40°C to +105°C, 3.0 V≤ AVRH − AVRL, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP}≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	AVRL − 1.5 × LSB	AVRL + 0.5 × LSB	AVRL + 2.5 × LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	AVRH − 3.5 × LSB	AVRH − 1.5 × LSB	AVRH + 0.5 × LSB	V	
Compare time	—	—	1.0	—	16500	µs	4.5 V≤ AV_{CC}≤ 5.5 V
			2.0				4.0 V≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	∞	µs	4.5 V≤ AV_{CC}≤ 5.5 V
			1.2				4.0 V≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN23	−0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 2.7	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

*: If the A/D convertor is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .
Note: : The accuracy gets worse as |AVRH − AVRL| becomes smaller.

11.8 Flash Memory Program/Erase Characteristics

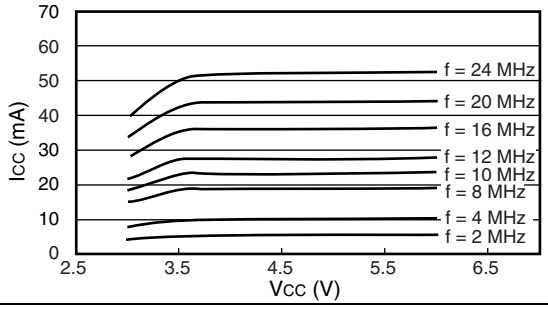
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25°C$ $V_{CC} = 5.0$ V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	µs	Except for the over head time of the system
Program/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average $T_A = +85°C$	20	—	—	year	*

* : This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85°C) .

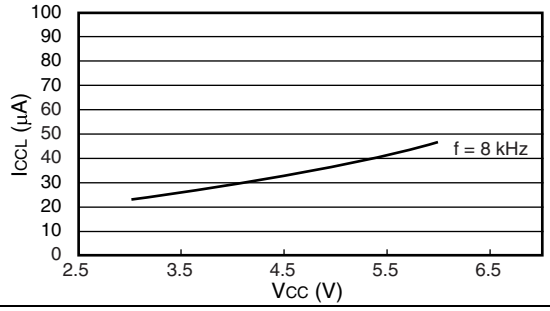
12. Example Characteristics

- MB90F346E, MB90F346ES, MB90F346CE, MB90F346CES

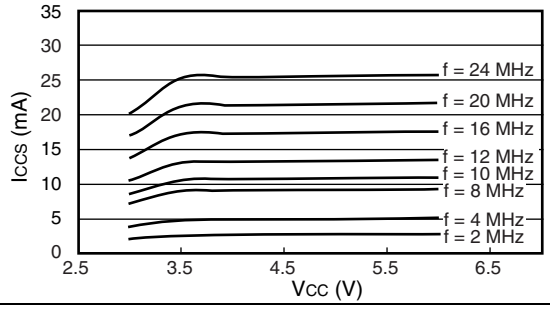
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



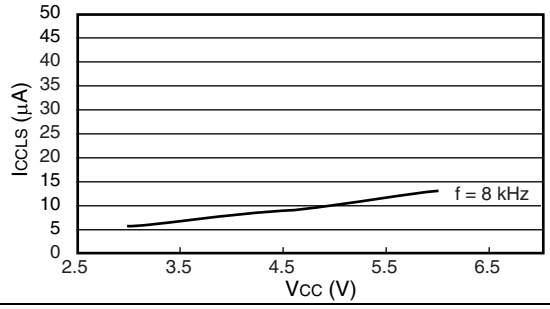
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



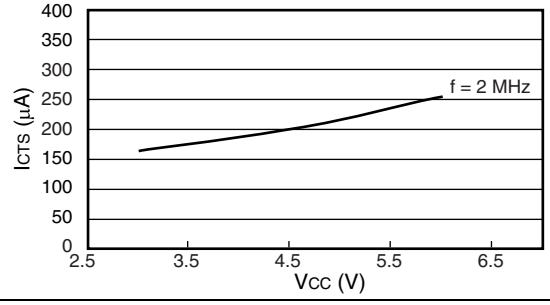
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



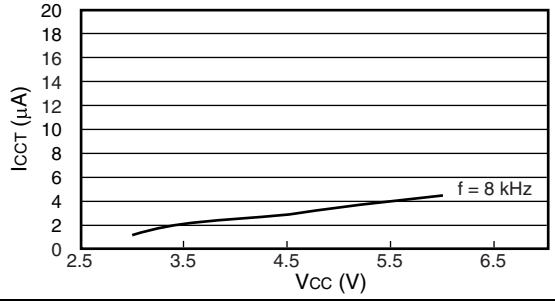
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



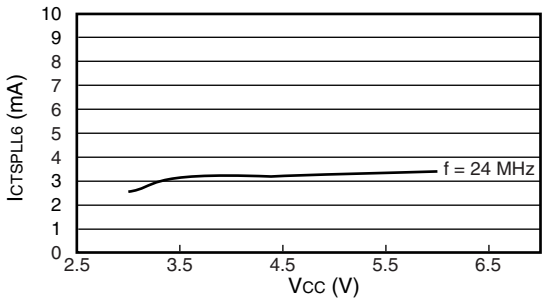
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



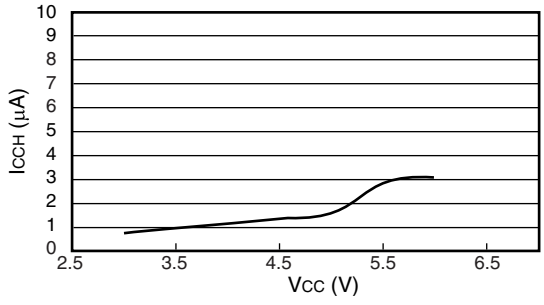
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency

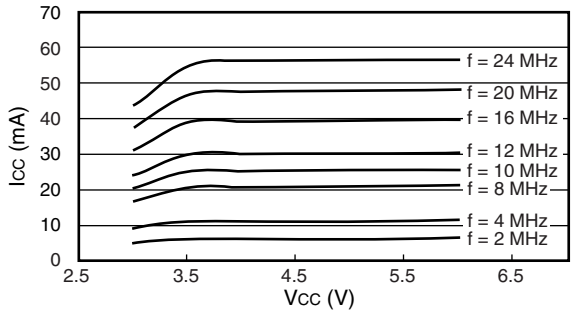


$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

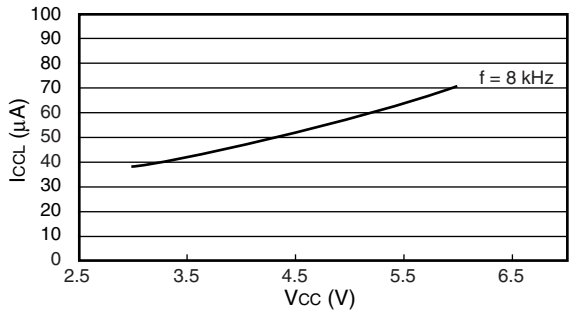


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

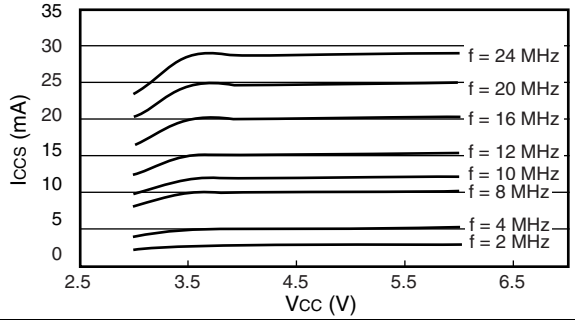
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



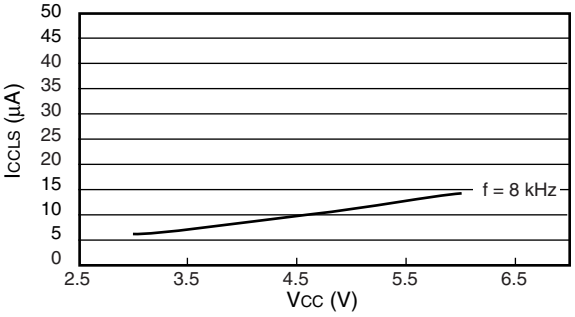
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



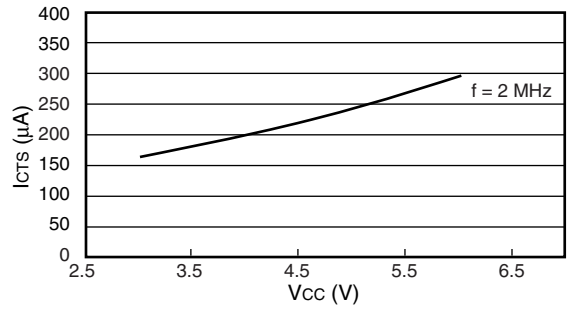
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



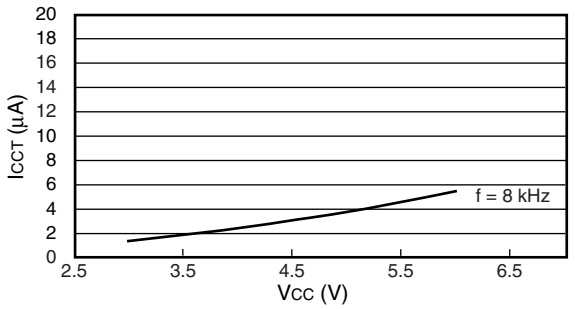
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



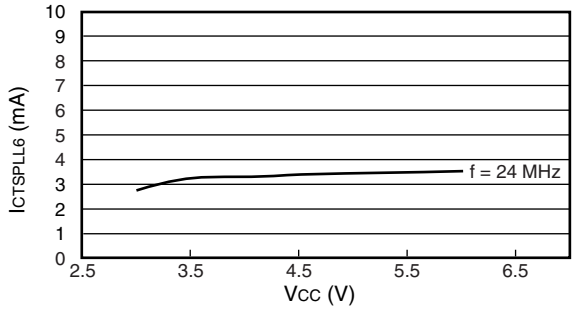
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



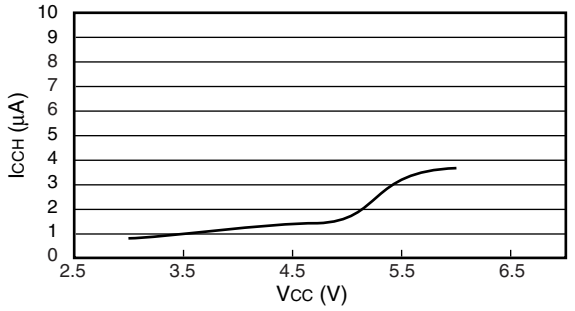
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency

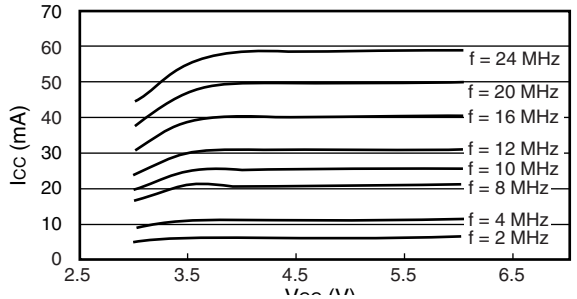


$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

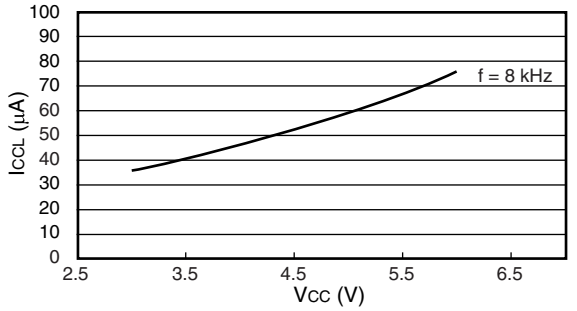


■ MB90F345E, MB90F345ES, MB90F345CE, MB90F345CES

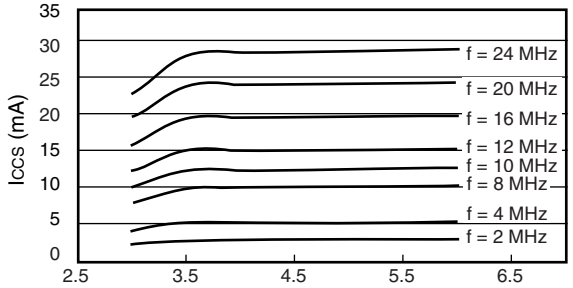
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



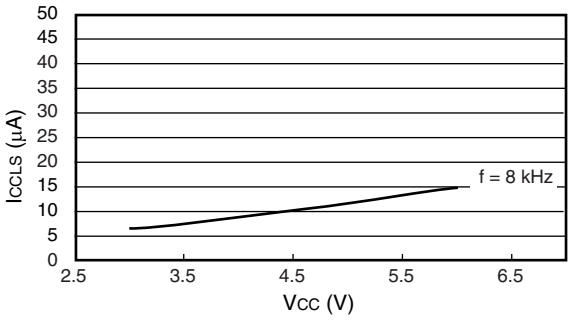
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



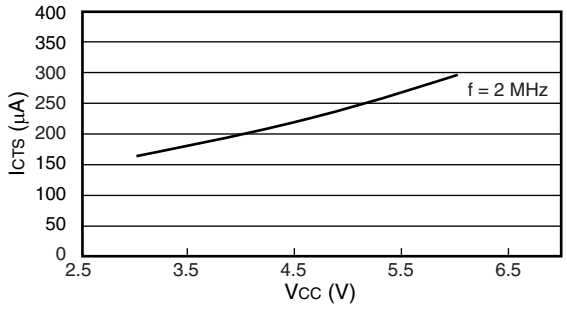
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



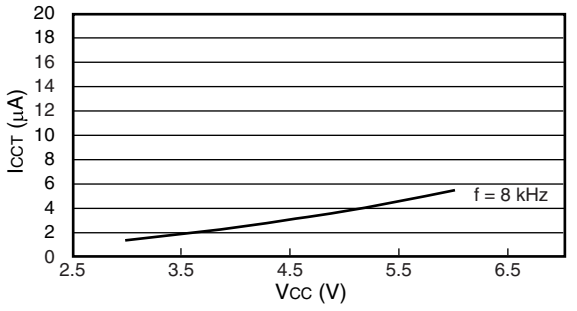
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



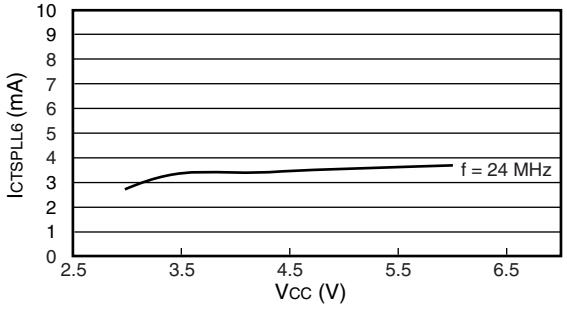
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped