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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-670e1

Contents

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101)
		X0A, X1A	B	Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102)
15	13	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
16	14	V_{SS}	—	GND pin
17	15	C	K	This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 µF.
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture.
		RX1		RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only)
		INT9R		External interrupt request input pin

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
66	64	V_{SS}	—	GND pin
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pins
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pins
		OUT0 to OUT3		Waveform output pins for output compares. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin
76	74	PA1	F	General purpose I/O pin.
		TX0		TX Output pin for CAN0
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer

(Continued)

5. Handling Devices

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Handling unused pins

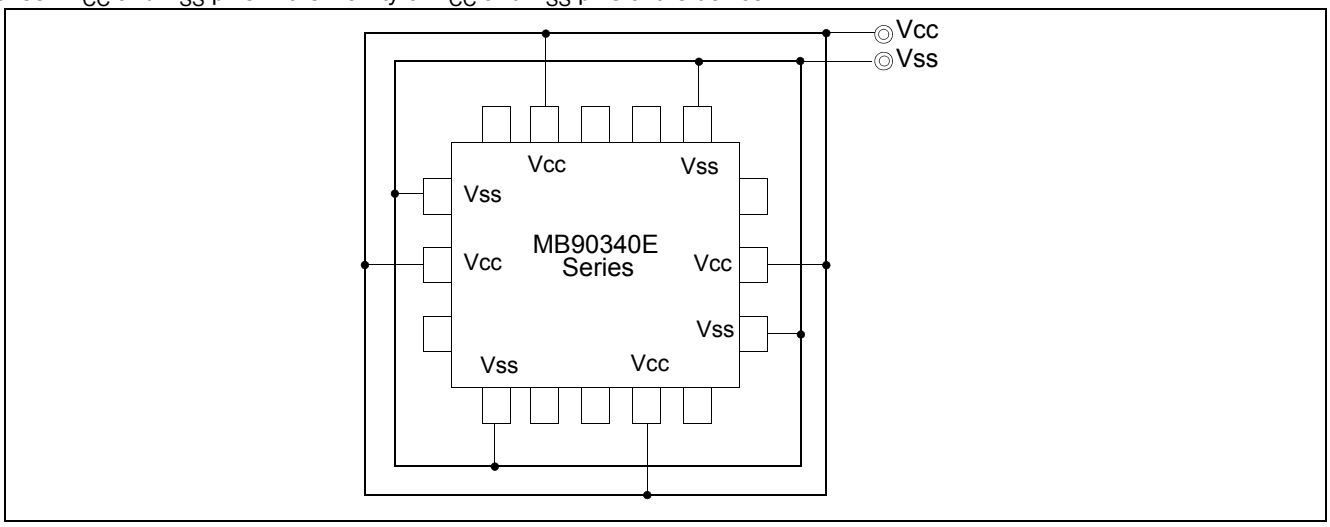
Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 kΩ or more.

3. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
Connect V_{CC} and V_{SS} pins to the device from the current supply source at a possibly low impedance.

- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.

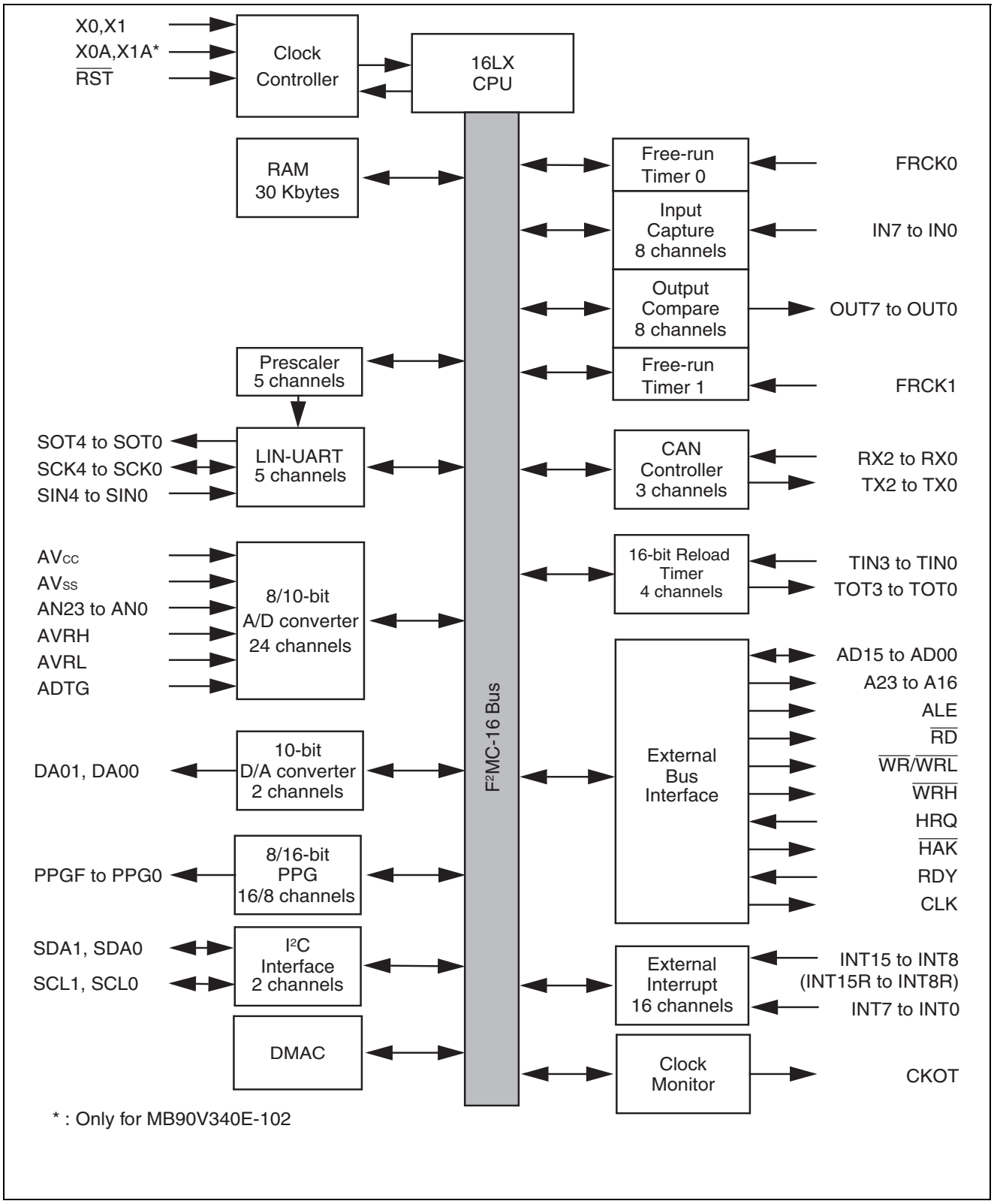


4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

6. Block Diagrams

- MB90V340E-101/102



Address	Register	Abbreviation	Access	Resource name	Initial value
000040_H	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	$0X000XX1_B$
000041_H	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		$0X000001_B$
000042_H	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		$000000X0_B$
000043_H	Reserved				
000044_H	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	$0X000XX1_B$
000045_H	PPG B Operation Mode Control Register	PPGCB	W,R/W		$0X000001_B$
000046_H	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		$000000X0_B$
000047_H	Reserved				
000048_H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	$0X000XX1_B$
000049_H	PPG D Operation Mode Control Register	PPGCD	W,R/W		$0X000001_B$
$00004A_H$	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		$000000X0_B$
$00004B_H$	Reserved				
$00004C_H$	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	$0X000XX1_B$
$00004D_H$	PPG F Operation Mode Control Register	PPGCF	W,R/W		$0X000001_B$
$00004E_H$	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		$000000X0_B$
$00004F_H$	Reserved				
000050_H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000_B
000051_H	Input Capture Edge 0/1	ICE01	R/W, R		$XXX0X0XX_B$
000052_H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000_B
000053_H	Input Capture Edge 2/3	ICE23	R		$XXXXXXXX_B$
000054_H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000_B
000055_H	Input Capture Edge 4/5	ICE45	R		$XXXXXXXX_B$
000056_H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000_B
000057_H	Input Capture Edge 6/7	ICE67	R/W, R		$XXX000XX_B$
000058_H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	$0000XX00_B$
000059_H	Output Compare Control Status 1	OCS1	R/W		$0XX00000_B$
$00005A_H$	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	$0000XX00_B$
$00005B_H$	Output Compare Control Status 3	OCS3	R/W		$0XX00000_B$
$00005C_H$	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	$0000XX00_B$
$00005D_H$	Output Compare Control Status 5	OCS5	R/W		$0XX00000_B$
$00005E_H$	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	$0000XX00_B$
$00005F_H$	Output Compare Control Status 7	OCS7	R/W		$0XX00000_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000060_H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000_B
000061_H	Timer Control Status 0	TMCSR0	R/W		$XXXX0000_B$
000062_H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000_B
000063_H	Timer Control Status 1	TMCSR1	R/W		$XXXX0000_B$
000064_H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000_B
000065_H	Timer Control Status 2	TMCSR2	R/W		$XXXX0000_B$
000066_H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000_B
000067_H	Timer Control Status 3	TMCSR3	R/W		$XXXX0000_B$
000068_H	A/D Control Status 0	ADCS0	R/W	A/D Converter	$000XXXX0_B$
000069_H	A/D Control Status 1	ADCS1	R/W		$0000000X_B$
$00006A_H$	A/D Data 0	ADCR0	R		00000000_B
$00006B_H$	A/D Data 1	ADCR1	R		$XXXXXX00_B$
$00006C_H$	ADC Setting 0	ADSR0	R/W		00000000_B
$00006D_H$	ADC Setting 1	ADSR1	R/W		00000000_B
$00006E_H$	Reserved				
$00006F_H$	ROM Mirror Function Select	ROMM	W	ROM Mirror	$XXXXXXX1_B$
000070_H to $00008F_H$	Reserved for CAN Controller 0/1. Refer to "CAN Controllers"				
000090_H to $00009A_H$	Reserved				
$00009B_H$	DMA Descriptor Channel Specified Register	DCSR	R/W	DMA	00000000_B
$00009C_H$	DMA Status L Register	DSRL	R/W		00000000_B
$00009D_H$	DMA Status H Register	DSRH	R/W		00000000_B
$00009E_H$	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000_B
$00009F_H$	Delayed Interrupt Trigger/Release Register	DIRR	R/W	Delayed Interrupt	$XXXXXXX0_B$
$0000A0_H$	Low-power Mode Control Register	LPMCR	W,R/W	Low Power Control Circuit	00011000_B
$0000A1_H$	Clock Selection Register	CKSCR	R,R/W	Low Power Control Circuit	11111100_B
$0000A2_H$, $0000A3_H$	Reserved				
$0000A4_H$	DMA Stop Status Register	DSSR	R/W	DMA	00000000_B

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Address	Register	Abbreviation	Access	Resource name	Initial value
$0079E0_H$	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	$XXXXXXXX_B$
$0079E1_H$	Detect Address Setting 0	PADR0	R/W		$XXXXXXXX_B$
$0079E2_H$	Detect Address Setting 0	PADR0	R/W		$XXXXXXXX_B$
$0079E3_H$	Detect Address Setting 1	PADR1	R/W		$XXXXXXXX_B$
$0079E4_H$	Detect Address Setting 1	PADR1	R/W		$XXXXXXXX_B$
$0079E5_H$	Detect Address Setting 1	PADR1	R/W		$XXXXXXXX_B$
$0079E6_H$	Detect Address Setting 2	PADR2	R/W		$XXXXXXXX_B$
$0079E7_H$	Detect Address Setting 2	PADR2	R/W		$XXXXXXXX_B$
$0079E8_H$	Detect Address Setting 2	PADR2	R/W		$XXXXXXXX_B$
$0079E9_H$ to $0079EF_H$	Reserved				
$0079F0_H$	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	$XXXXXXXX_B$
$0079F1_H$	Detect Address Setting 3	PADR3	R/W		$XXXXXXXX_B$
$0079F2_H$	Detect Address Setting 3	PADR3	R/W		$XXXXXXXX_B$
$0079F3_H$	Detect Address Setting 4	PADR4	R/W		$XXXXXXXX_B$
$0079F4_H$	Detect Address Setting 4	PADR4	R/W		$XXXXXXXX_B$
$0079F5_H$	Detect Address Setting 4	PADR4	R/W		$XXXXXXXX_B$
$0079F6_H$	Detect Address Setting 5	PADR5	R/W		$XXXXXXXX_B$
$0079F7_H$	Detect Address Setting 5	PADR5	R/W		$XXXXXXXX_B$
$0079F8_H$	Detect Address Setting 5	PADR5	R/W		$XXXXXXXX_B$
$0079F9_H$ to $0079FF_H$	Reserved				
$007A00_H$ to $007AFF_H$	Reserved for CAN Controller 0. Refer to “CAN Controllers				
$007B00_H$ to $007BFF_H$	Reserved for CAN Controller 0. Refer to “CAN Controllers”				
$007C00_H$ to $007CFF_H$	Reserved for CAN Controller 1. Refer to “CAN Controllers”				
$007D00_H$ to $007DFF_H$	Reserved for CAN Controller 1. Refer to “CAN Controllers”				
$007E00_H$ to $007FFF_H$	Reserved				

Note:
- Initial value of “X” represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A60_H$	$007C60_H$	DLC Register 0	DLCR0	R/W	$XXXXXXXX_B$
$007A61_H$	$007C61_H$				
$007A62_H$	$007C62_H$	DLC Register 1	DLCR1	R/W	$XXXXXXXX_B$
$007A63_H$	$007C63_H$				
$007A64_H$	$007C64_H$	DLC Register 2	DLCR2	R/W	$XXXXXXXX_B$
$007A65_H$	$007C65_H$				
$007A66_H$	$007C66_H$	DLC Register 3	DLCR3	R/W	$XXXXXXXX_B$
$007A67_H$	$007C67_H$				
$007A68_H$	$007C68_H$	DLC Register 4	DLCR4	R/W	$XXXXXXXX_B$
$007A69_H$	$007C69_H$				
$007A6A_H$	$007C6A_H$	DLC Register 5	DLCR5	R/W	$XXXXXXXX_B$
$007A6B_H$	$007C6B_H$				
$007A6C_H$	$007C6C_H$	DLC Register 6	DLCR6	R/W	$XXXXXXXX_B$
$007A6D_H$	$007C6D_H$				
$007A6E_H$	$007C6E_H$	DLC Register 7	DLCR7	R/W	$XXXXXXXX_B$
$007A6F_H$	$007C6F_H$				
$007A70_H$	$007C70_H$	DLC Register 8	DLCR8	R/W	$XXXXXXXX_B$
$007A71_H$	$007C71_H$				
$007A72_H$	$007C72_H$	DLC Register 9	DLCR9	R/W	$XXXXXXXX_B$
$007A73_H$	$007C73_H$				
$007A74_H$	$007C74_H$	DLC Register 10	DLCR10	R/W	$XXXXXXXX_B$
$007A75_H$	$007C75_H$				
$007A76_H$	$007C76_H$	DLC Register 11	DLCR11	R/W	$XXXXXXXX_B$
$007A77_H$	$007C77_H$				
$007A78_H$	$007C78_H$	DLC Register 12	DLCR12	R/W	$XXXXXXXX_B$
$007A79_H$	$007C79_H$				
$007A7A_H$	$007C7A_H$	DLC Register 13	DLCR13	R/W	$XXXXXXXX_B$
$007A7B_H$	$007C7B_H$				
$007A7C_H$	$007C7C_H$	DLC Register 14	DLCR14	R/W	$XXXXXXXX_B$
$007A7D_H$	$007C7D_H$				
$007A7E_H$	$007C7E_H$	DLC Register 15	DLCR15	R/W	$XXXXXXXX_B$
$007A7F_H$	$007C7F_H$				

List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007AF0_H$ to $007AF7_H$	$007CF0_H$ to $007CF7_H$	Data Register 14 (8 bytes)	DTR14	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AF8_H$ to $007AFF_H$	$007CF8_H$ to $007CFF_H$	Data Register 15 (8 bytes)	DTR15	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI^{2}OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC$_H$	—	—
INT9 instruction	N	—	#09	FFFFD8$_H$	—	—
Exception	N	—	#10	FFFFD4$_H$	—	—
CAN 0 RX	N	—	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N	—	#12	FFFFCC$_H$		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4$_H$		
CAN 2 RX / I^{2}C0	N	—	#15	FFFFC0$_H$	ICR02	0000B2$_H$
CAN 2 TX/NS	N	—	#16	FFFFBC$_H$		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8$_H$	ICR03	0000B3$_H$
16-bit Reload Timer 1	Y1	1	#18	FFFFB4$_H$		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit Reload Timer 3	Y1	—	#20	FFFFAC$_H$		
PPG 0/1/4/5	N	—	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG 2/3/6/7	N	—	#22	FFFFA4$_H$		
PPG 8/9/C/D	N	—	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG A/B/E/F	N	—	#24	FFFF9C$_H$		
Time Base Timer	N	—	#25	FFFF98$_H$	ICR07	0000B7$_H$
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94$_H$		
Watch Timer	N	—	#27	FFFF90$_H$	ICR08	0000B8$_H$
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C$_H$		
A/D Converter	Y1	5	#29	FFFF88$_H$	ICR09	0000B9$_H$
Free-run Timer 0 / Free-run Timer 1	N	—	#30	FFFF84$_H$		
Input Capture 4/5 / I^{2}C1	Y1	6	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C$_H$		
Input Capture 0 to 3	Y1	8	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output Compare 2/3/6/7	Y1	9	#34	FFFF74$_H$		
UART 0 RX	Y2	10	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART 0 TX	Y1	11	#36	FFFF6C$_H$		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64$_H$		

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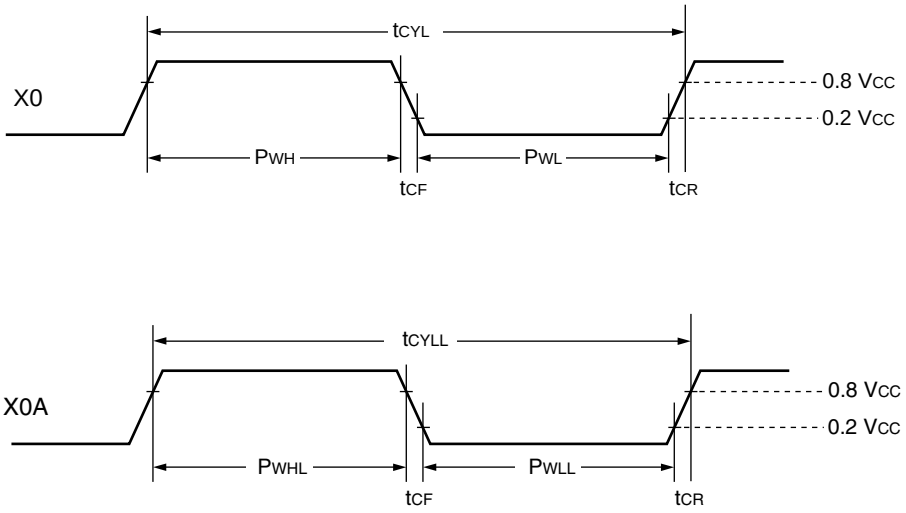
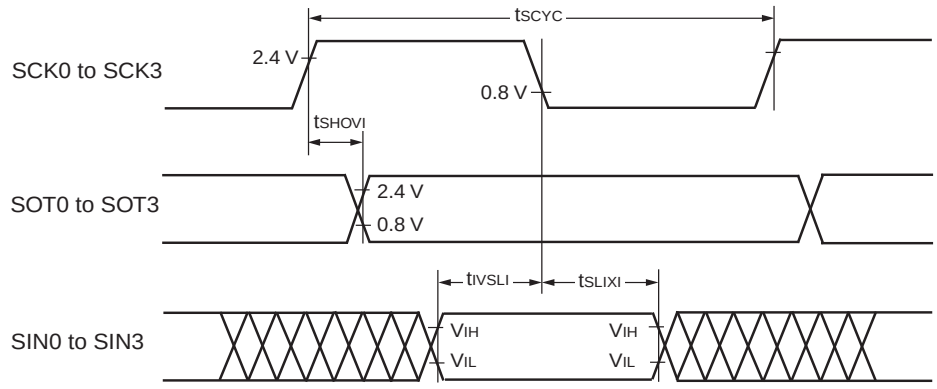
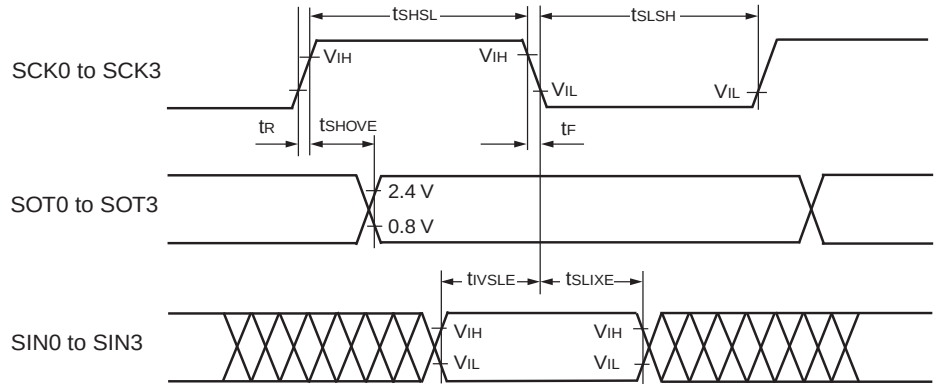
Clock Timing



- Internal Shift Clock Mode



- External Shift Clock Mode

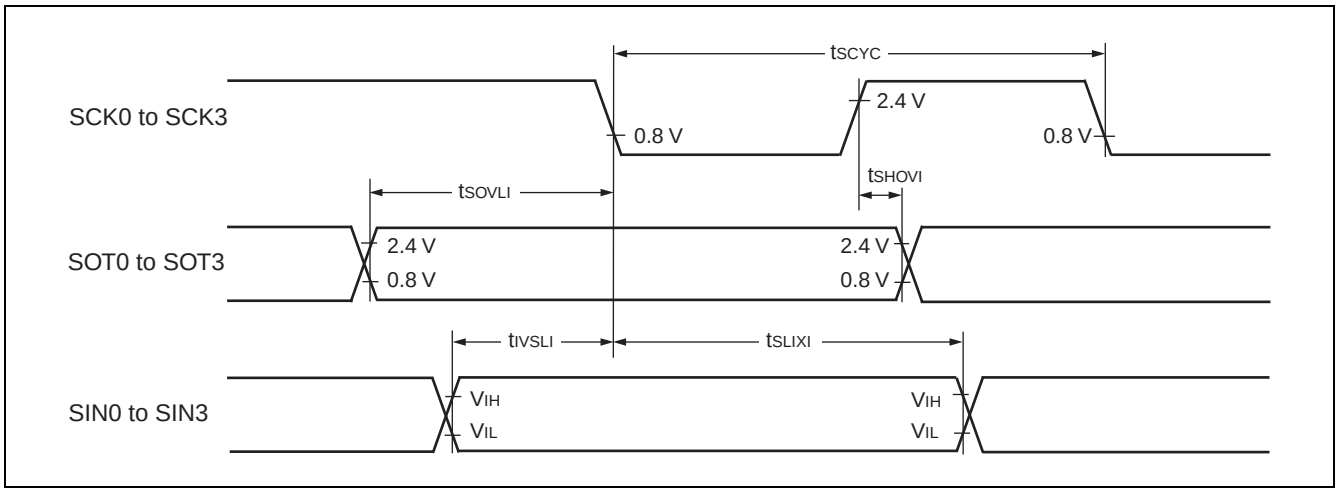


■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1**

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		−50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} − 70	—	ns

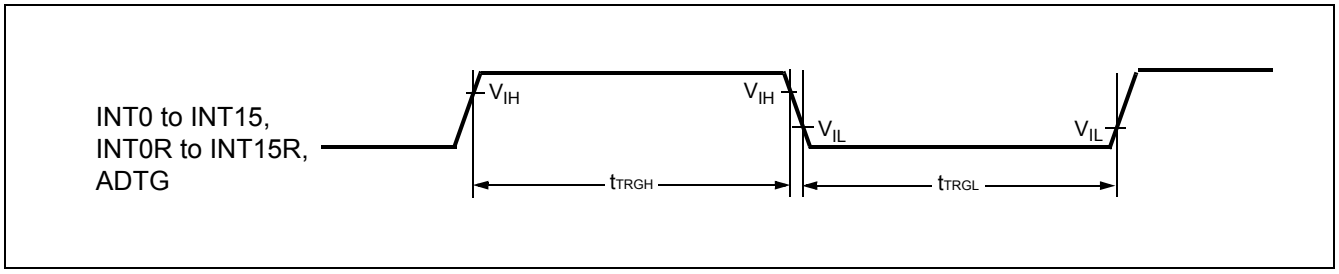
Note:
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".



11.4.10 Trigger Input Timing

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0.0 V)

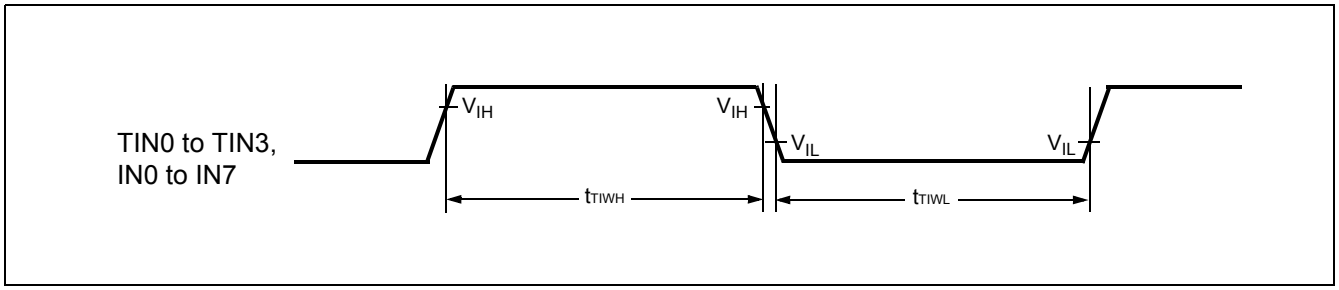
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT15, INT0R to INT15R, ADTG	—	5 t_{CP}	—	ns



11.4.11 Timer Related Resource Input Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

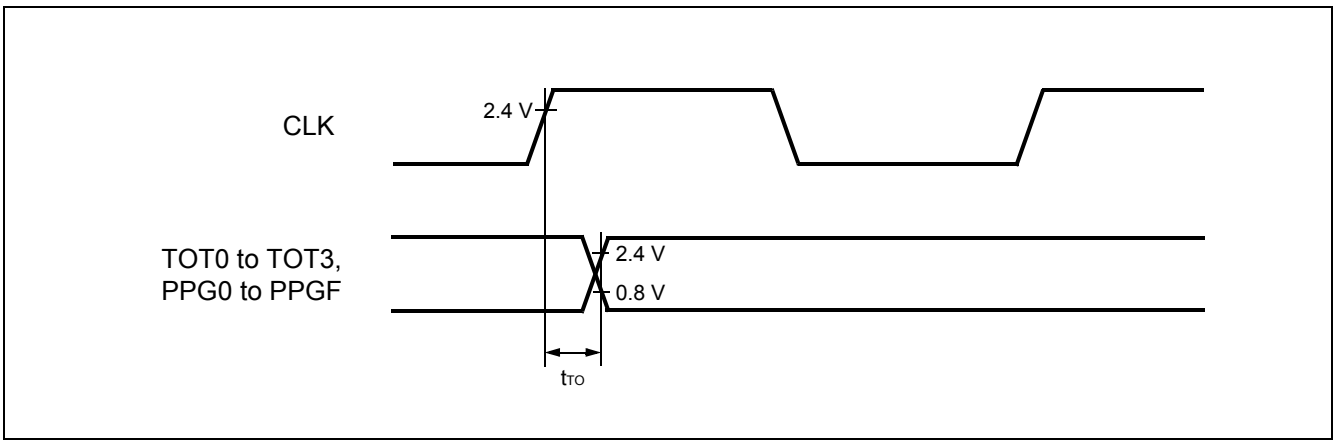
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN3, IN0 to IN7	—	4 t_{CP}	—	ns



11.4.12 Timer Related Resource Output Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0.0 V)

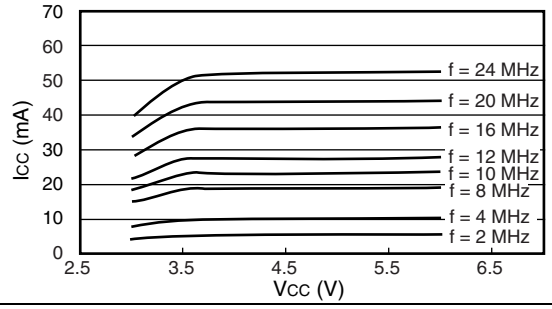
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns



■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES

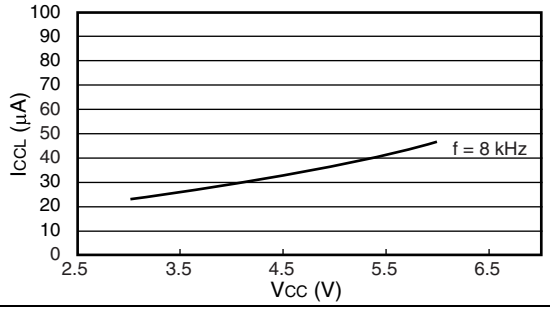
$I_{CC} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



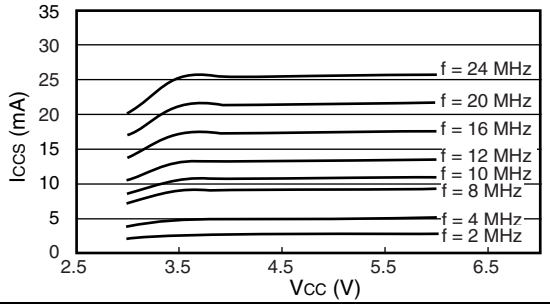
$I_{CCL} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



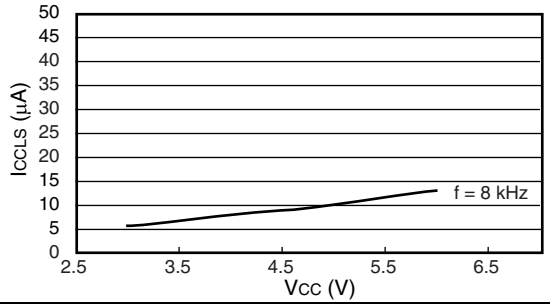
$I_{CCS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



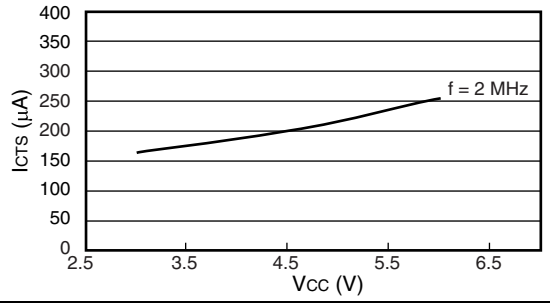
$I_{CCLS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



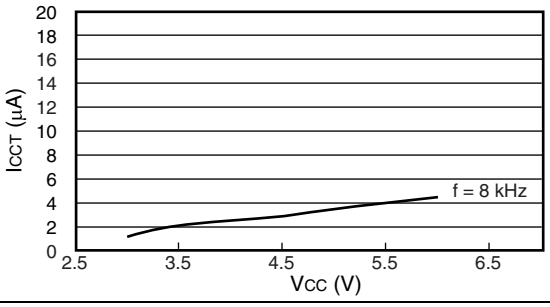
$I_{CTS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



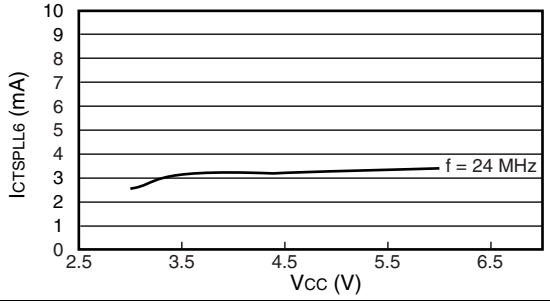
$I_{CCT} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



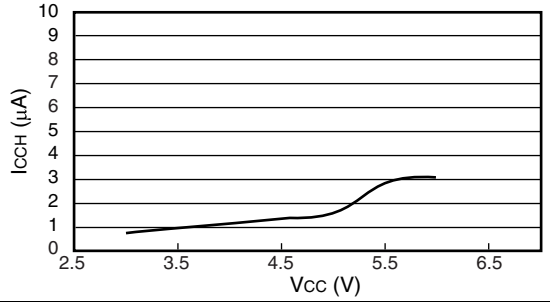
$I_{CTSPLL6} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



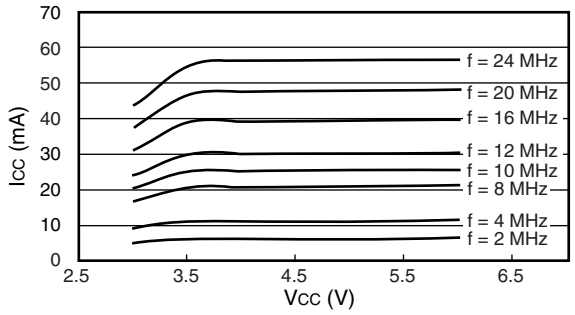
$I_{CCH} - V_{CC}$

$T_A = +25°C$, stopped

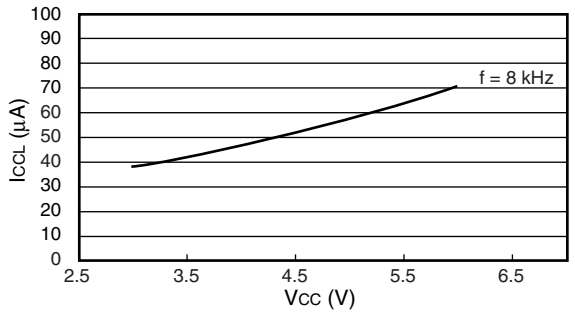


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

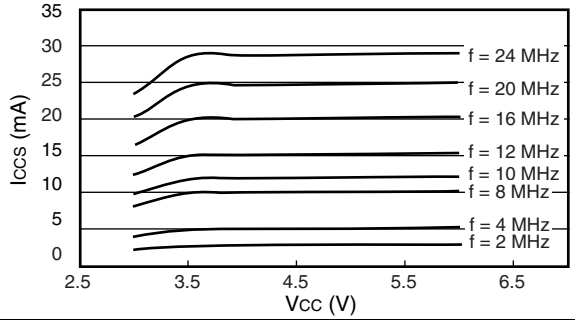
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



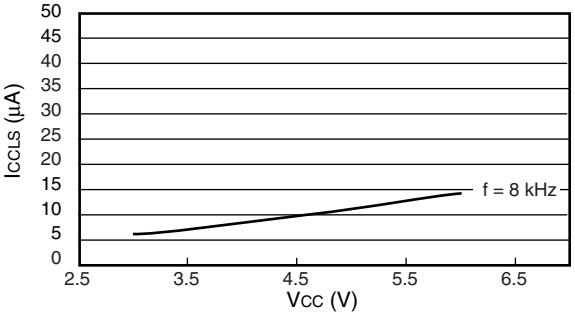
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



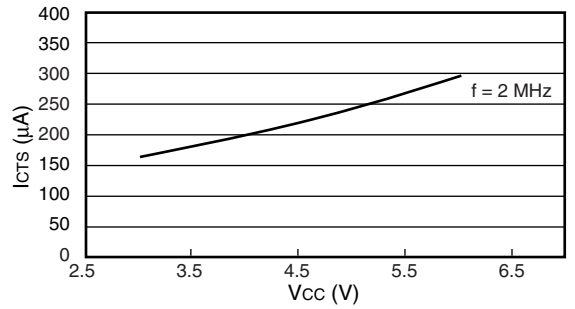
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



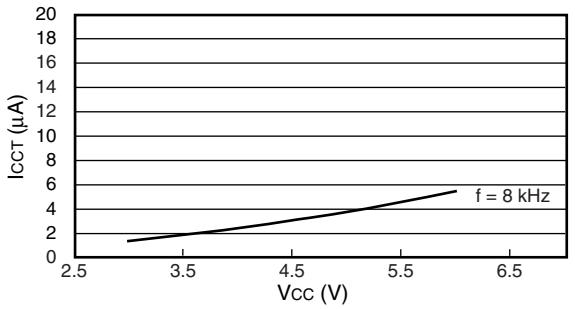
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



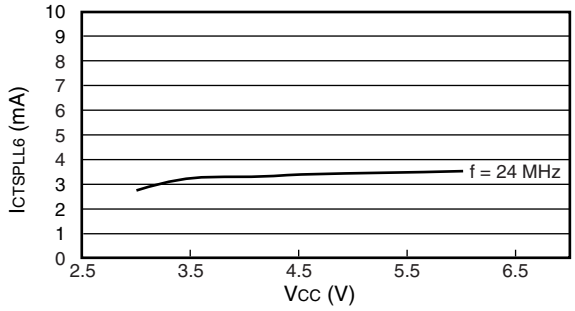
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



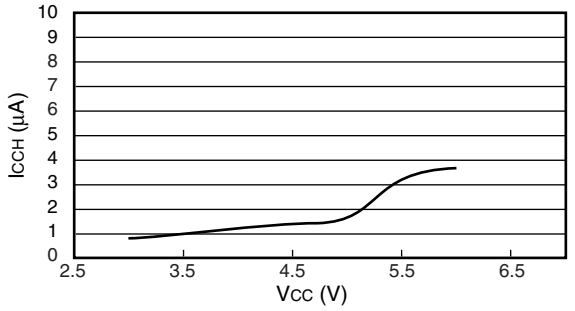
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency

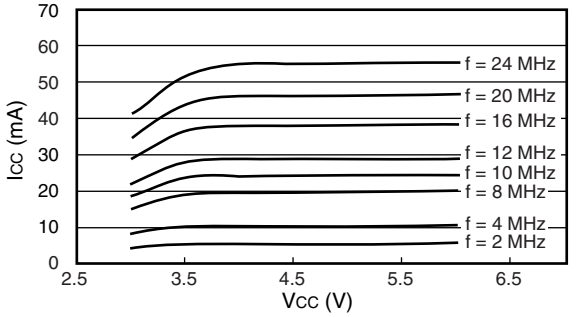


$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

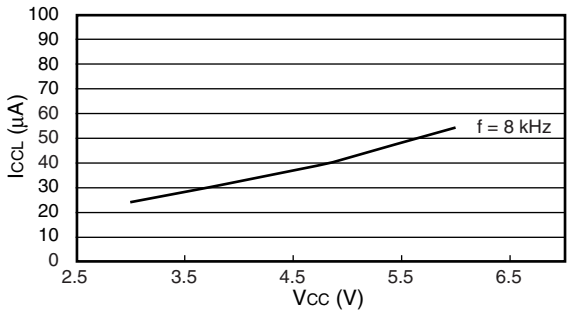


■ MB90346E, MB90346ES, MB90346CE, MB90346CES

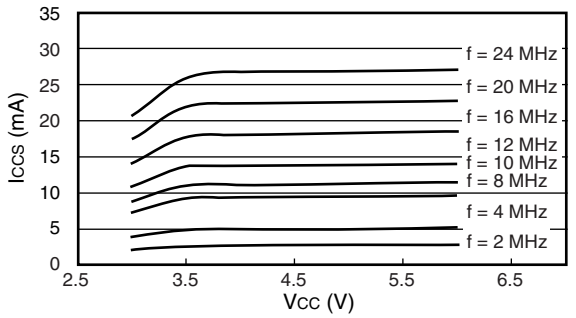
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



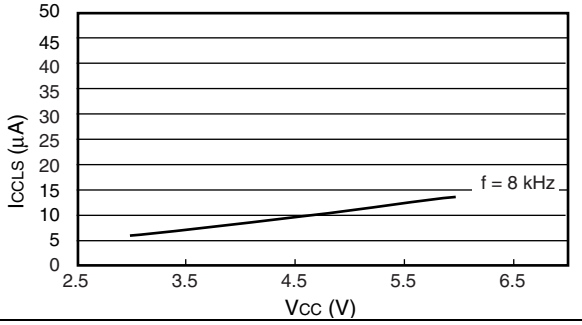
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



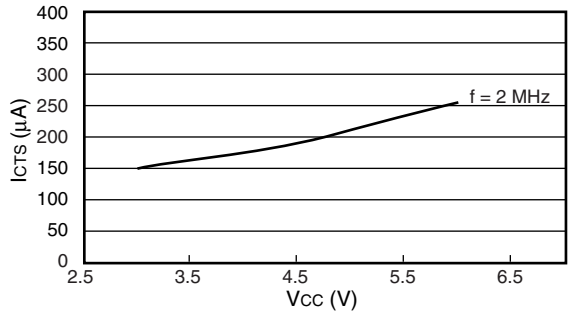
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



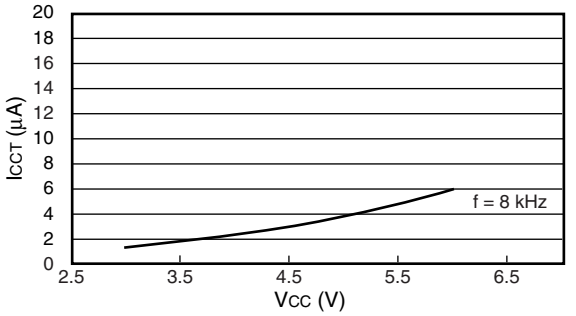
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



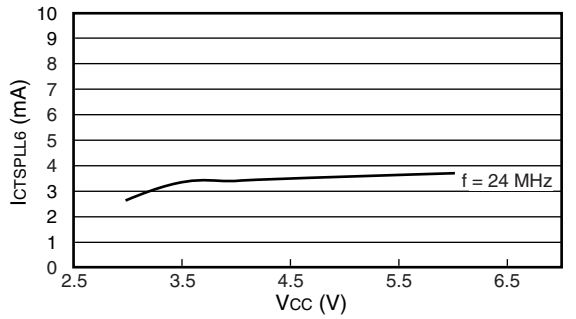
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



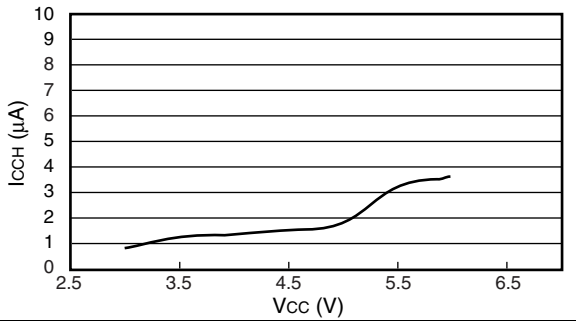
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency

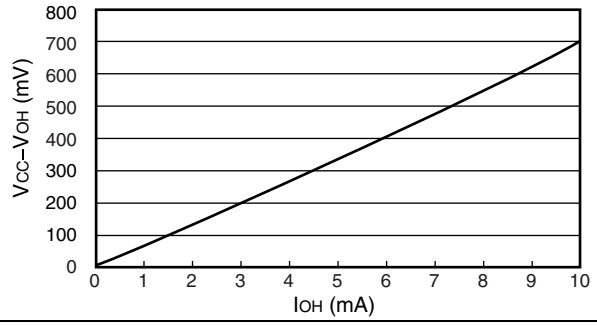


$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

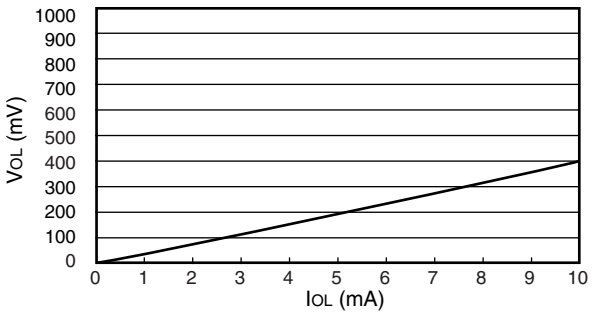


■ I/O characteristics

$(V_{CC}-V_{OH})$ – I_{OH}
T_A = +25°C, V_{CC} = 4.5 V

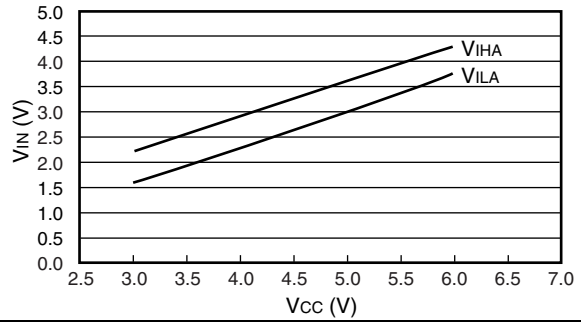


V_{OL} – I_{OL}
T_A = +25°C, V_{CC} = 4.5 V

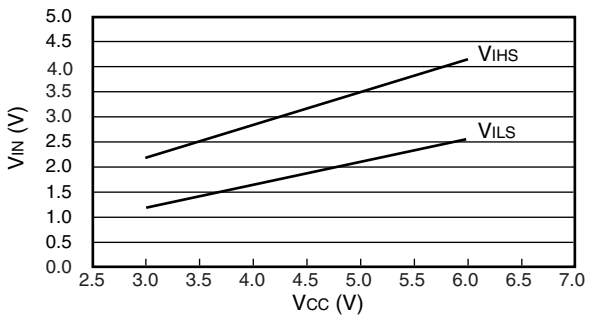


Automotive V_{IN} – V_{CC}

T_A = +25°C

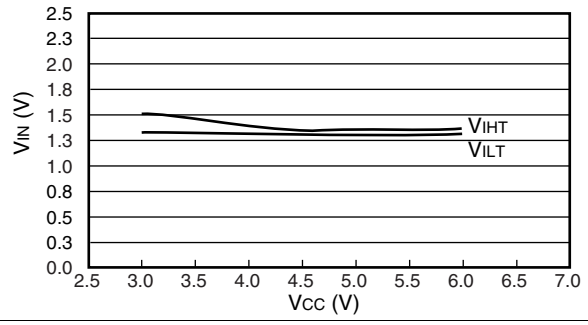


CMOS V_{IN} – V_{CC}
Other than UART-SIN pin and I^2C pin
T_A = +25°C



TTL V_{IN} – V_{CC}

T_A = +25°C



CMOS V_{IN} – V_{CC}
UART-SIN pin, I^2C pin
T_A = +25°C