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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

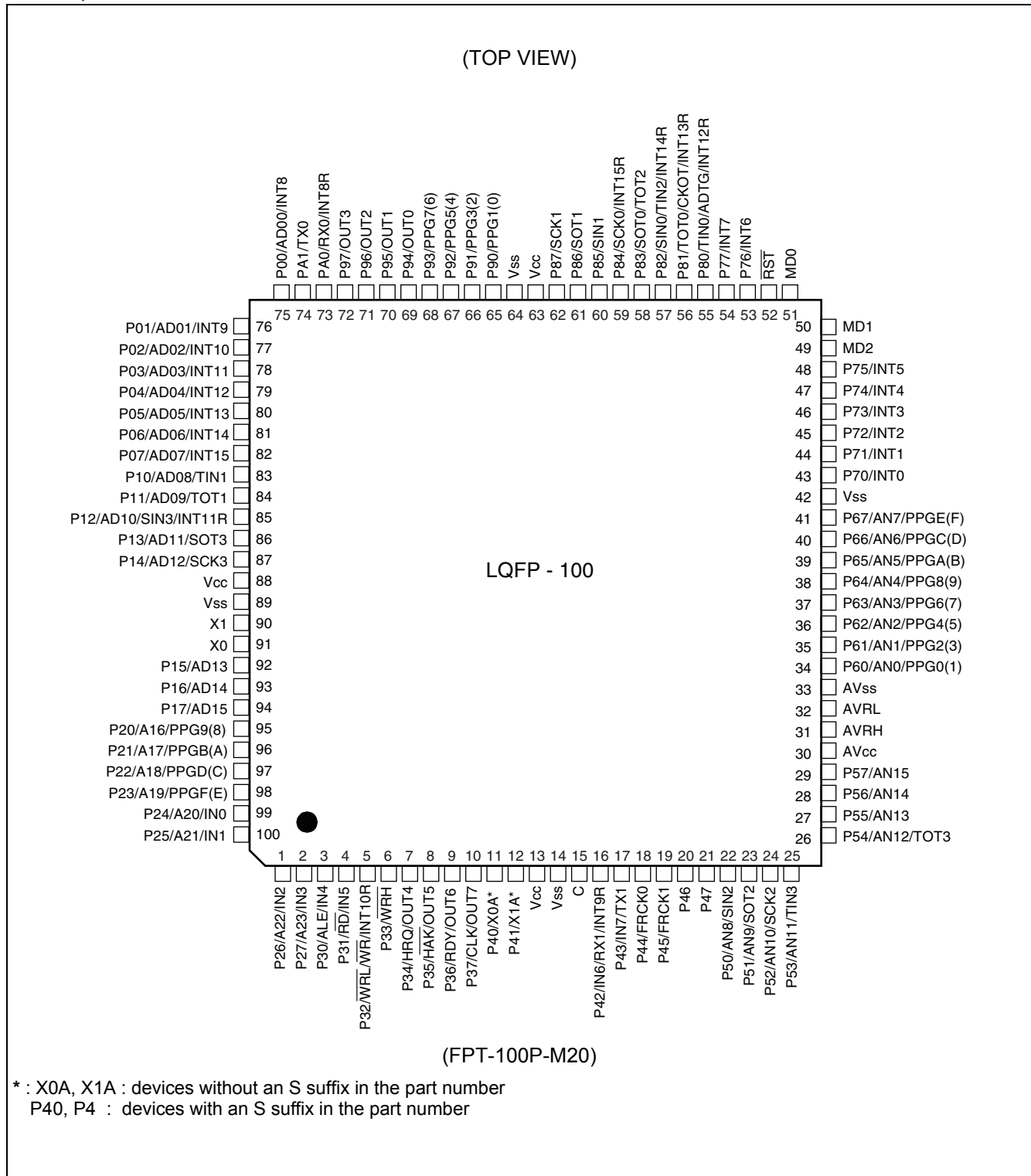
Product Status	Obsolete
Core Processor	F <sup>2</sup> MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-677e1">https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-677e1</a>

## 1. Product Lineup

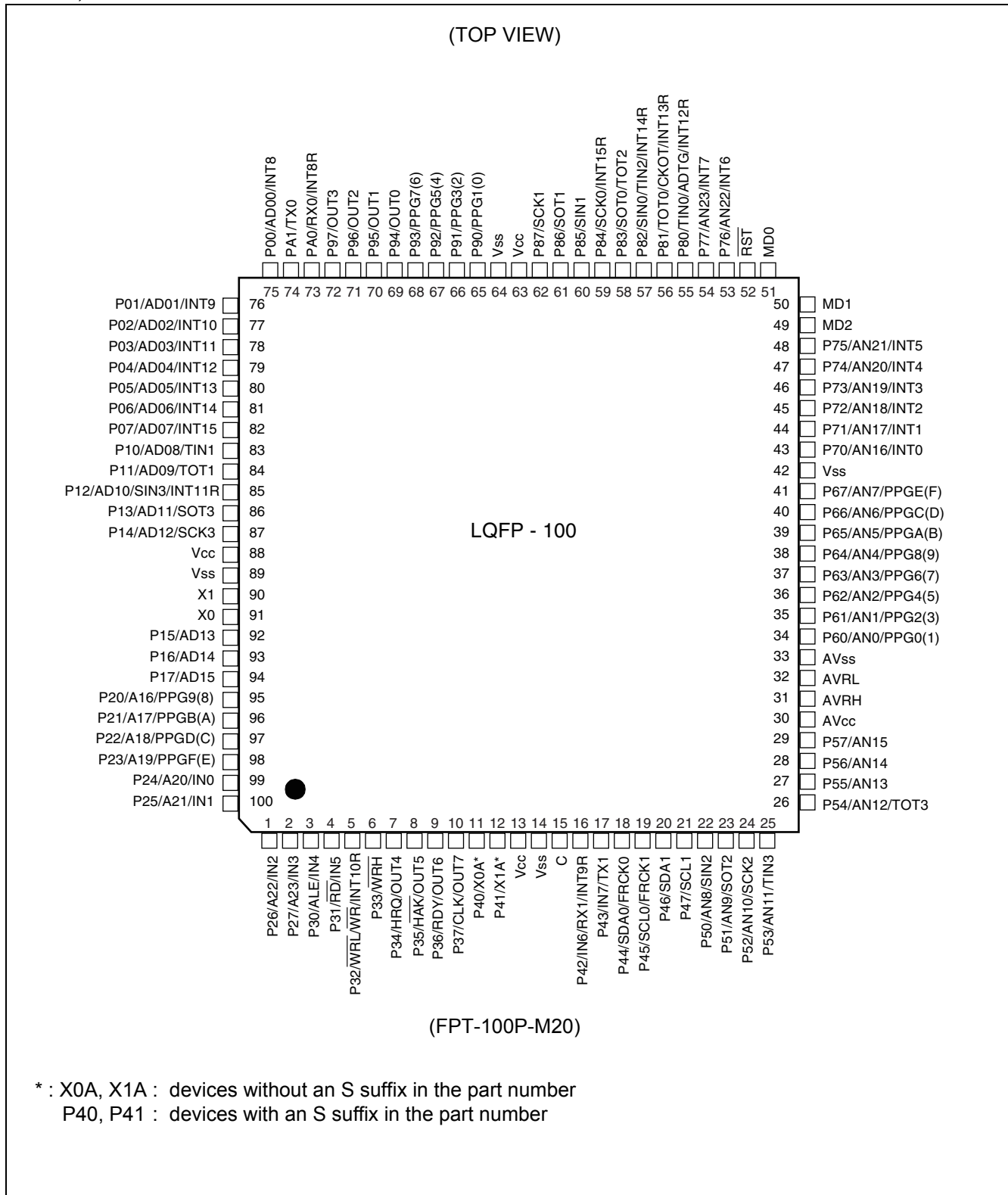
<div>Part Number</div> <div>Parameter</div>	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
Type	Evaluation products	Flash memory products	MASK ROM products
CPU	F <sup>2</sup> MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)		
ROM	External	512 Kbytes : MB90F345E(S), MB90F345CE(S) 256 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 128 Kbytes : MB90F347E(S), MB90F347CE(S) 64 Kbytes : MB90F346E(S), MB90F346CE(S)	256 Kbytes : MB90342E(S), MB90342CE(S), MB90349E(S), MB90349CE(S) 128 Kbytes : MB90341E(S), MB90341CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S) 64 Kbytes : MB90346E(S), MB90346CE(S)
RAM	30 Kbytes	20 Kbytes : MB90F345E(S), MB90F345CE(S) 16 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 6 Kbytes : MB90F347E(S), MB90F347CE(S) 2 Kbytes : MB90F346E(S), MB90F346CE(S)	16 Kbytes : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) 6 Kbytes : MB90347E(S), MB90347CE(S) 2 Kbytes : MB90346E(S), MB90346CE(S)
Emulator-specific power supply*	Yes	—	
Technology	0.35 μm CMOS with regulator for built-in power supply	0.35 μm CMOS with built-in power supply regulator + Flash memory with Charge pump for programming voltage	
Operating voltage range	5 V ± 10%	3.5 V to 5.5 V : When normal operating (not using A/D converter) 4.0 V to 5.5 V : When using the A/D converter/Flash programming 4.5 V to 5.5 V : When using the external bus	
Temperature range	—	−40°C to +105°C	
Package	PGA-299	QFP-100, LQFP-100	
LIN-UART	5 channels	4 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device		
I <sup>2</sup> C (400 kbps)	2 channels	Devices with a C suffix in the part number : 2 channels Devices without a C suffix in the part number : —	

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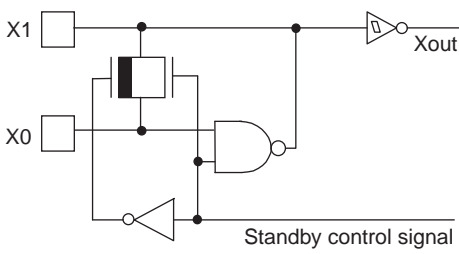
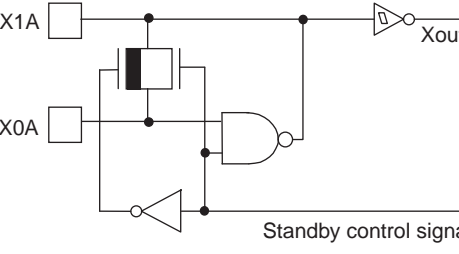

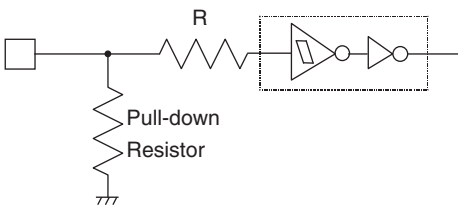
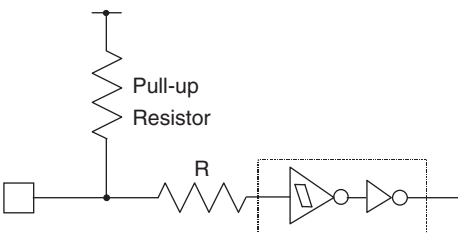
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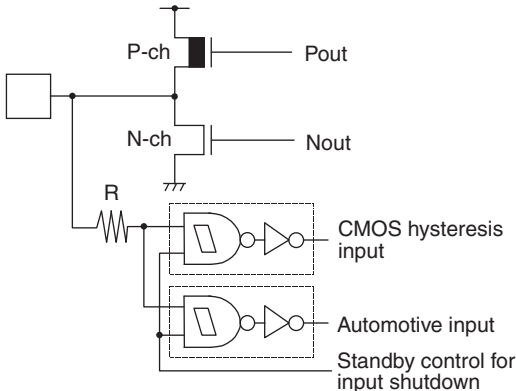
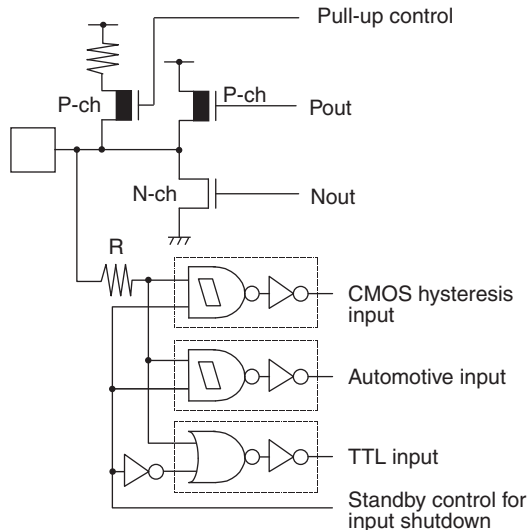
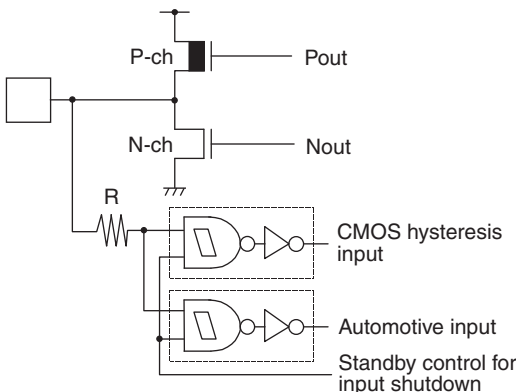
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I <sup>2</sup> C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV <sub>CC</sub>	K	Analog power input pin for the A/D Converter

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#### 4. I/O Circuit Type

Type	Circuit	Remarks
A		<p>Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ</p>
B		<p>Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ</p>
C		<ul style="list-style-type: none"> <li>■ MASK ROM and evaluation products: CMOS hysteresis input pin</li> <li>■ Flash memory products: CMOS input pin</li> </ul>
D		<p>MASK ROM and evaluation products:</p> <ul style="list-style-type: none"> <li>■ CMOS hysteresis input pin</li> <li>■ Pull-down resistor value: approx. 50 kΩ</li> </ul> <p>Flash memory products:</p> <ul style="list-style-type: none"> <li>■ CMOS input pin</li> <li>■ No pull-down</li> </ul>
E		<p>CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ</p>

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Type	Circuit	Remarks
F		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> </ul>
G		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 4 \text{ mA}</math>, <math>I_{OH} = -4 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> <li>■ TTL input (with function to disconnect input during standby)</li> <li>■ Programmable pull-up resistor: 50 kΩ approx.</li> </ul>
H		<ul style="list-style-type: none"> <li>■ CMOS level output (<math>I_{OL} = 3 \text{ mA}</math>, <math>I_{OH} = -3 \text{ mA}</math>)</li> <li>■ CMOS hysteresis input (with function to disconnect input during standby)</li> <li>■ Automotive input (with function to disconnect input during standby)</li> </ul>

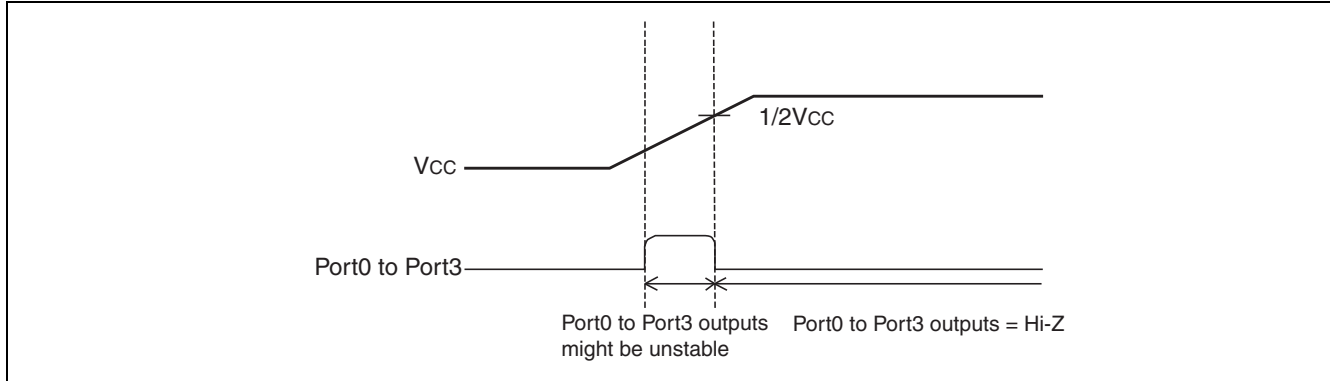
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### 13. Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the  $V_{CC}$  supply voltage operating range. Therefore, the  $V_{CC}$  supply voltage should be stabilized. For reference, the supply voltage should be controlled so that  $V_{CC}$  ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/60 MHz) fall below 10% of the standard  $V_{CC}$  supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

### 14. Port 0 to Port 3 Output During Power-on (External-bus Mode)

As shown below, when the power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable irrespective of the reset input.



### 15. Notes on Using the CAN Function

To use the CAN function, please set the DIRECT bit of the CAN Direct Mode Register (CDMR) to 1.

### 16. Flash Security Function (except for MB90F346E)

A security bit is located in the area of the flash memory.

If protection code  $01_H$  is written in the security bit, the flash memory is in the protected state by security.

Therefore please do not write  $01_H$  in this address if you do not use the security function.

Refer to following table for the address of the security bit.

	Flash memory size	Address of the security bit
MB90F347E	Embedded 1 Mbit Flash Memory	FE0001 <sub>H</sub>
MB90F342E MB90F349E	Embedded 2 Mbits Flash Memory	FC0001 <sub>H</sub>
MB90F345E	Embedded 4 Mbits Flash Memory	F80001 <sub>H</sub>

### 17. Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

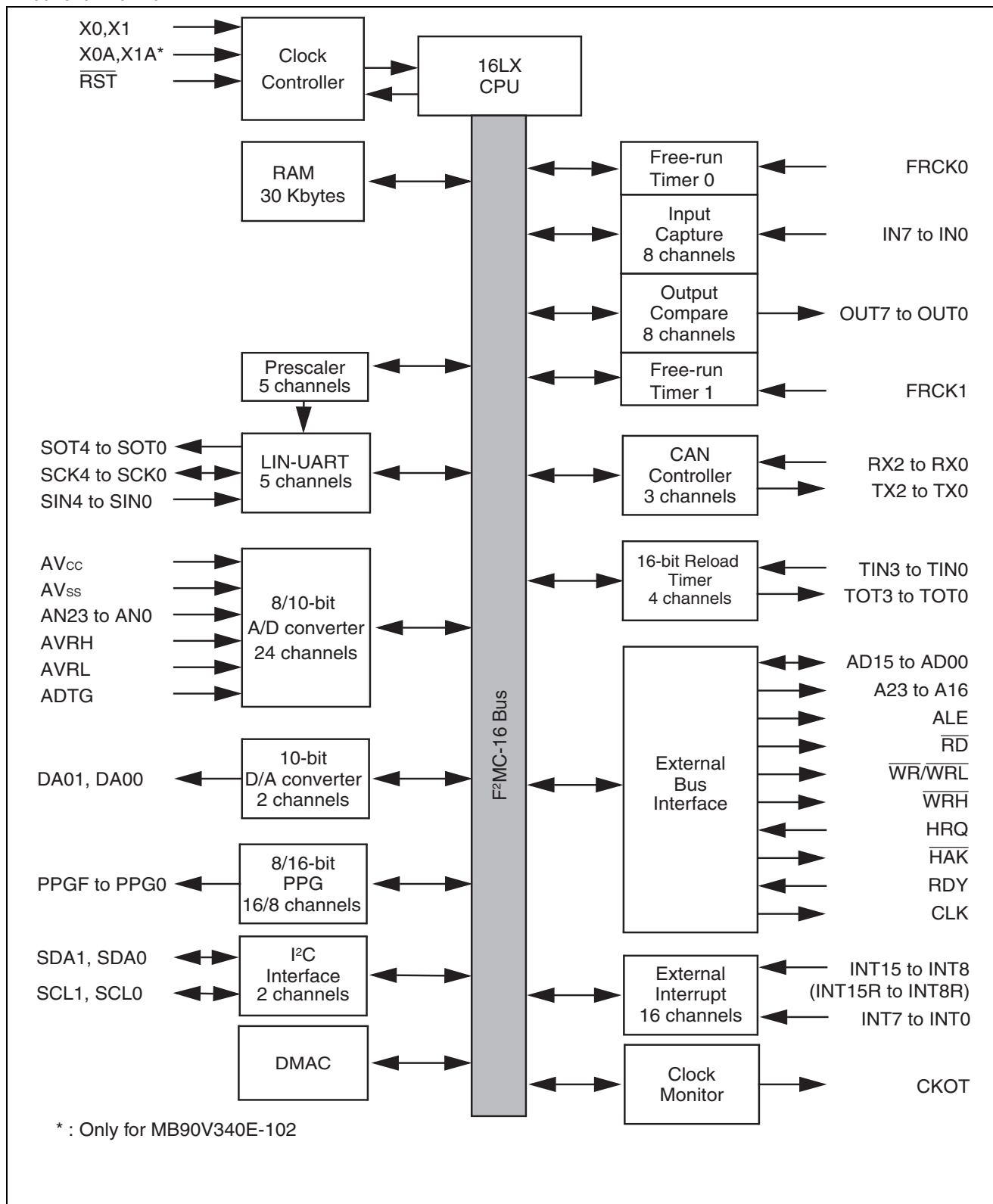
Therefore, design a printed circuit board so as to avoid noise.

Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

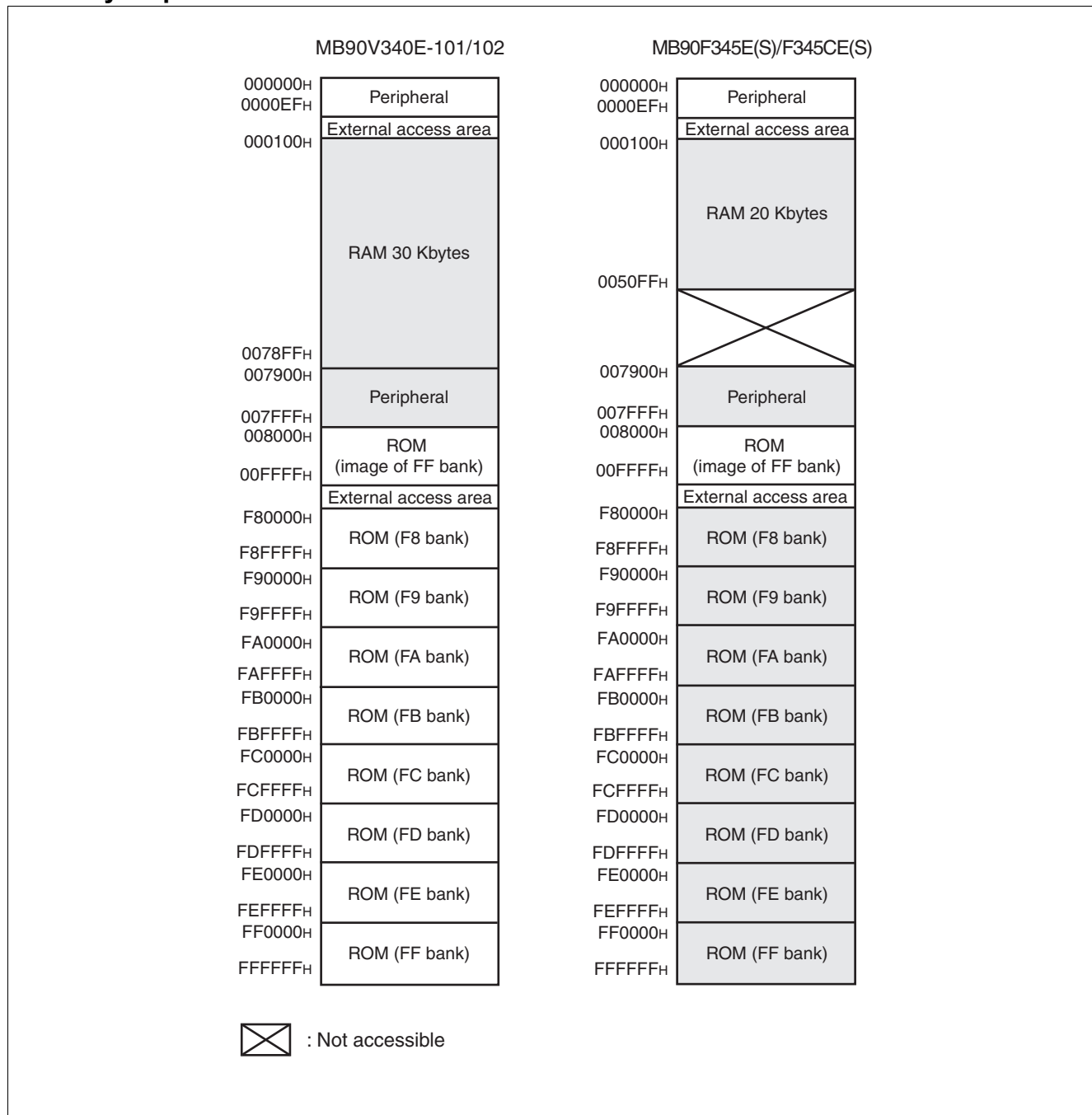


## 6. Block Diagrams

### ■ MB90V340E-101/102



## 7. Memory Map



Address	Register	Abbreviation	Access	Resource name	Initial value
0000A5 <sub>H</sub>	Automatic Ready Function Select Register	ARSR	W	External Memory Access	0011XX00 <sub>B</sub>
0000A6 <sub>H</sub>	External Address Output Control Register	HACR	W		00000000 <sub>B</sub>
0000A7 <sub>H</sub>	Bus Control Signal Selection Register	ECSR	W		0000000X <sub>B</sub>
0000A8 <sub>H</sub>	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXXX11 <sub>B</sub>
0000A9 <sub>H</sub>	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	1XX00100 <sub>B</sub>
0000AA <sub>H</sub>	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 <sub>B</sub>
0000AB <sub>H</sub>	Reserved				
0000AC <sub>H</sub>	DMA Enable L Register	DERL	R/W	DMA	00000000 <sub>B</sub>
0000AD <sub>H</sub>	DMA Enable H Register	DERH	R/W		00000000 <sub>B</sub>
0000AE <sub>H</sub>	Flash Control Status Register (Flash memory devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000 <sub>B</sub>
0000AF <sub>H</sub>	Reserved				
0000B0 <sub>H</sub>	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111 <sub>B</sub>
0000B1 <sub>H</sub>	Interrupt Control Register 01	ICR01	W,R/W		00000111 <sub>B</sub>
0000B2 <sub>H</sub>	Interrupt Control Register 02	ICR02	W,R/W		00000111 <sub>B</sub>
0000B3 <sub>H</sub>	Interrupt Control Register 03	ICR03	W,R/W		00000111 <sub>B</sub>
0000B4 <sub>H</sub>	Interrupt Control Register 04	ICR04	W,R/W		00000111 <sub>B</sub>
0000B5 <sub>H</sub>	Interrupt Control Register 05	ICR05	W,R/W		00000111 <sub>B</sub>
0000B6 <sub>H</sub>	Interrupt Control Register 06	ICR06	W,R/W		00000111 <sub>B</sub>
0000B7 <sub>H</sub>	Interrupt Control Register 07	ICR07	W,R/W		00000111 <sub>B</sub>
0000B8 <sub>H</sub>	Interrupt Control Register 08	ICR08	W,R/W		00000111 <sub>B</sub>
0000B9 <sub>H</sub>	Interrupt Control Register 09	ICR09	W,R/W		00000111 <sub>B</sub>
0000BA <sub>H</sub>	Interrupt Control Register 10	ICR10	W,R/W		00000111 <sub>B</sub>
0000BB <sub>H</sub>	Interrupt Control Register 11	ICR11	W,R/W		00000111 <sub>B</sub>
0000BC <sub>H</sub>	Interrupt Control Register 12	ICR12	W,R/W		00000111 <sub>B</sub>
0000BD <sub>H</sub>	Interrupt Control Register 13	ICR13	W,R/W		00000111 <sub>B</sub>
0000BE <sub>H</sub>	Interrupt Control Register 14	ICR14	W,R/W		00000111 <sub>B</sub>
0000BF <sub>H</sub>	Interrupt Control Register 15	ICR15	W,R/W		00000111 <sub>B</sub>
0000C0 <sub>H</sub>	D/A Converter Data 0	DAT0	R/W	D/A Converter	XXXXXXXX <sub>B</sub>
0000C1 <sub>H</sub>	D/A Converter Data 1	DAT1	R/W		XXXXXXXX <sub>B</sub>
0000C2 <sub>H</sub>	D/A Control 0	DACR0	R/W		XXXXXXXX0 <sub>B</sub>
0000C3 <sub>H</sub>	D/A Control 1	DACR1	R/W		XXXXXXXX0 <sub>B</sub>

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
0000C4 <sub>H</sub> , 0000C5 <sub>H</sub>	Reserved				
0000C6 <sub>H</sub>	External Interrupt Enable 0	ENIR0	R/W	External Interrupt 0	00000000 <sub>B</sub>
0000C7 <sub>H</sub>	External Interrupt Source 0	EIRR0	R/W		XXXXXXXX <sub>B</sub>
0000C8 <sub>H</sub>	External Interrupt Level Setting 0	ELVR0	R/W		00000000 <sub>B</sub>
0000C9 <sub>H</sub>	External Interrupt Level Setting 0	ELVR0	R/W		00000000 <sub>B</sub>
0000CA <sub>H</sub>	External Interrupt Enable 1	ENIR1	R/W	External Interrupt 1	00000000 <sub>B</sub>
0000CB <sub>H</sub>	External Interrupt Source 1	EIRR1	R/W		XXXXXXXX <sub>B</sub>
0000CC <sub>H</sub>	External Interrupt Level Setting 1	ELVR1	R/W		00000000 <sub>B</sub>
0000CD <sub>H</sub>	External Interrupt Level Setting 1	ELVR1	R/W		00000000 <sub>B</sub>
0000CE <sub>H</sub>	External Interrupt Source Select	EISSR	R/W		00000000 <sub>B</sub>
0000CF <sub>H</sub>	PLL/Sub clock Control Register	PSCCR	W	PLL	XXXX0000 <sub>B</sub>
0000D0 <sub>H</sub>	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	XXXXXXXX <sub>B</sub>
0000D1 <sub>H</sub>	DMA Buffer Address Pointer M Register	BAPM	R/W		XXXXXXXX <sub>B</sub>
0000D2 <sub>H</sub>	DMA Buffer Address Pointer H Register	BAPH	R/W		XXXXXXXX <sub>B</sub>
0000D3 <sub>H</sub>	DMA Control Register	DMACS	R/W		XXXXXXXX <sub>B</sub>
0000D4 <sub>H</sub>	I/O Register Address Pointer L Register	IOAL	R/W		XXXXXXXX <sub>B</sub>
0000D5 <sub>H</sub>	I/O Register Address Pointer H Register	IOAH	R/W		XXXXXXXX <sub>B</sub>
0000D6 <sub>H</sub>	Data Counter L Register	DCTL	R/W		XXXXXXXX <sub>B</sub>
0000D7 <sub>H</sub>	Data Counter H Register	DCTH	R/W		XXXXXXXX <sub>B</sub>
0000D8 <sub>H</sub>	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000 <sub>B</sub>
0000D9 <sub>H</sub>	Serial Control Register 2	SCR2	W,R/W		00000000 <sub>B</sub>
0000DA <sub>H</sub>	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000 <sub>B</sub>
0000DB <sub>H</sub>	Serial Status Register 2	SSR2	R,R/W		00001000 <sub>B</sub>
0000DC <sub>H</sub>	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XX <sub>B</sub>
0000DD <sub>H</sub>	Extended Status Control Register 2	ESCR2	R/W		00000100 <sub>B</sub>
0000DE <sub>H</sub>	Baud Rate Generator Register 20	BGR20	R/W		00000000 <sub>B</sub>
0000DF <sub>H</sub>	Baud Rate Generator Register 21	BGR21	R/W		00000000 <sub>B</sub>
0000E0 <sub>H</sub> to 0000EF <sub>H</sub>	Reserved for CAN Controller 2. Refer to “CAN Controllers”				
0000F0 <sub>H</sub> to 0000FF <sub>H</sub>	External				

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## List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007AF0 <sub>H</sub> to 007AF7 <sub>H</sub>	007CF0 <sub>H</sub> to 007CF7 <sub>H</sub>	Data Register 14 (8 bytes)	DTR14	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>
007AF8 <sub>H</sub> to 007AFF <sub>H</sub>	007CF8 <sub>H</sub> to 007CFF <sub>H</sub>	Data Register 15 (8 bytes)	DTR15	R/W	XXXXXXXX <sub>B</sub> to XXXXXXXX <sub>B</sub>

### 11.3 DC Characteristics

( $T_A = -40^{\circ}\text{C}$  to  $+105^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5\text{ V} \pm 10\%$ )	$V_{IHS}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	$V_{IHA}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if Automotive input levels are selected
	$V_{IHT}$	—	—	2.0	—	$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected
	$V_{IHS}$	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	$V_{IHI}$	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	$V_{IHR}$	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	$V_{IHM}$	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5\text{ V} \pm 10\%$ )	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	$V_{ILA}$	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if Automotive input levels are selected
	$V_{ILT}$	—	—	$V_{SS} - 0.3$	—	0.8	V	Port inputs if TTL input levels are selected
	$V_{ILS}$	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	$V_{ILI}$	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	$V_{ILR}$	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	$V_{ILM}$	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	$V_{OH}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	$V_{OHI}$	I <sup>2</sup> C current outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	$V_{OL}$	Normal outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Output L voltage	$V_{OLI}$	I <sup>2</sup> C current outputs	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 3.0\text{ mA}$	—	—	0.4	V	

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## 11.4.9 LIN-UART0/1/2/3

■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

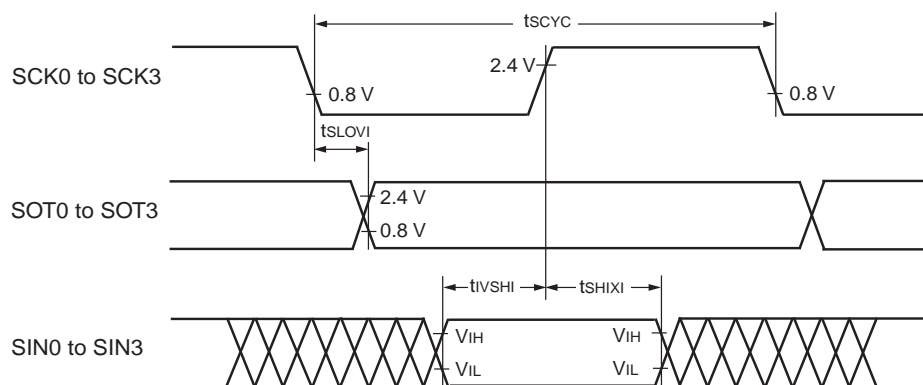
( $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $f_{CP} \leq 24\text{ MHz}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK0 to SCK3	Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$5 t_{CP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOVI}$	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	$t_{IVSHI}$	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	$t_{SHIXI}$	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock "L" pulse width	$t_{SHSL}$	SCK0 to SCK3	External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$ .	$3 t_{CP} - t_R$	—	ns
Serial clock "H" pulse width	$t_{SLSH}$	SCK0 to SCK3		$t_{CP} + 10$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOVE}$	SCK0 to SCK3, SOT0 to SOT3		—	$2 t_{CP} + 60$	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	$t_{IVSHE}$	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	$t_{SHIXE}$	SCK0, SCK1, SIN0 to SIN3		$t_{CP} + 30$	—	ns
SCK fall time	$t_F$	SCK0 to SCK3		—	10	ns
SCK rise time	$t_R$	SCK0 to SCK3		—	10	ns

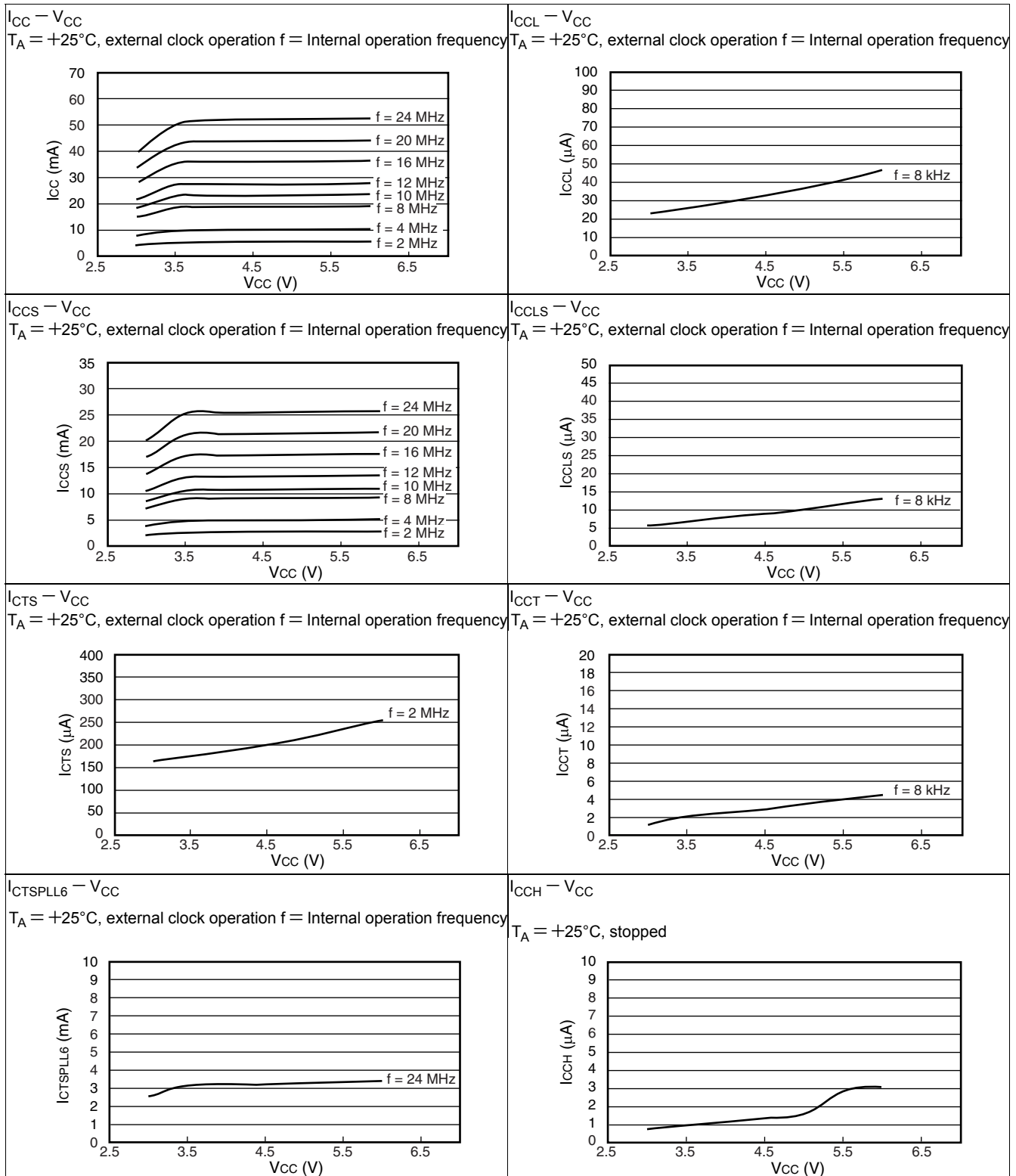
**Note:**

- AC characteristic in CLK synchronized mode.
- $C_L$  is load capacity value of pins when testing.
- $t_{CP}$  is internal operating clock cycle time (machine clock) . Refer to “(1) Clock Timing”.

### • Internal Shift Clock Mode

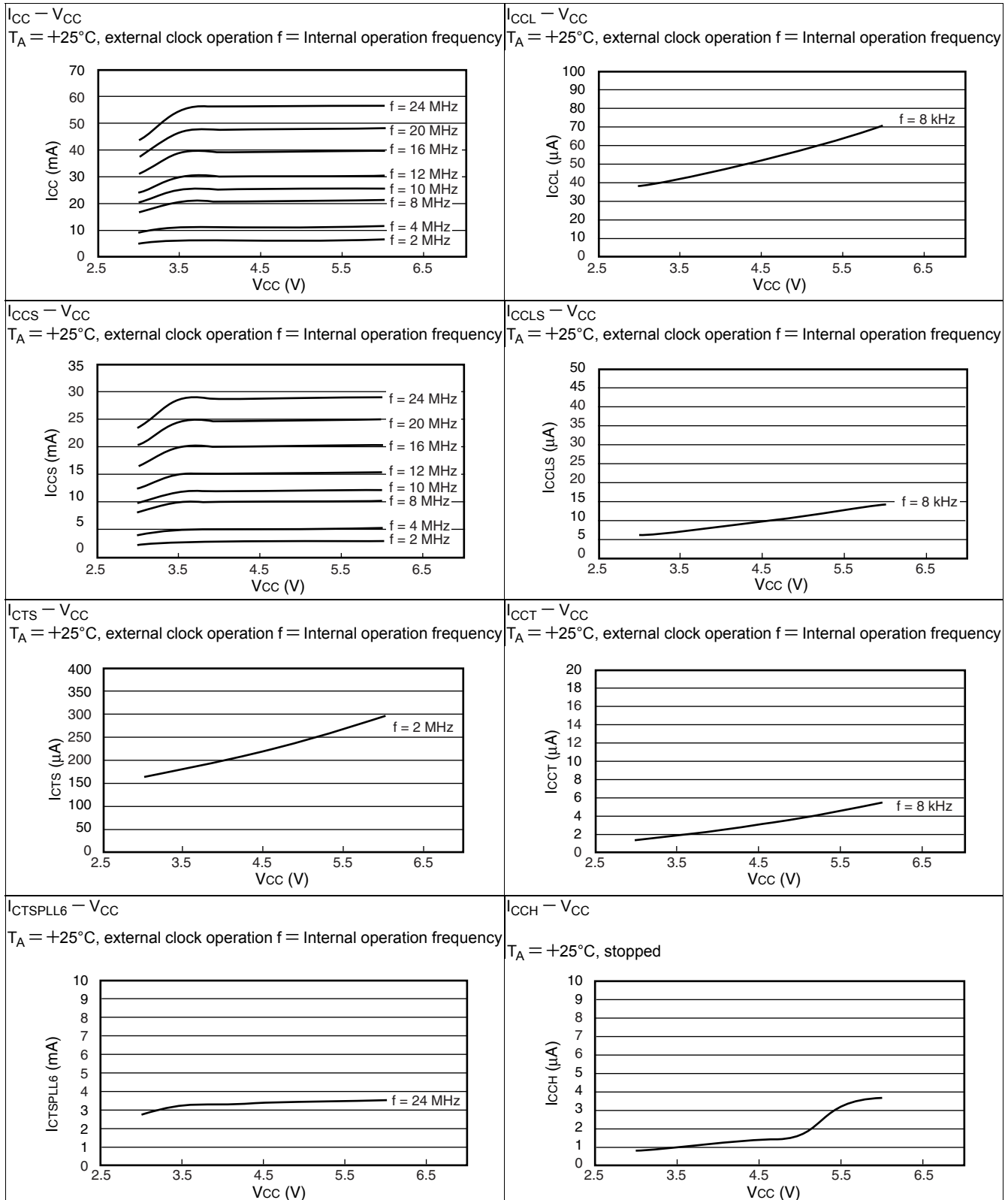


■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES

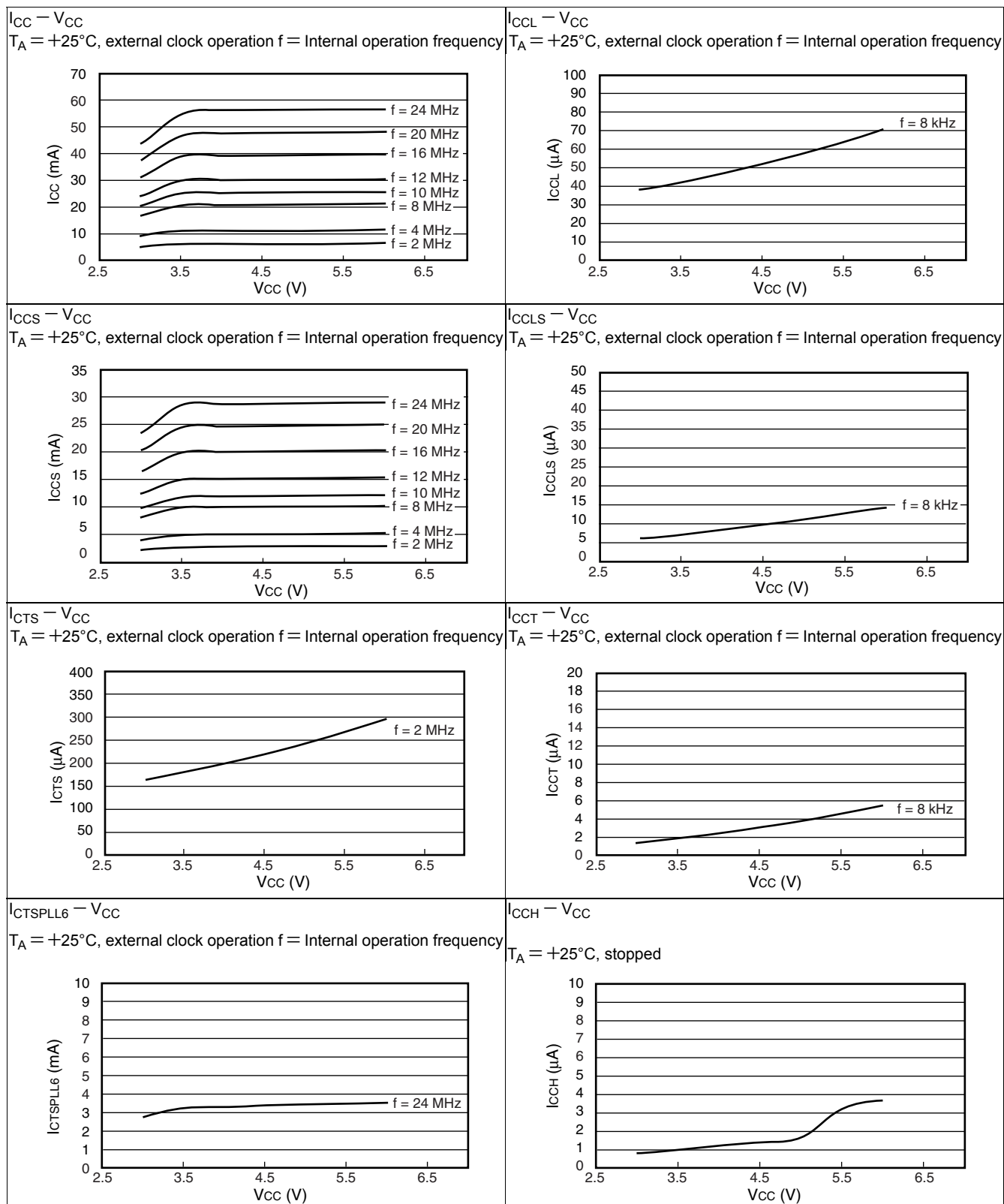




■ MB90F349E, MB90F349ES, MB90F349CE, MB90F349CES

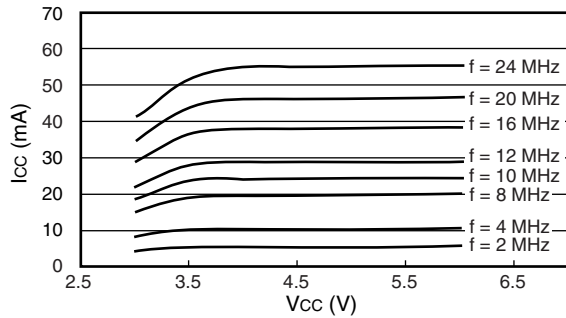


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

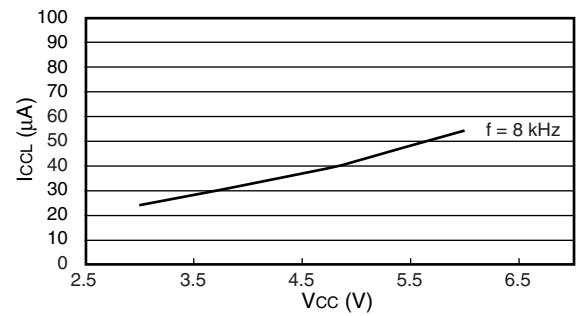


■ MB90346E, MB90346ES, MB90346CE, MB90346CES

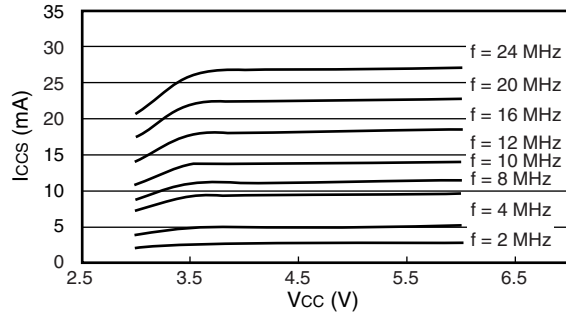
$I_{CC} - V_{CC}$   
 $T_A = +25^\circ\text{C}$ , external clock operation  $f$  = Internal operation frequency



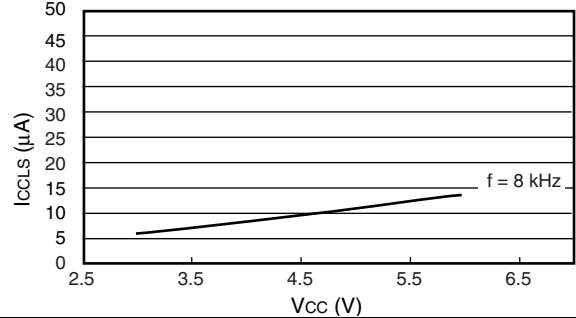
$I_{CCL} - V_{CC}$   
 $T_A = +25^\circ\text{C}$ , external clock operation  $f$  = Internal operation frequency



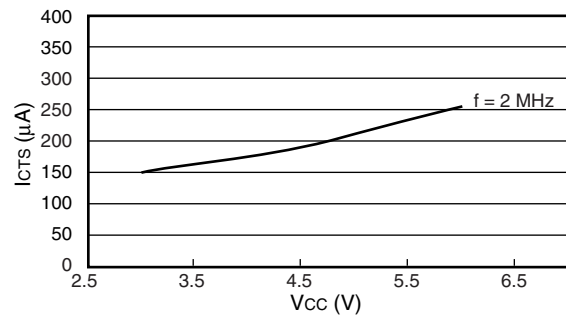
$I_{CCS} - V_{CC}$   
 $T_A = +25^\circ\text{C}$ , external clock operation  $f$  = Internal operation frequency



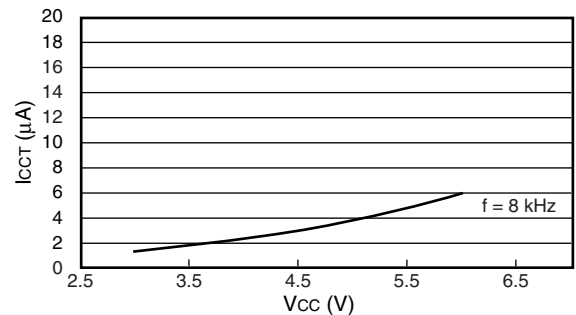
$I_{CCLS} - V_{CC}$   
 $T_A = +25^\circ\text{C}$ , external clock operation  $f$  = Internal operation frequency



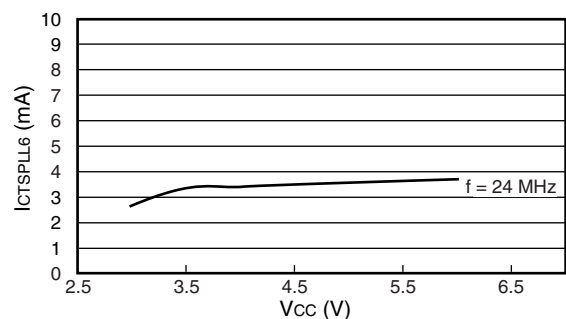
$I_{CTS} - V_{CC}$   
 $T_A = +25^\circ\text{C}$ , external clock operation  $f$  = Internal operation frequency



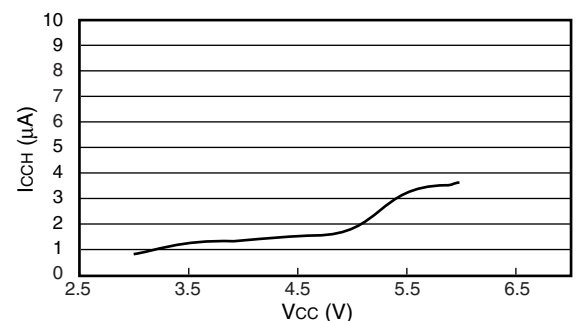
$I_{CCT} - V_{CC}$   
 $T_A = +25^\circ\text{C}$ , external clock operation  $f$  = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$   
 $T_A = +25^\circ\text{C}$ , external clock operation  $f$  = Internal operation frequency



$I_{CCH} - V_{CC}$   
 $T_A = +25^\circ\text{C}$ , stopped



## 15. Major Changes

Spanision Publication Number: DS07-13747-4E

Page	Section	Change Results
—	—	Deleted the part numbers; MB90F343E(S), MB90F343CE(S)
51	Electrical Characteristics Absolute Maximum Ratings	Added “*6” in remark for “L” level maximum output current and “H” level maximum output current. Added “*7” in remark for “L” level average output current and “H” level average output current. Added “*8” in remark for “L” level average overall output current and “H” level average overall output current.
52		Added as follows. “*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.” “*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.” “*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.”

**NOTE:** Please see “Document History” about later revised information.

## Document History

Document Title: MB90340E Series F2MC-16LX 16-bit Microcontroller Datasheet Document Number: 002-04498				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	08/23/2010	Migrated to Cypress and assigned document number 002-04498. No change to document contents or format.
*A	5221535	AKIH	05/04/2016	Updated to Cypress template

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