Infineon Technologies - MB90347ESPMC-GS-698E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-698e1

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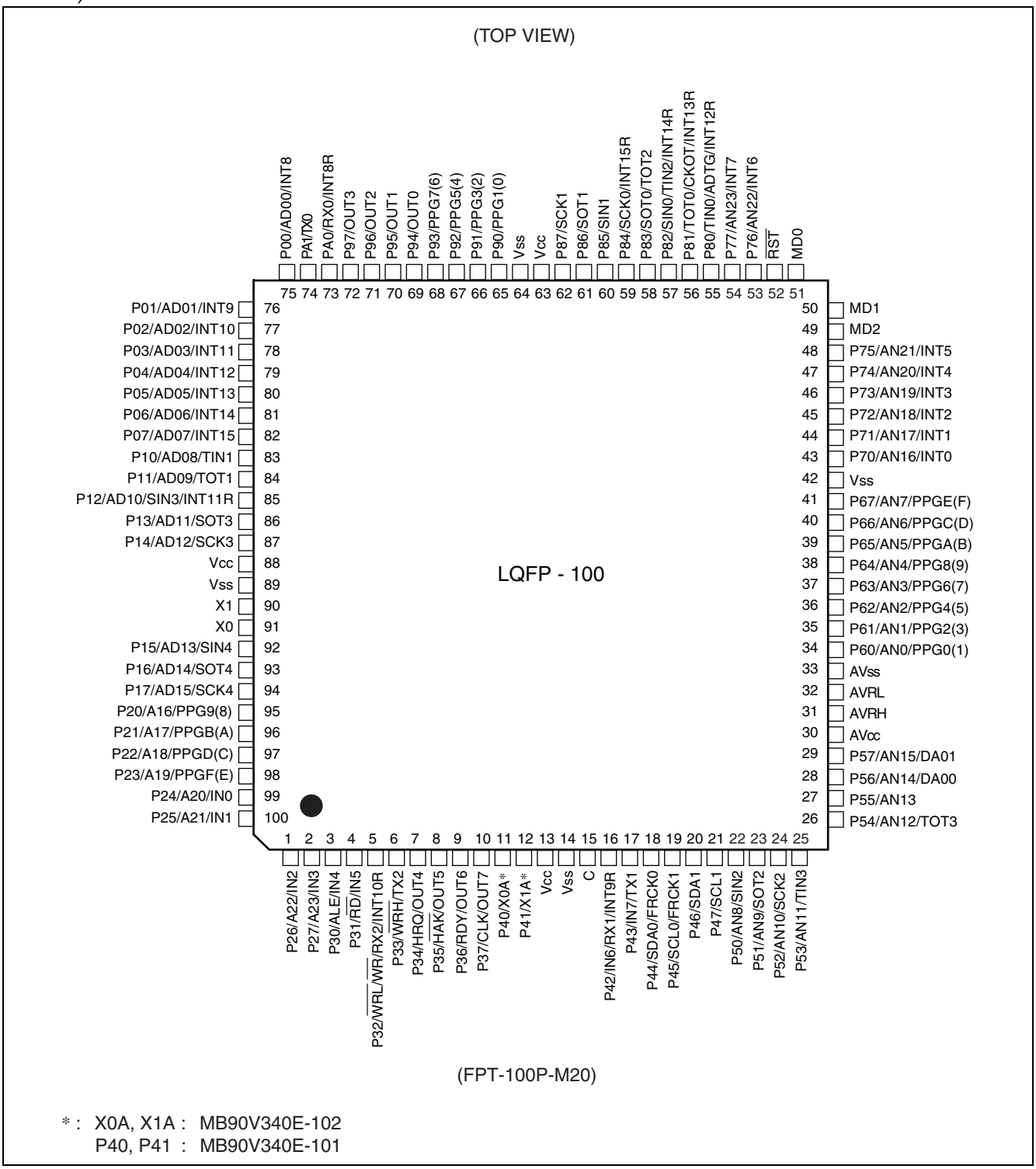

This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

3. Pin Description

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
1 to 4	99 to 2	P24 to P27	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Trigger input pins for input captures.
5	3	P30	G	General purpose I/O pin.The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Trigger input pin for input capture.
6	4	P31	G	General purpose I/O pin.The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		$\overline{RD}$		External read strobe output pin. This function is enabled when the external bus is enabled.
		IN5		Trigger input pin for input capture.
7	5	P32	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the WR/WRL pin output is disabled.
		$\overline{WR}$ / $\overline{WRL}$		Write strobe output pin for the external data bus. This function is enabled when both the external bus and the WR/WRL pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
		INT10R		External interrupt request input pin.
8	6	P33	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or when the WRH pin output is disabled.
		$\overline{WRH}$		Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.

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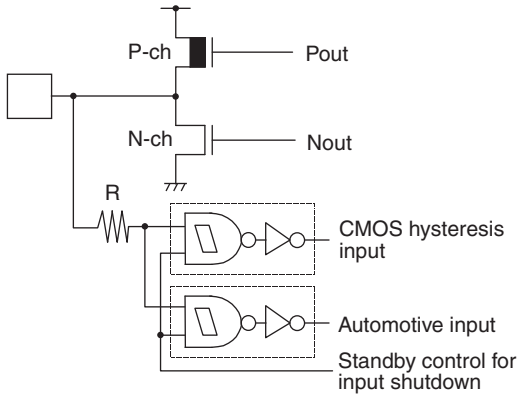
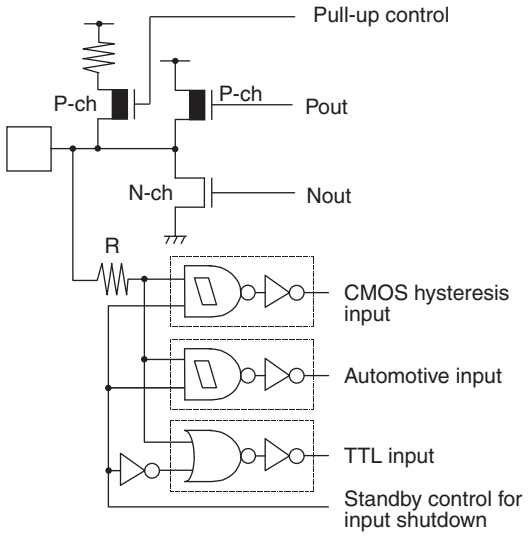
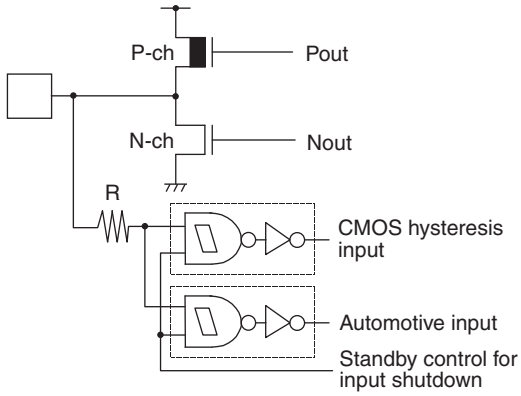
Type	Circuit	Remarks
F		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
G		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) ■ Programmable pull-up resistor: 50 kΩ approx.
H		■ CMOS level output (I_{OL} = 3 mA, I_{OH} = –3 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)

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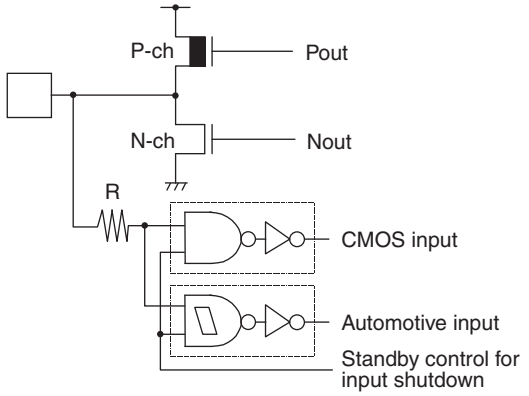
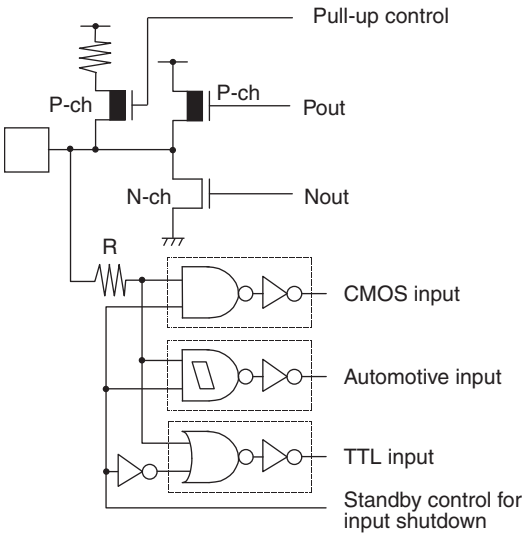
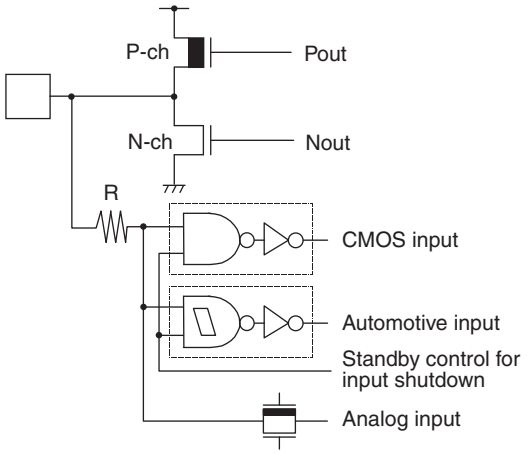
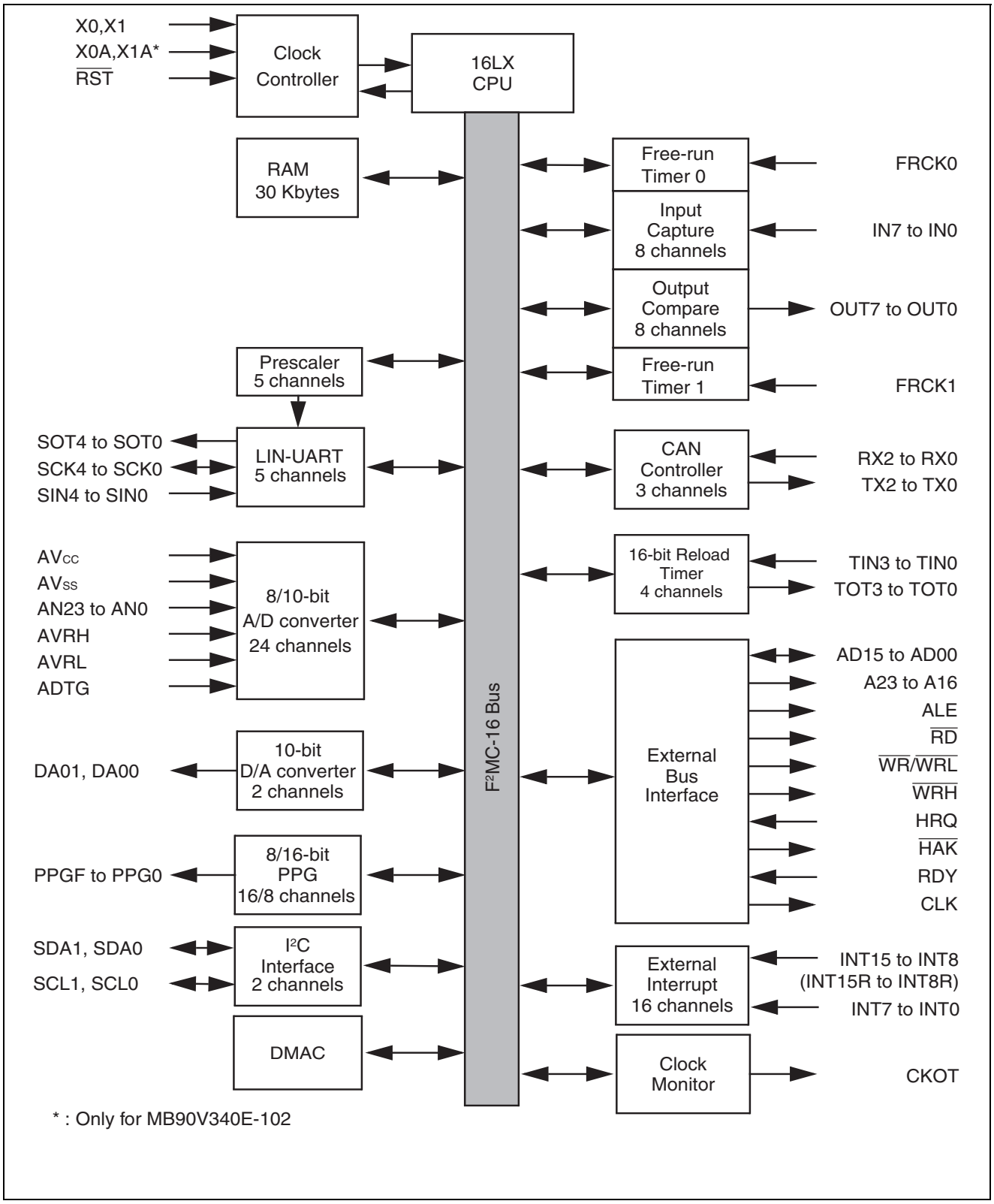
Type	Circuit	Remarks
M		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
N		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) Programmable pull-up resistor: 50 kΩ approx
O		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input

6. Block Diagrams

- MB90V340E-101/102



Address	Register	Abbreviation	Access	Resource name	Initial value
007970_H	I^2C Bus Status Register 0	IBSR0	R	I^2C Interface 0	00000000_B
007971_H	I^2C Bus Control Register 0	IBCR0	W,R/W		00000000_B
007972_H	I^2C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000_B
007973_H		ITBAH0	R/W		00000000_B
007974_H	I^2C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111_B
007975_H		ITMKH0	R/W		00111111_B
007976_H	I^2C 7-bit Slave Address Register 0	ISBA0	R/W		00000000_B
007977_H	I^2C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111_B
007978_H	I^2C Data Register 0	IDAR0	R/W		00000000_B
007979_H, $00797A_H$	Reserved				
$00797B_H$	I^2C Clock Control Register 0	ICCR0	R/W	I^2C Interface 0	00011111_B
$00797C_H$ to $00797F_H$	Reserved				
007980_H	I^2C Bus Status Register 1	IBSR1	R	I^2C Interface 1	00000000_B
007981_H	I^2C Bus Control Register 1	IBCR1	W,R/W		00000000_B
007982_H	I^2C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000_B
007983_H		ITBAH1	R/W		00000000_B
007984_H	I^2C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111_B
007985_H		ITMKH1	R/W		00111111_B
007986_H	I^2C 7-bit Slave Address Register 1	ISBA1	R/W		00000000_B
007987_H	I^2C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111_B
007988_H	I^2C Data Register 1	IDAR1	R/W		00000000_B
007989_H, $00798A_H$	Reserved				
$00798B_H$	I^2C Clock Control Register 1	ICCR1	R/W	I^2C Interface 1	00011111_B
$00798C_H$ to $0079C1_H$	Reserved				
$0079C2_H$	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	$0001X000_B$
$0079C3_H$ to $0079DF_H$	Reserved				

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9. CAN Controllers

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
- Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
- 29-bit ID and 8-byte data
- Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
- Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers (1)

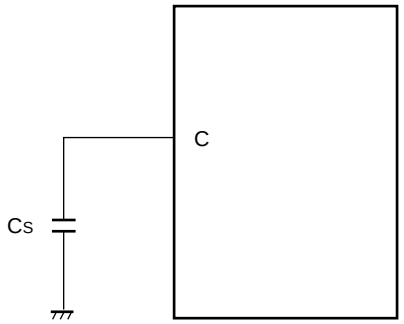
Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070_H	000080_H	Message Buffer Valid Register	BVALR	R/W	00000000_B 00000000_B
000071_H	000081_H				
000072_H	000082_H	Transmit Request Register	TREQR	R/W	00000000_B 00000000_B
000073_H	000083_H				
000074_H	000084_H	Transmit Cancel Register	TCANR	W	00000000_B 00000000_B
000075_H	000085_H				
000076_H	000086_H	Transmission Complete Register	TCR	R/W	00000000_B 00000000_B
000077_H	000087_H				
000078_H	000088_H	Receive Complete Register	RCR	R/W	00000000_B 00000000_B
000079_H	000089_H				
$00007A_H$	$00008A_H$	Remote Request Receiving Register	RRTRR	R/W	00000000_B 00000000_B
$00007B_H$	$00008B_H$				
$00007C_H$	$00008C_H$	Receive Overrun Register	ROVRR	R/W	00000000_B 00000000_B
$00007D_H$	$00008D_H$				
$00007E_H$	$00008E_H$	Reception Interrupt Enable Register	RIER	R/W	00000000_B 00000000_B
$00007F_H$	$00008F_H$				

11.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.
Operating temperature	T_A	−40	—	+105	°C	

C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

11.4 AC Characteristics

11.4.1 Clock Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP}≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

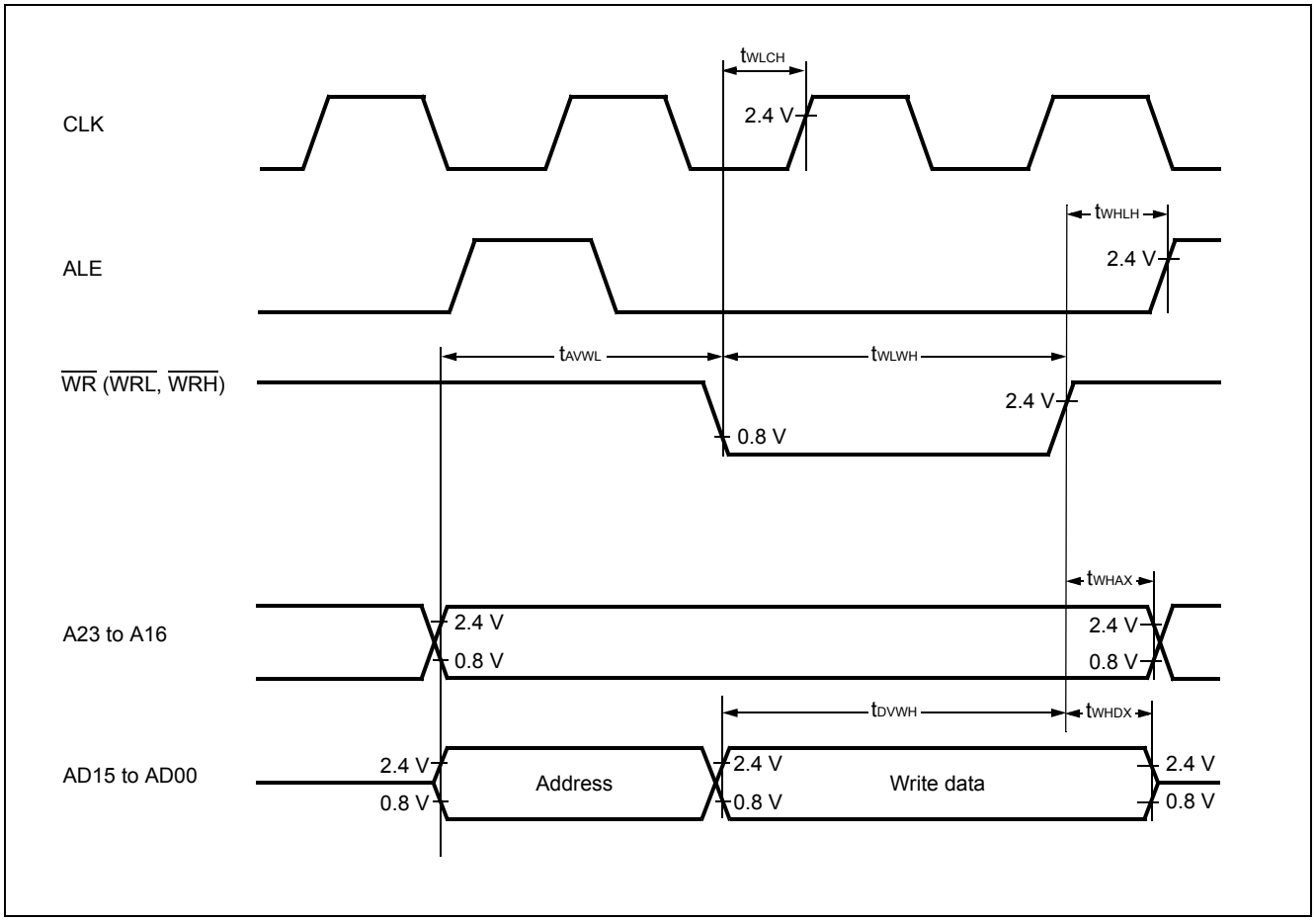
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	When using an oscillation circuit
			4	—	16	MHz	PLL multiplied by 1 When using an oscillation circuit
			4	—	12	MHz	PLL multiplied by 2 When using an oscillation circuit
			4	—	8	MHz	PLL multiplied by 3 When using an oscillation circuit
			4	—	6	MHz	PLL multiplied by 4 When using an oscillation circuit
			—	—	4	MHz	PLL multiplied by 6 When using an oscillation circuit
			3	—	24	MHz	When using an external clock*
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	µs	When using sub clock

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in “Relation between the external clock frequency and machine clock frequency”.

11.4.6 Bus Timing (Write)

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{WR}$	—	t_{CP}−15	—	ns
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		3 t_{CP}/2 − 20	—	ns
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		3 t_{CP}/2 − 20	—	ns
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	—	ns
$\overline{WR}$ ↑ → Address valid time	t_{WHAX}	A23 to A16, $\overline{WR}$		t_{CP}/2 − 10	—	ns
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 − 15	—	ns
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 − 15	—	ns

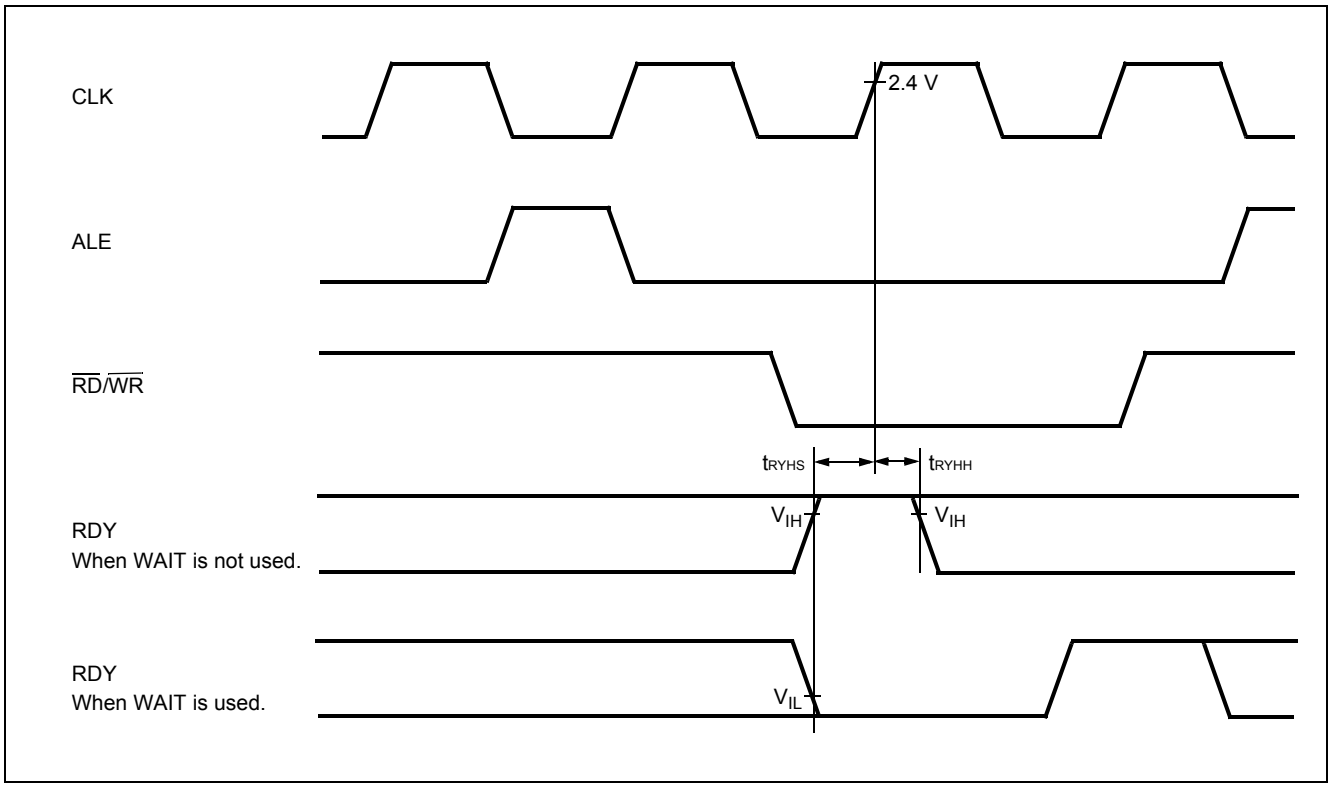


11.4.7 Ready Input Timing

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Test Condition	Rated Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	f_{CP} = 16 MHz
				32	—	ns	f_{CP} = 24 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note: : If the RDY setup time is insufficient, use the auto-ready function.



11.4.9 LIN-UART0/1/2/3

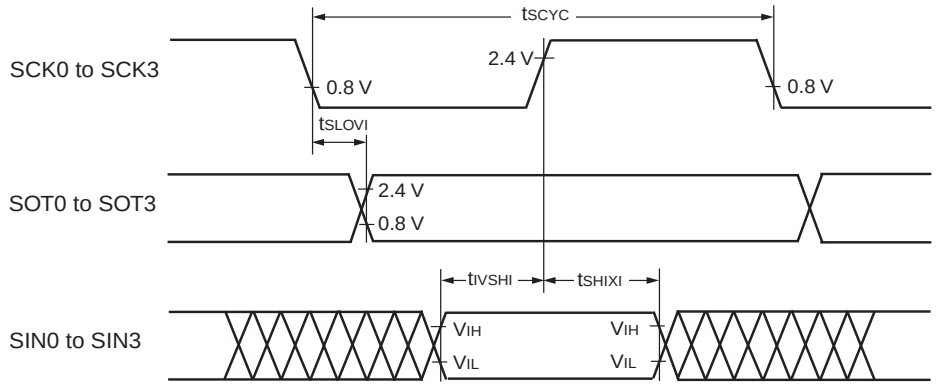
■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0**

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		−50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock “L” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “H” pulse width	t_{SLSH}	SCK0 to SCK3		t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SIN0 to SIN3		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

Note:
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

- Internal Shift Clock Mode



11.8 Flash Memory Program/Erase Characteristics

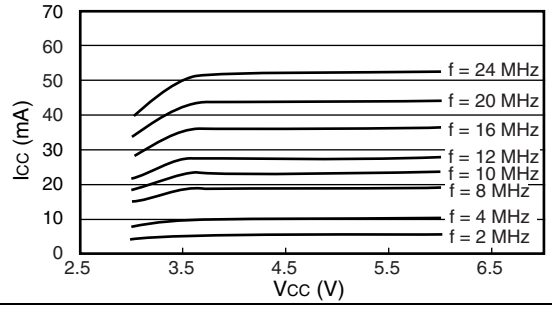
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25°C$ $V_{CC} = 5.0$ V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	µs	Except for the over head time of the system
Program/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average $T_A = +85°C$	20	—	—	year	*

* : This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85°C) .

■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES

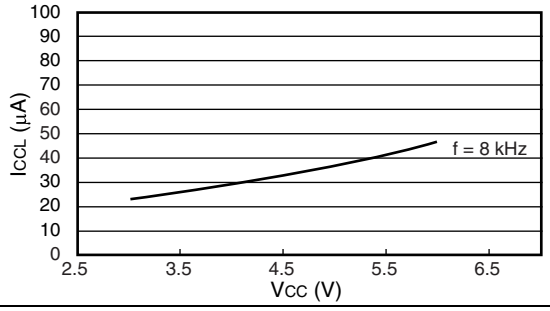
$I_{CC} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



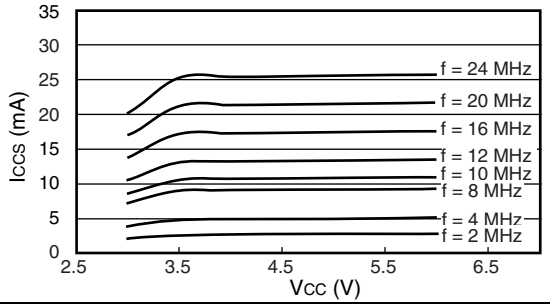
$I_{CCL} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



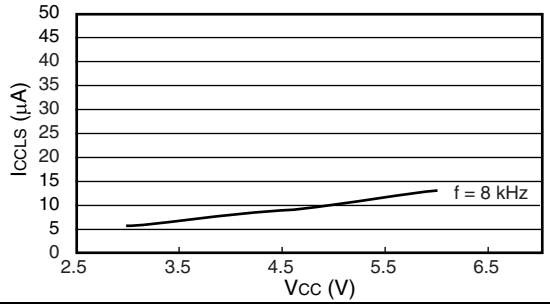
$I_{CCS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



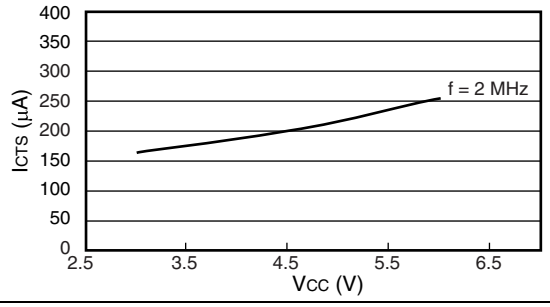
$I_{CCLS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



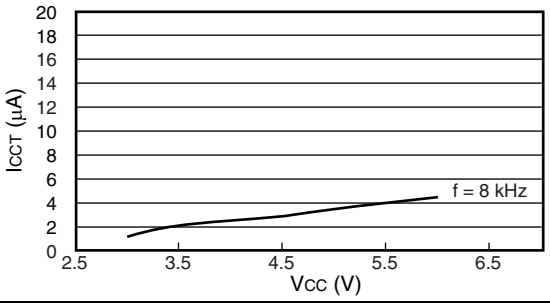
$I_{CTS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



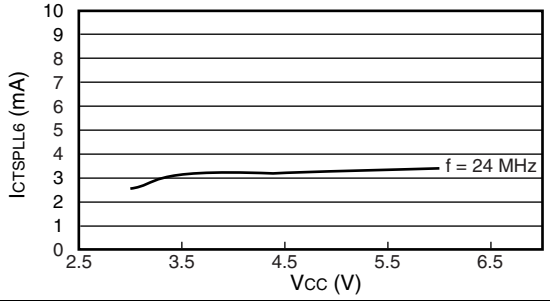
$I_{CCT} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



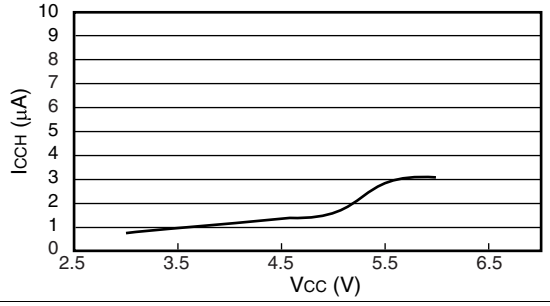
$I_{CTSPLL6} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



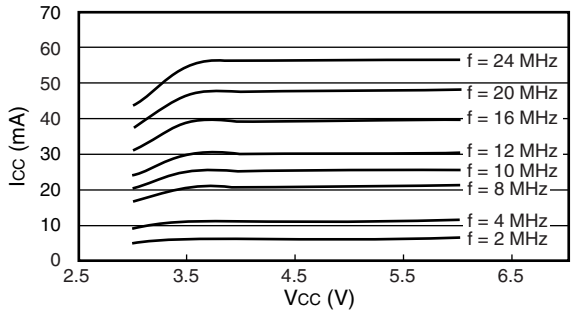
$I_{CCH} - V_{CC}$

$T_A = +25°C$, stopped

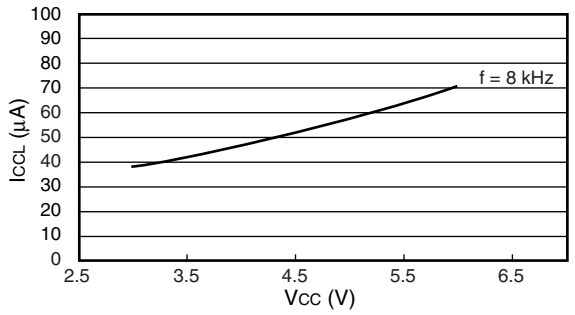


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

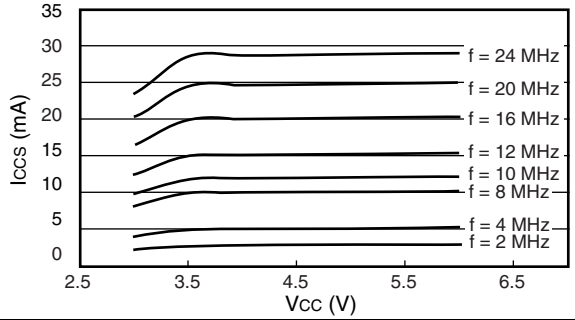
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



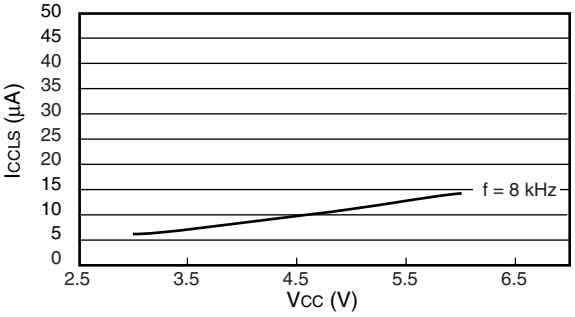
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



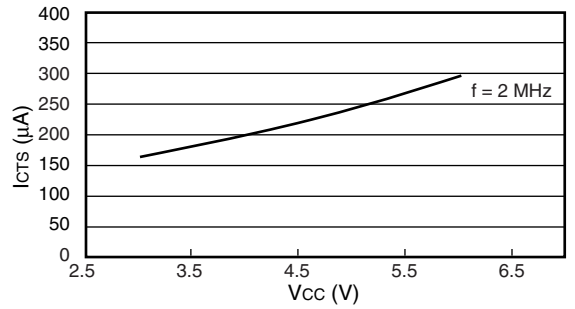
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



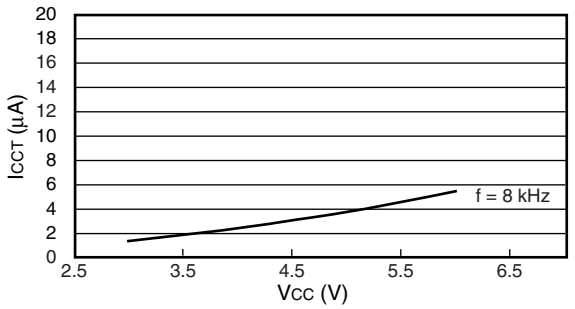
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



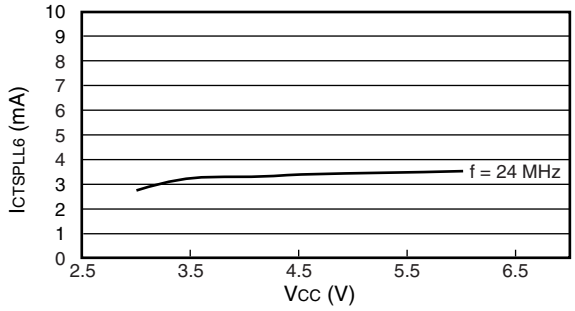
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



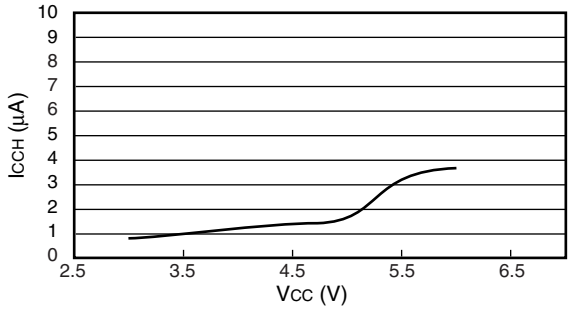
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency

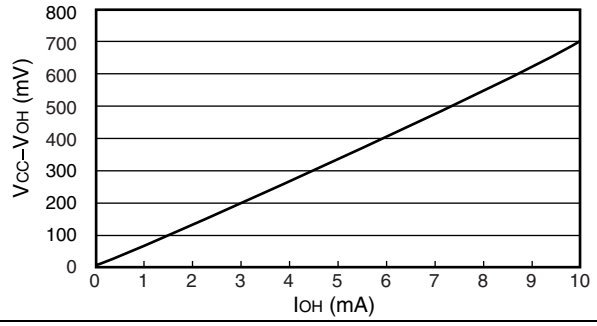


$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

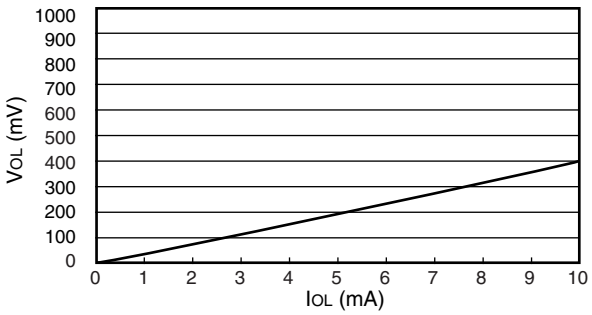


■ I/O characteristics

$(V_{CC}-V_{OH})$ – I_{OH}
T_A = +25°C, V_{CC} = 4.5 V

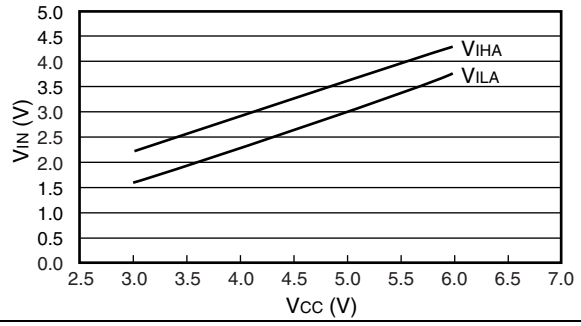


V_{OL} – I_{OL}
T_A = +25°C, V_{CC} = 4.5 V

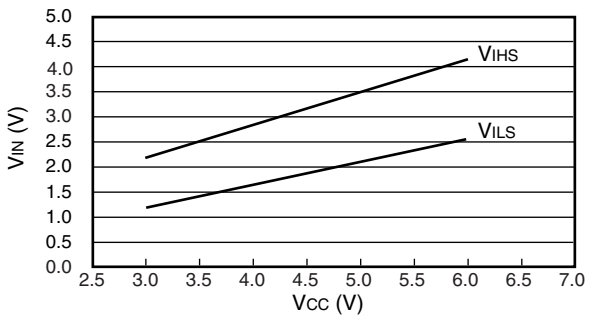


Automotive V_{IN} – V_{CC}

T_A = +25°C

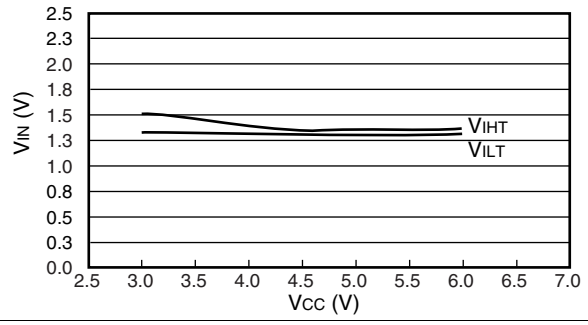


CMOS V_{IN} – V_{CC}
Other than UART-SIN pin and I^2C pin
T_A = +25°C

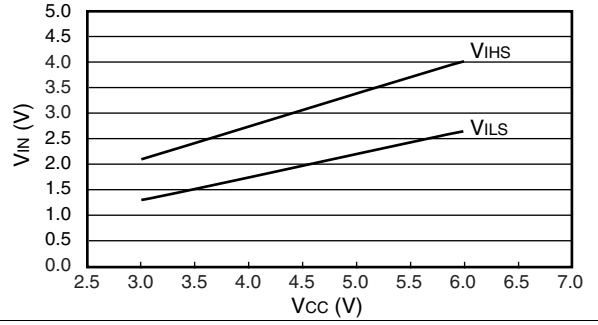


TTL V_{IN} – V_{CC}

T_A = +25°C



CMOS V_{IN} – V_{CC}
UART-SIN pin, I^2C pin
T_A = +25°C



(Continued)

Part number	Package	Remarks
MB90346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90346ESPF		
MB90346CEPF		
MB90346CESPF		
MB90346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90346ESPMC		
MB90346CEPMC		
MB90346CESPMC		
MB90347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90347ESPF		
MB90347CEPF		
MB90347CESPF		
MB90347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90347ESPMC		
MB90347CEPMC		
MB90347CESPMC		
MB90348EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90348ESPF		
MB90348CEPF		
MB90348CESPF		
MB90348EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90348ESPMC		
MB90348CEPMC		
MB90348CESPMC		
MB90349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90349ESPF		
MB90349CEPF		
MB90349CESPF		
MB90349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90349ESPMC		
MB90349CEPMC		
MB90349CESPMC		
MB90V340E-101CR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation
MB90V340E-102CR		

15. Major Changes

Spansiion Publication Number: DS07-13747-4E

Page	Section	Change Results
___	___	Deleted the part numbers; MB90F343E(S), MB90F343CE(S)
51	Electrical Characteristics Absolute Maximum Ratings	Added “*6” in remark for “L" level maximum output current and “H” level maximum output current. Added “*7” in remark for “L" level average output current and “H” level average output current. Added “*8” in remark for “L"level average overall output current and “H” level average overall output current.
52		Added as follows. “*6:The maximum output current is defined as the peak value of the current of any one of the corresponding pins.” “*7:The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.” “*8:The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.”

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90340E Series F2MC-16LX 16-bit Microcontroller Datasheet Document Number: 002-04498				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	08/23/2010	Migrated to Cypress and assigned document number 002-04498. No change to document contents or format.
*A	5221535	AKIH	05/04/2016	Updated to Cypress template

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