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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90347espmc-gs-698e1

Email: info@E-XFL.COM

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MB90340E Series

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This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.



3. Pin Description

Pin No.			I/O	-				
QFP100* ¹	LQFP100* ²	Pin name	type*3	Function				
1 to 4 99 to 2		P24 to P27		General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.				
1 to 4	99 to 2	A20 to A23	G	Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).				
		IN0 to IN3		Trigger input pins for input captures.				
		P30		General purpose I/O pin.The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.				
5 3		ALE	G	Address latch enable output pin. This function is enabled when the external bu is enabled.				
	IN4			Trigger input pin for input capture.				
		P31	G	General purpose I/O pin.The register can be set to select whether to use a pull-up resistor.				
6	4			This function is enabled in single-chip mode.				
0		RD		External read strobe output pin. This function is enabled when the external bus is enabled.				
	IN5		Trigger input pin for input capture.					
	F			General purpose I/O pin. The register can be set to select whether to use a <u>pull-up re</u> sistor. This function is enabled either in single-chip mode or when the WR/WRL pin output is disabled.				
7 5	5	WR / WRL	G	Write strobe output pin for the <u>external</u> data bus. This function is <u>enabled</u> when both the external bus and the WR/WRL pin output are enabled. WRL is used to write-strobe 8 lower bits of the data bus in 16-bit access while WR is used to write-strobe 8 bits of the data bus in 8-bit access.				
		INT10R		External interrupt request input pin.				
8	6	P33		General purpose I/O pin. The register can be set to select whether to use a <u>pull-up</u> resistor. This function is enabled either in single-chip mode or when the WRH pin output is disabled.				
5	б	WRH	<u> </u>	Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.				





Туре	Circuit	Remarks
		■ CMOS level output (I _{OL} = 4 mA, I _{OH} = -4 mA)
F	P-ch Pout	 CMOS hysteresis input (with function to disconnect input during standby)
	N-ch Nout	 Automotive input (with function to disconnect input during standby)
F	CMOS hysteresis input	
	Automotive input Standby control for	
	input shutdown	
	Pull-up control	■ CMOS level output (I _{OL} = 4 mA, I _{OH} = -4 mA)
G	P-ch	 CMOS hysteresis input (with function to disconnect input during standby)
	P-ch P-ch Pout	 Automotive input (with function to disconnect input during standby)
	N-ch Nout	 TTL input (with function to disconnect input during standby)
	CMOS hysteresis	 Programmable pull-up resistor: 50 kΩ approx.
	Automotive input	
	TTL input	
	Standby control for input shutdown	
	+	■ CMOS level output (I _{OL} = 3 mA, I _{OH} = -3 mA)
	P-ch Pout	 CMOS hysteresis input (with function to disconnect input during standby)
	N-ch Nout	 Automotive input (with function to disconnect input during standby)
н	R 7/2 CMOS hysteresis input	
	Automotive input	
	Standby control for input shutdown	



MB90340E Series

Туре	Circuit	Remarks
	P-ch Pout	 CMOS level output (I_{OL} = 4 mA, I_{OH} = -4 mA) CMOS input (with function to disconnect input during standby) Automotive input (with function to
Μ	R R CMOS input Automotive input Standby control for input shutdown	disconnect input during standby)
	Pull-up control	CMOS level output ($I_{OL} = 4 \text{ mA}, I_{OH} = -4 \text{ mA}$)
	P-ch Pout	 CMOS input (with function to disconnect input during standby)
		 Automotive input (with function to disconnect input during standby)
Ν	N-ch Nout R CMOS input Automotive input TTL input Standby control for	 TTL input (with function to disconnect input during standby) Programmable pull-up resistor: 50 kΩ approx
	 	CMOS level output (lov = 4 mA lov = -4 mA)
	P-ch Pout	 CMOS input (with function to disconnect input during standby)
	N-ch Nout	 Automotive input (with function to disconnect input during standby)
0	CMOS input	 A/D converter analog input
	Automotive input Standby control for	
	Analog input	



6. Block Diagrams





Address	Register	Abbreviation	Access	Resource name	Initial value
007970 _H	I ² C Bus Status Register 0	IBSR0	R		00000000 _B
007971 _H	I ² C Bus Control Register 0	IBCR0	W,R/W		00000000 _B
007972 _H	1 ² C 10 bit Slove Address Register 0	ITBAL0	R/W		00000000 _B
007973 _H	T-C TO-bit Slave Address Register 0	ITBAH0	R/W		00000000 _B
007974 _H	I ² C 10-bit Slave Address Mask	ITMKL0	R/W	I ² C Interface 0	11111111 _B
007975 _H	Register 0	ITMKH0	R/W	-	00111111 _B
007976 _H	I ² C 7-bit Slave Address Register 0	ISBA0	R/W		00000000 _B
007977 _H	I ² C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111 _B
007978 _H	I ² C Data Register 0	IDAR0	R/W		00000000 _B
007979 _H , 00797A _H	Reserved	·			
00797B _H	I ² C Clock Control Register 0	ICCR0	R/W	I ² C Interface 0	00011111 _B
00797C _H to 00797F _H	Reserved	·			
007980 _H	I ² C Bus Status Register 1	IBSR1	R		00000000 _B
007981 _H	I ² C Bus Control Register 1	IBCR1	W,R/W		00000000 _B
007982 _H	1 ² C 10-bit Slave Address Register 1	ITBAL1	R/W	I ² C Interface 1	00000000 _B
007983 _H	TO TO-DIL SIAVE AUGLESS REGISLEL T	ITBAH1	R/W		00000000 _B
007984 _H	I ² C 10-bit Slave Address Mask	ITMKL1	R/W		11111111 _B
007985 _H	Register 1	ITMKH1	R/W		00111111 _B
007986 _H	I ² C 7-bit Slave Address Register 1	ISBA1	R/W		00000000 _B
007987 _H	I ² C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111 _B
007988 _H	I ² C Data Register 1	IDAR1	R/W		00000000 _B
007989 _H , 00798A _H	Reserved				
00798B _H	I ² C Clock Control Register 1	ICCR1	R/W	I ² C Interface 1	00011111 _B
00798C _H to 0079C1 _H	Reserved				
0079C2 _H	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	0001X000 _B
0079C3 _H to 0079DF _H	Reserved				



9. CAN Controllers

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
- Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
- 29-bit ID and 8-byte data
- Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
- Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers (1)

Address		Pagistar	Abbroviation	Access	Initial Value	
CAN0	CAN1	Register	ADDIEVIATION	ALLESS		
000070 _H	000080 _H	Message Buffer			00000000 _B	
000071 _H	000081 _H	Valid Register	DVALK		00000000B	
000072 _H	000082 _H	Transmit Request			00000000 _B	
000073 _H	000083 _H	Register	INEQN		00000000B	
000074 _H	000084 _H	Transmit Cancel		\ M /	00000000 _B	
000075 _H	000085 _H	Register	ICANK	vv	00000000 ⁻ B	
000076 _H	000086 _H	Transmission	TCP	R/W	00000000 _B	
000077 _H	000087 _H	Complete Register	TOR		00000000 _B	
000078 _H	000088 _H	Receive Complete	PCP	R/W	00000000 _B 00000000 _B	
000079 _H	000089 _H	Register	NON			
00007A _H	00008A _H	Remote Request	DDTDD		00000000 _B	
00007B _H	00008B _H	Receiving Register			00000000 [–]	
00007C _H	00008C _H	Receive Overrun			00000000 _B	
00007D _H	00008D _H	Register	KOWKK		00000000B	
00007E _H	00008E _H	Reception Interrupt	DIED		00000000 _B	
00007F _H	00008F _H	Enable Register		1.7.4.4	00000000B	



11.2 Recommended Operating Conditions

 $(V_{SS} = AV_{SS} = 0 V)$

Paramotor	Symbol	Value			Unit	Bomarka	
Farameter	Min Typ Max		Remarks				
		4.0	5.0	5.5	V	Under normal operation	
Power supply voltage	V _{CC} , AV _{CC}	3.5	5.0	5.5	v	Under normal operation, when not using the A/D converter and not Flash programming.	
		4.5	5.0	5.5	V	When External bus is used.	
		3.0		5.5	V	Maintains RAM data in stop mode	
Smoothing capacitor	C _S	0.1		1.0	μF	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.	
Operating temperature	T _A	-40		+105	°C		



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



11.4 AC Characteristics

11.4.1 Clock Timing

(T_A = -40°C to +105°C, V_{CC} = 5.0 V \pm 10%, f_{CP} \leq 24 MHz, V_{SS} = AV_{SS} = 0 V)

Devementer	Symbol	Din	Value			Unit	Domorko	
Parameter	Symbol	PIN	Min	Тур	Max	Unit	Remarks	
			3		16	MHz	When using an oscillation circuit	
			4		16	MHz	PLL multiplied by 1 When using an oscillation circuit	
			4		12	MHz	PLL multiplied by 2 When using an oscillation circuit	
Clock frequency	f _C	X0, X1	4		8	MHz	PLL multiplied by 3 When using an oscillation circuit	
			4		6	MHz	PLL multiplied by 4 When using an oscillation circuit	
					4	MHz	PLL multiplied by 6 When using an oscillation circuit	
			3	_	24	MHz	When using an external clock*	
	fc∟	X0A, X1A		32.768	100	kHz		
	t	X0, X1	62.5		333	ns	When using an oscillation circuit	
Clock cycle time	^I CYL	X0, X1	41.67		333	ns	When using an external clock	
	tcyll	X0A, X1A	10	30.5	_	μS		
Input clock pulse width	P_{WH}, P_{WL}	X0	10	_	_	ns	Duty ratio is about 20% to 70%	
input clock pulse width	P_{WHL}, P_{WLL}	X0A	5	15.2		μS		
Input clock rise and fall time	t _{CR} , t _{CF}	X0			5	ns	When using external clock	
Internal operating clock	f _{CP}		1.5		24	MHz	When using main clock	
frequency (machine clock)	f _{CPL}	—		8.192	50	kHz	When using sub clock	
Internal operating clock	t _{CP}		41.67		666	ns	When using main clock	
cycle time (machine clock)	t _{CPL}		20	122.1		μS	When using sub clock	

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in "Relation between the external clock frequency and machine clock frequency".



11.4.6 Bus Timing (Write)

(T_A = -40°C to +105°C, V_{CC} = 5.0 V \pm 10%, V_{SS} = 0.0 V, f_{CP} {\leq} 24 MHz)

Baramatar	Symbol	Bin	Condition	Val	Unit	
Falameter	Symbol	FIII	Continuition	Min	Max	Unit
Valid address $\rightarrow \overline{WR} \downarrow$ time	t _{AVWL}	A23 to A1 <u>6, A</u> D15 to AD00, WR		t _{CP} —15		ns
WR pulse width	t _{WLWH}	WR		3 t _{CP} /2 - 20		ns
Valid data output $ ightarrow \overline{WR} \uparrow$ time	t _{DVWH}	AD15 to AD00, WR		3 t _{CP} /2 - 20		ns
\overline{WR} \uparrow $ ightarrow$ Data hold time	t _{WHDX}	AD15 to AD00, WR		15		ns
\overline{WR} \uparrow $ ightarrow$ Address valid time	t _{WHAX}	A23 to A16, WR		t _{CP} /2 - 10		ns
\overline{WR} \uparrow \rightarrow ALE \uparrow time	t _{WHLH}	WR, ALE		t _{CP} /2 - 15		ns
$\overline{WR} \downarrow \rightarrow CLK \uparrow time$	t _{WLCH}	WR, CLK		t _{CP} /2 - 15		ns





11.4.7 Ready Input Timing

(T_A = -40°C to +105°C, V_{CC} = 5.0 V \pm 10%, V_{SS} = 0.0 V, f_{CP} {\leq} 24 MHz)

Paramotor	Symbol Pin		Test	Rated	Value	Unit	Remarks
Falailletei	Symbol	Condition		Min	Max	Unit	
RDY setup time	t _{RYHS}	RDY		45	—	ns	$f_{CP} = 16 \text{ MHz}$
				32	—	ns	$f_{CP} = 24 \text{ MHz}$
RDY hold time	t _{RYHH}	RDY		0		ns	

Note: : If the RDY setup time is insufficient, use the auto-ready function.







11.4.9 LIN-UART0/1/2/3 ■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

(T_A = -40°C to +105°C, V_{CC} = 5.0 V \pm 10%, f_{CP} \leq 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Din	Condition	Value		Unit
Farameter Sym		FIII	Condition	Min	Max	
Serial clock cycle time	t _{SCYC}	SCK0 to SCK3		5 t _{CP}		ns
$SCK \downarrow \to SOT$ delay time	t _{SLOVI}	SCK0 to SCK3, SOT0 to SOT3	Internal shift clock mode output pins are $C_L = 80 \text{ pF} + 1 \text{ TTL}.$	-50	+50	ns
Valid SIN \rightarrow SCK \uparrow	t _{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t _{CP} + 80		ns
$SCK\!\uparrow \to ValidSINholdtime$	t _{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0		ns
Serial clock "L" pulse width	t _{SHSL}	SCK0 to SCK3		3 t _{CP} - t _R	—	ns
Serial clock "H" pulse width	t _{SLSH}	SCK0 to SCK3	External shift clock mode output pins are $C_L = 80 \text{ pF} + 1 \text{ TTL}.$	t _{CP} + 10		ns
$SCK \downarrow \to SOT$ delay time	t _{SLOVE}	SCK0 to SCK3, SOT0 to SOT3			2 t _{CP} + 60	ns
Valid SIN \rightarrow SCK \uparrow	t _{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30		ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t _{SHIXE}	SCK0, SCK1, SIN0 to SIN3		t _{CP} + 30		ns
SCK fall time	t _F	SCK0 to SCK3			10	ns
SCK rise time	t _R	SCK0 to SCK3			10	ns

Note: • AC characteristic in CLK synchronized mode.

C_L is load capacity value of pins when testing.
t_{CP} is internal operating clock cycle time (machine clock). Refer to " (1) Clock Timing".





11.8 Flash Memory Program/Erase Characteristics

Paramotor	Conditions	Value			Unit	Pomarke	
Falameter	Conditions	Min	Тур	Max		Itemarks	
Sector erase time			1	15	s	Excludes programming prior to erasure	
Chip erase time	$T_A = +25^{\circ}C$ $V_{CC} = 5.0 V$		9	—	s	Excludes programming prior to erasure	
Word (16-bit width) programming time			16	3600	μs	Except for the over head time of the system	
Program/Erase cycle		10000			cycle		
Flash Data Retention Time	Average $T_A = +85^{\circ}C$	20			year	*	

*: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85°C).



■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES





■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES





I/O characteristics





Part number	Package	Remarks
MB90346EPF		
MB90346ESPF	100-pin plastic QFP	
MB90346CEPF	(FPT-100P-M06)	
MB90346CESPF		
MB90346EPMC		1
MB90346ESPMC	100-pin plastic LQFP	
MB90346CEPMC	(FPT-100P-M20)	
MB90346CESPMC		
MB90347EPF		
MB90347ESPF	100-pin plastic QFP	
MB90347CEPF	(FPT-100P-M06)	
MB90347CESPF		
MB90347EPMC		
MB90347ESPMC	100-pin plastic LQFP	
MB90347CEPMC	(FPT-100P-M20)	
MB90347CESPMC		
MB90348EPF		
MB90348ESPF	100-pin plastic QFP	
MB90348CEPF	(FPT-100P-M06)	
MB90348CESPF		
MB90348EPMC		
MB90348ESPMC	100-pin plastic LQFP	
MB90348CEPMC	(FPT-100P-M20)	
MB90348CESPMC		
MB90349EPF		
MB90349ESPF	100-pin plastic QFP	
MB90349CEPF	(FPT-100P-M06)	
MB90349CESPF		
MB90349EPMC		1
MB90349ESPMC	100-pin plastic LQFP	
MB90349CEPMC	(FPT-100P-M20)	
MB90349CESPMC	1	
MB90V340E-101CR	299-pin ceramic PGA	For evolution
MB90V340E-102CR	(PGA-299C-A01)	



15. Major Changes

Spansiion Publication Number: DS07-13747-4E

Page	Section	Change Results
		Deleted the part numbers; MB90F343E(S), MB90F343CE(S)
51	Electrical Characteristics Absolute Maximum Ratings	Added "*6" in remark for "L" level maximum output current and "H" level maximum output current. Added "*7" in remark for "L" level average output current and "H" level average
		Added "*8" in remark for "L"level average overall output current and "H" level average overall output current.
		Added as follows. "*6:The maximum output current is defined as the peak value of the current of any one of the corresponding pins."
52		"*7:The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins."
		"*8:The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins."

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB90340E Series F2MC-16LX 16-bit Microcontroller Datasheet Document Number: 002-04498				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	AKIH	08/23/2010	Migrated to Cypress and assigned document number 002-04498. No change to document contents or format.
*A	5221535	AKIH	05/04/2016	Updated to Cypress template



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