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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

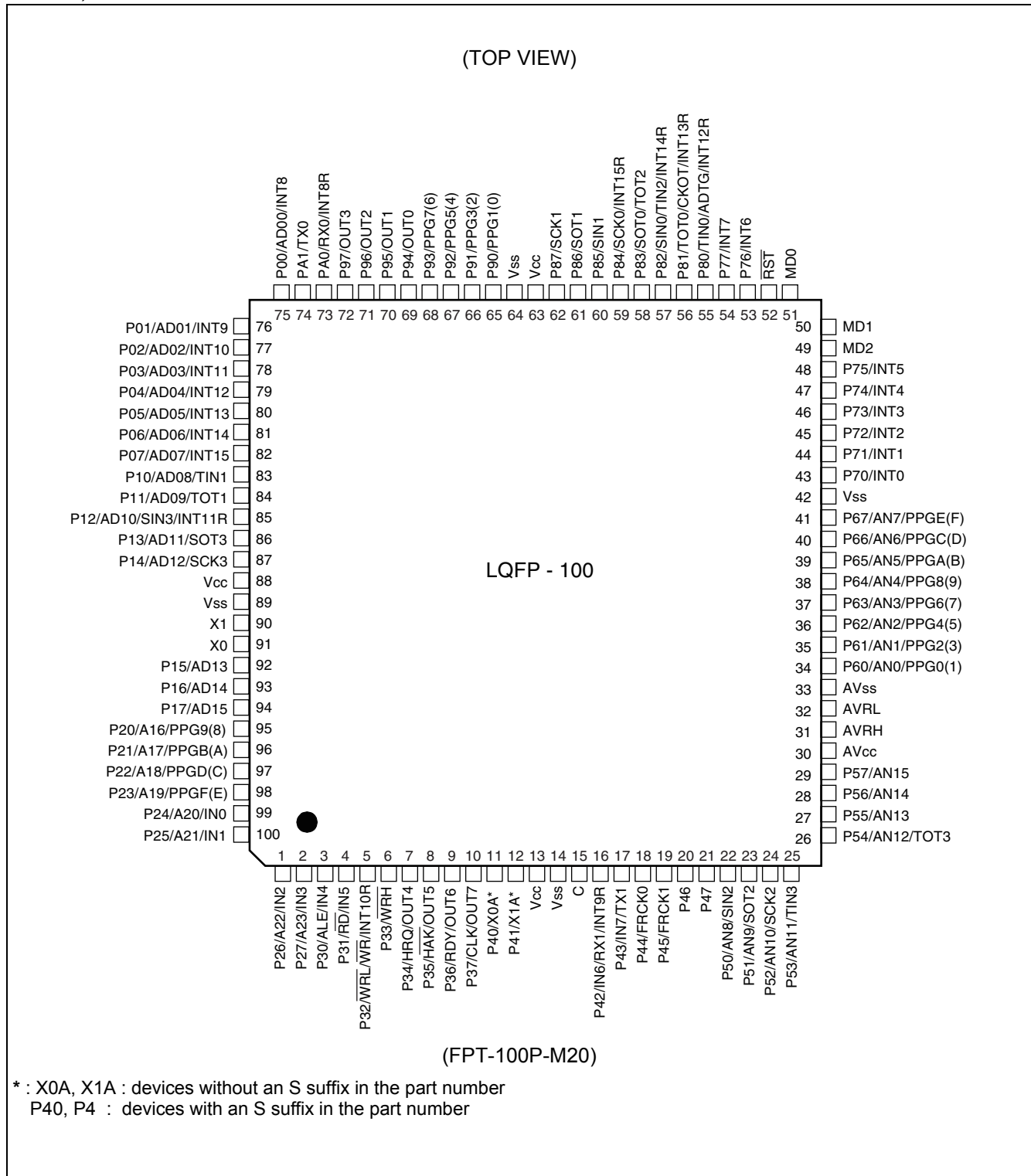
Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 24x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90349cepf-g-286e1

1. Product Lineup

Part Number			
Parameter	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
Type	Evaluation products	Flash memory products	MASK ROM products
CPU	F ² MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)		
ROM	External	512 Kbytes : MB90F345E(S), MB90F345CE(S) 256 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 128 Kbytes : MB90F347E(S), MB90F347CE(S) 64 Kbytes : MB90F346E(S), MB90F346CE(S)	256 Kbytes : MB90342E(S), MB90342CE(S), MB90349E(S), MB90349CE(S) 128 Kbytes : MB90341E(S), MB90341CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S) 64 Kbytes : MB90346E(S), MB90346CE(S)
RAM	30 Kbytes	20 Kbytes : MB90F345E(S), MB90F345CE(S) 16 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 6 Kbytes : MB90F347E(S), MB90F347CE(S) 2 Kbytes : MB90F346E(S), MB90F346CE(S)	16 Kbytes : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) 6 Kbytes : MB90347E(S), MB90347CE(S) 2 Kbytes : MB90346E(S), MB90346CE(S)
Emulator-specific power supply*	Yes	—	
Technology	0.35 μm CMOS with regulator for built-in power supply	0.35 μm CMOS with built-in power supply regulator + Flash memory with Charge pump for programming voltage	
Operating voltage range	5 V ± 10%	3.5 V to 5.5 V : When normal operating (not using A/D converter) 4.0 V to 5.5 V : When using the A/D converter/Flash programming 4.5 V to 5.5 V : When using the external bus	
Temperature range	—	−40°C to +105°C	
Package	PGA-299	QFP-100, LQFP-100	
LIN-UART	5 channels	4 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device		
I ² C (400 kbps)	2 channels	Devices with a C suffix in the part number : 2 channels Devices without a C suffix in the part number : —	

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3. Pin Description

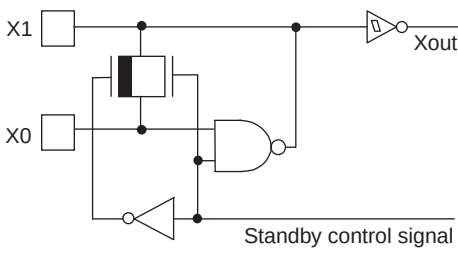
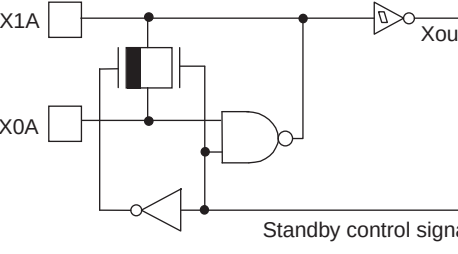
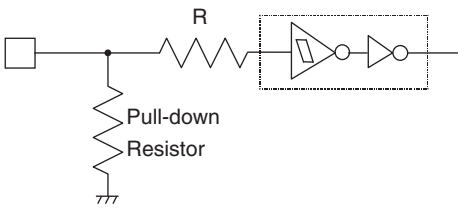
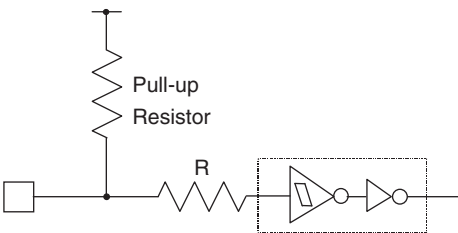
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
1 to 4	99 to 2	P24 to P27	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Trigger input pins for input captures.
5	3	P30	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Trigger input pin for input capture.
6	4	P31	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		$\overline{RD}$		External read strobe output pin. This function is enabled when the external bus is enabled.
		IN5		Trigger input pin for input capture.
7	5	P32	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the WR/WRL pin output is disabled.
		$\overline{WR} / \overline{WRL}$		Write strobe output pin for the external data bus. This function is enabled when both the external bus and the WR/WRL pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
		INT10R		External interrupt request input pin.
8	6	P33	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the WRH pin output is disabled.
		$\overline{WRH}$		Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled.

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV _{CC} .
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter
35	33	AV _{SS}	K	Analog GND pin for the A/D Converter
36 to 43	34 to 41	P60 to P67	I	General purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
44	42	V _{SS}	—	GND pin
45 to 50	43 to 48	P70 to P75	I	General purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT0 to INT5		External interrupt request input pins
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	RST	E	Reset input pin
55, 56	53, 54	P76, P77	I	General purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT6, INT7		External interrupt request input pins
57	55	P80	F	General purpose I/O pin.
		TIN0		Event input pin for the reload timer
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin
58	56	P81	F	General purpose I/O pin.
		TOT0		Output pin for the reload timer
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin
59	57	P82	M	General purpose I/O pin.
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer
		INT14R		External interrupt request input pin
60	58	P83	F	General purpose I/O pin.
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer

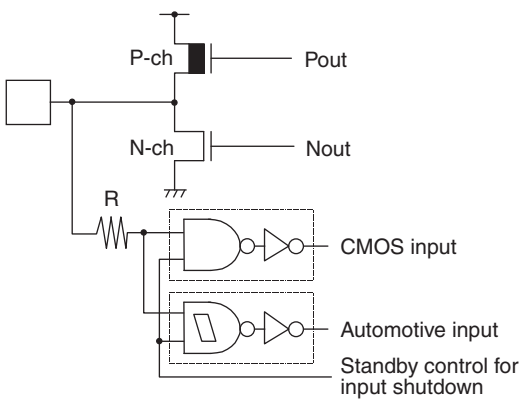
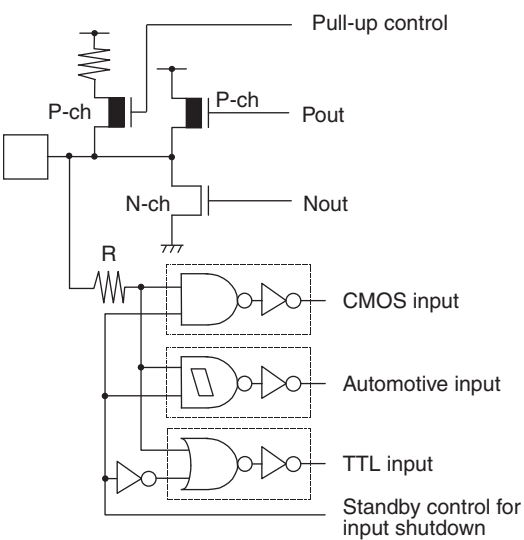
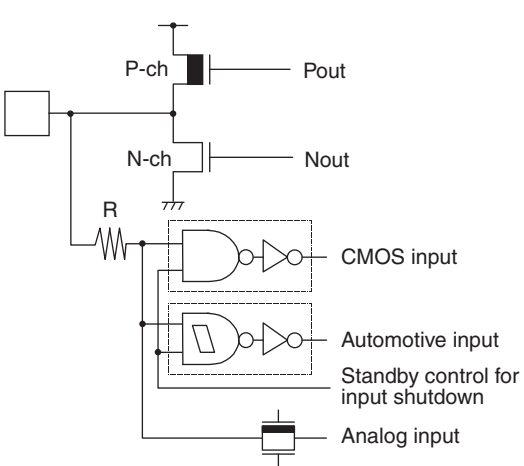
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4. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		■ MASK ROM and evaluation products: CMOS hysteresis input pin ■ Flash memory products: CMOS input pin
D		MASK ROM and evaluation products: ■ CMOS hysteresis input pin ■ Pull-down resistor value: approx. 50 kΩ Flash memory products: ■ CMOS input pin ■ No pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ

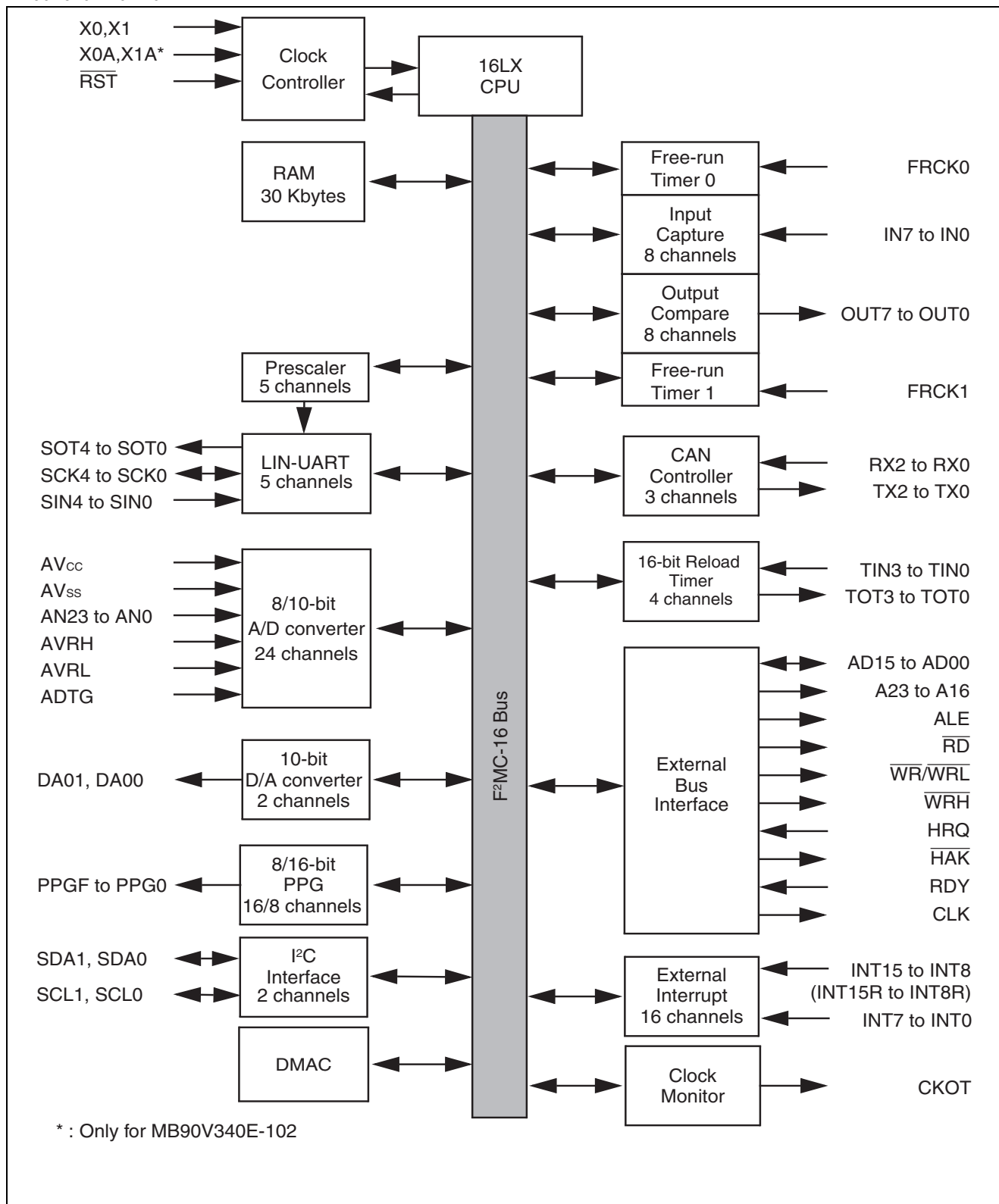
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Type	Circuit	Remarks
M		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
N		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) Programmable pull-up resistor: 50 kΩ approx
O		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input

6. Block Diagrams

■ MB90V340E-101/102



Address	Register	Abbreviation	Access	Resource name	Initial value
000040 _H	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	0X000XX1 _B
000041 _H	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		0X000001 _B
000042 _H	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		000000X0 _B
000043 _H	Reserved				
000044 _H	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	0X000XX1 _B
000045 _H	PPG B Operation Mode Control Register	PPGCB	W,R/W		0X000001 _B
000046 _H	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		000000X0 _B
000047 _H	Reserved				
000048 _H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	0X000XX1 _B
000049 _H	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001 _B
00004A _H	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		000000X0 _B
00004B _H	Reserved				
00004C _H	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	0X000XX1 _B
00004D _H	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001 _B
00004E _H	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		000000X0 _B
00004F _H	Reserved				
000050 _H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000 _B
000051 _H	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XX _B
000052 _H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000 _B
000053 _H	Input Capture Edge 2/3	ICE23	R		XXXXXXXX _B
000054 _H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000 _B
000055 _H	Input Capture Edge 4/5	ICE45	R		XXXXXXXX _B
000056 _H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000 _B
000057 _H	Input Capture Edge 6/7	ICE67	R/W, R		XXX000XX _B
000058 _H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00 _B
000059 _H	Output Compare Control Status 1	OCS1	R/W		0XX00000 _B
00005A _H	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00 _B
00005B _H	Output Compare Control Status 3	OCS3	R/W		0XX00000 _B
00005C _H	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00 _B
00005D _H	Output Compare Control Status 5	OCS5	R/W		0XX00000 _B
00005E _H	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00 _B
00005F _H	Output Compare Control Status 7	OCS7	R/W		0XX00000 _B

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List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007AF0 _H to 007AF7 _H	007CF0 _H to 007CF7 _H	Data Register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
007AF8 _H to 007AFF _H	007CF8 _H to 007CFF _H	Data Register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI ² OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC _H	—	—
INT9 instruction	N	—	#09	FFFFD8 _H	—	—
Exception	N	—	#10	FFFFD4 _H	—	—
CAN 0 RX	N	—	#11	FFFFD0 _H	ICR00	0000B0 _H
CAN 0 TX/NS	N	—	#12	FFFFCC _H		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4 _H		
CAN 2 RX / I ² C0	N	—	#15	FFFFC0 _H	ICR02	0000B2 _H
CAN 2 TX/NS	N	—	#16	FFFFBC _H		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8 _H	ICR03	0000B3 _H
16-bit Reload Timer 1	Y1	1	#18	FFFFB4 _H		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0 _H	ICR04	0000B4 _H
16-bit Reload Timer 3	Y1	—	#20	FFFFAC _H		
PPG 0/1/4/5	N	—	#21	FFFFA8 _H	ICR05	0000B5 _H
PPG 2/3/6/7	N	—	#22	FFFFA4 _H		
PPG 8/9/C/D	N	—	#23	FFFFA0 _H	ICR06	0000B6 _H
PPG A/B/E/F	N	—	#24	FFFF9C _H		
Time Base Timer	N	—	#25	FFFF98 _H	ICR07	0000B7 _H
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94 _H		
Watch Timer	N	—	#27	FFFF90 _H	ICR08	0000B8 _H
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C _H		
A/D Converter	Y1	5	#29	FFFF88 _H	ICR09	0000B9 _H
Free-run Timer 0 / Free-run Timer 1	N	—	#30	FFFF84 _H		
Input Capture 4/5 / I ² C1	Y1	6	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C _H		
Input Capture 0 to 3	Y1	8	#33	FFFF78 _H	ICR11	0000BB _H
Output Compare 2/3/6/7	Y1	9	#34	FFFF74 _H		
UART 0 RX	Y2	10	#35	FFFF70 _H	ICR12	0000BC _H
UART 0 TX	Y1	11	#36	FFFF6C _H		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68 _H	ICR13	0000BD _H
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64 _H		

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11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *2
	$AVRH, AVRL$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH, AV_{CC} \geq AVRL, AVRH \geq AVRL$
Input voltage*1	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\sum I_{CLAMP} $	—	40	mA	*5
"L" level maximum output current	I_{OL}	—	15	mA	*4, *6
"L" level average output current	I_{OLAV}	—	4	mA	*4, *7
"L" level maximum overall output current	$\sum I_{OL}$	—	100	mA	*4
"L" level average overall output current	$\sum I_{OLAV}$	—	50	mA	*4, *8
"H" level maximum output current	I_{OH}	—	-15	mA	*4, *6
"H" level average output current	I_{OHAV}	—	-4	mA	*4, *7
"H" level maximum overall output current	$\sum I_{OH}$	—	-100	mA	*4
"H" level average overall output current	$\sum I_{OHAV}$	—	-50	mA	*4, *8
Power consumption	P_D	—	450	mW	
Operating temperature	T_A	-40	+105	°C	
Storage temperature	T_{STG}	-55	+150	°C	

*1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V

*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed $V_{CC} + 0.3$ V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, PA1

*5: • Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (Evaluation device : P50 to P55), P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1

• Use within recommended operating conditions.

• Use with DC voltage (current)

• The +B signal should always be applied by using a limiting resistance placed between the +B signal and the microcontroller.

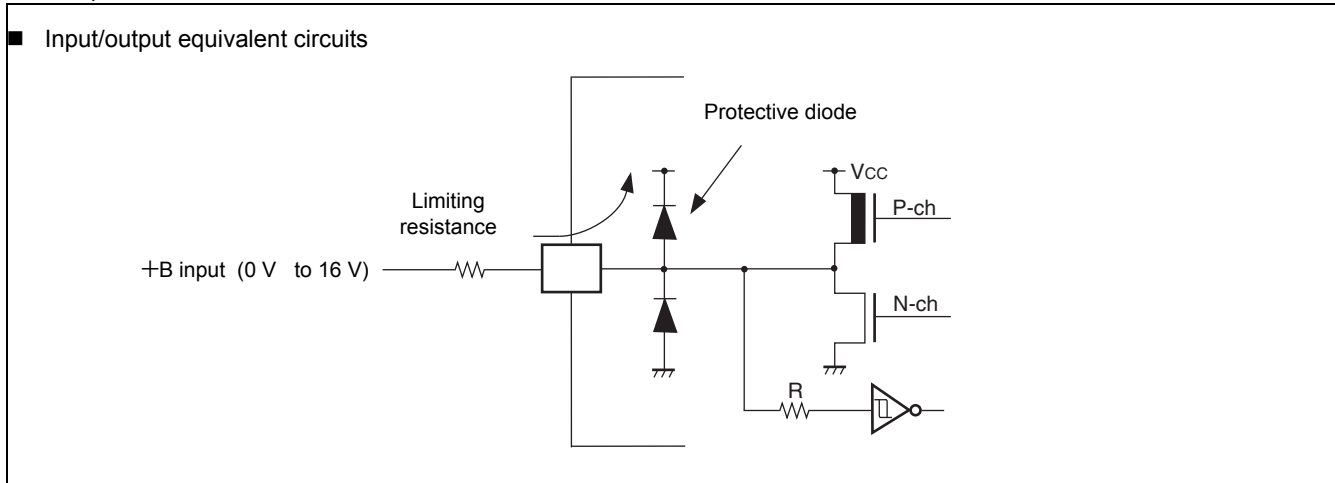
• The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed the rated value, either instantaneously or for prolonged periods.

• Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.

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- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:



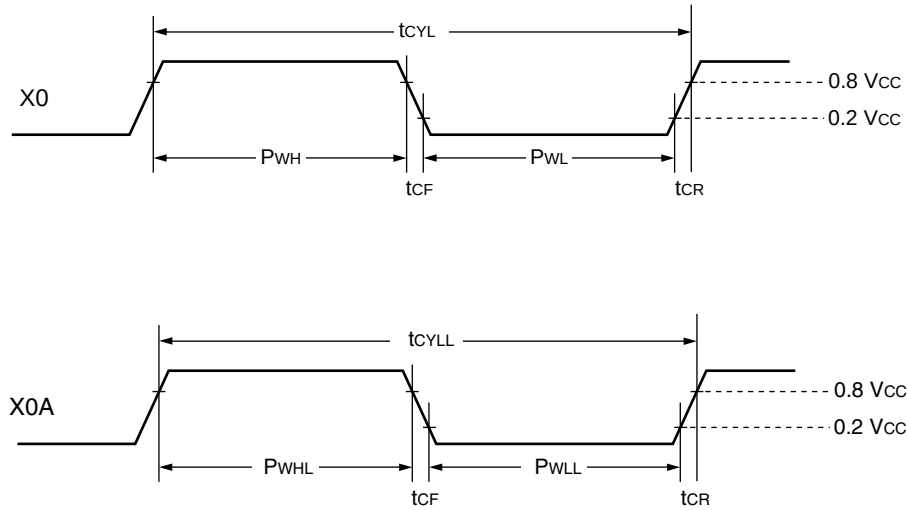
*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

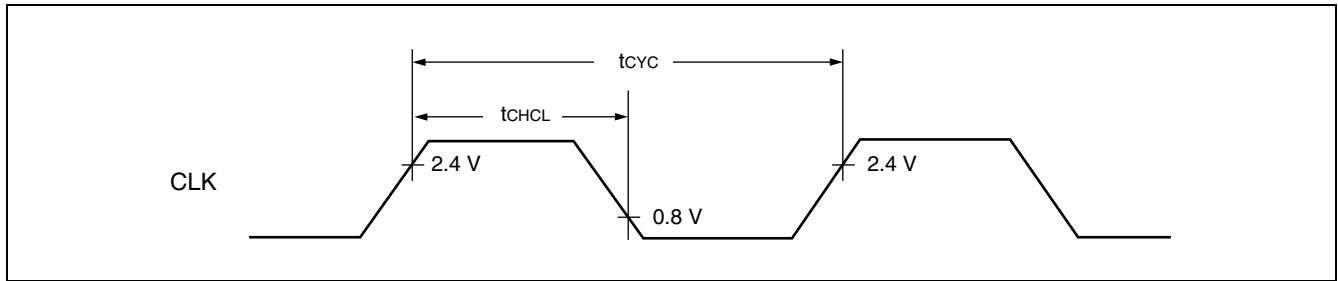
*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Clock Timing

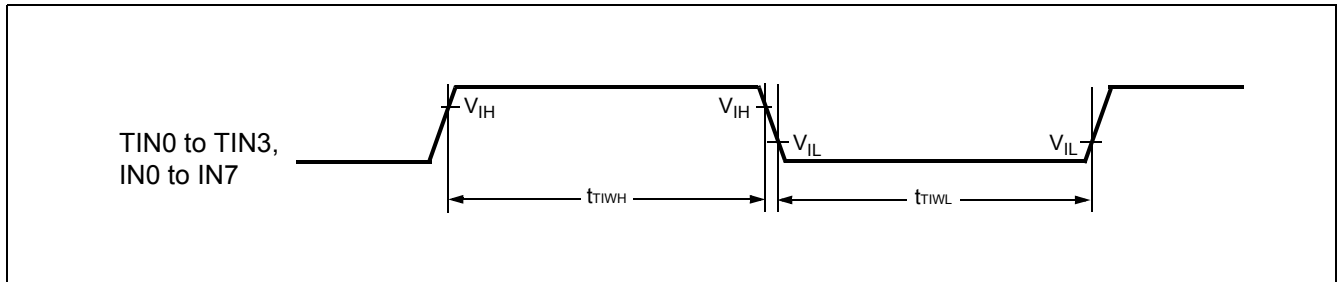




11.4.11 Timer Related Resource Input Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

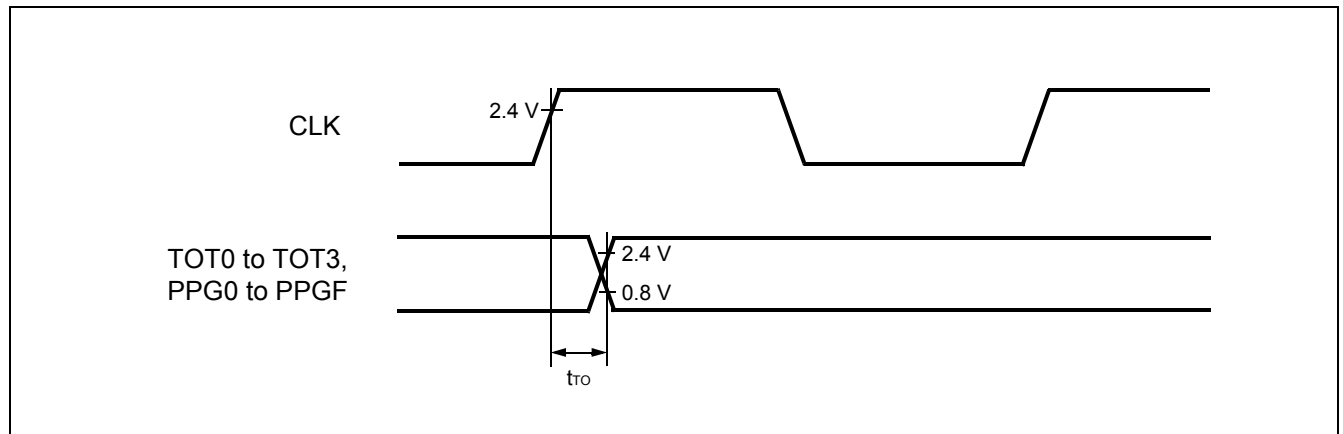
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH}	TIN0 to TIN3, IN0 to IN7	—	$4 t_{CP}$	—	ns
	t_{TIWL}					



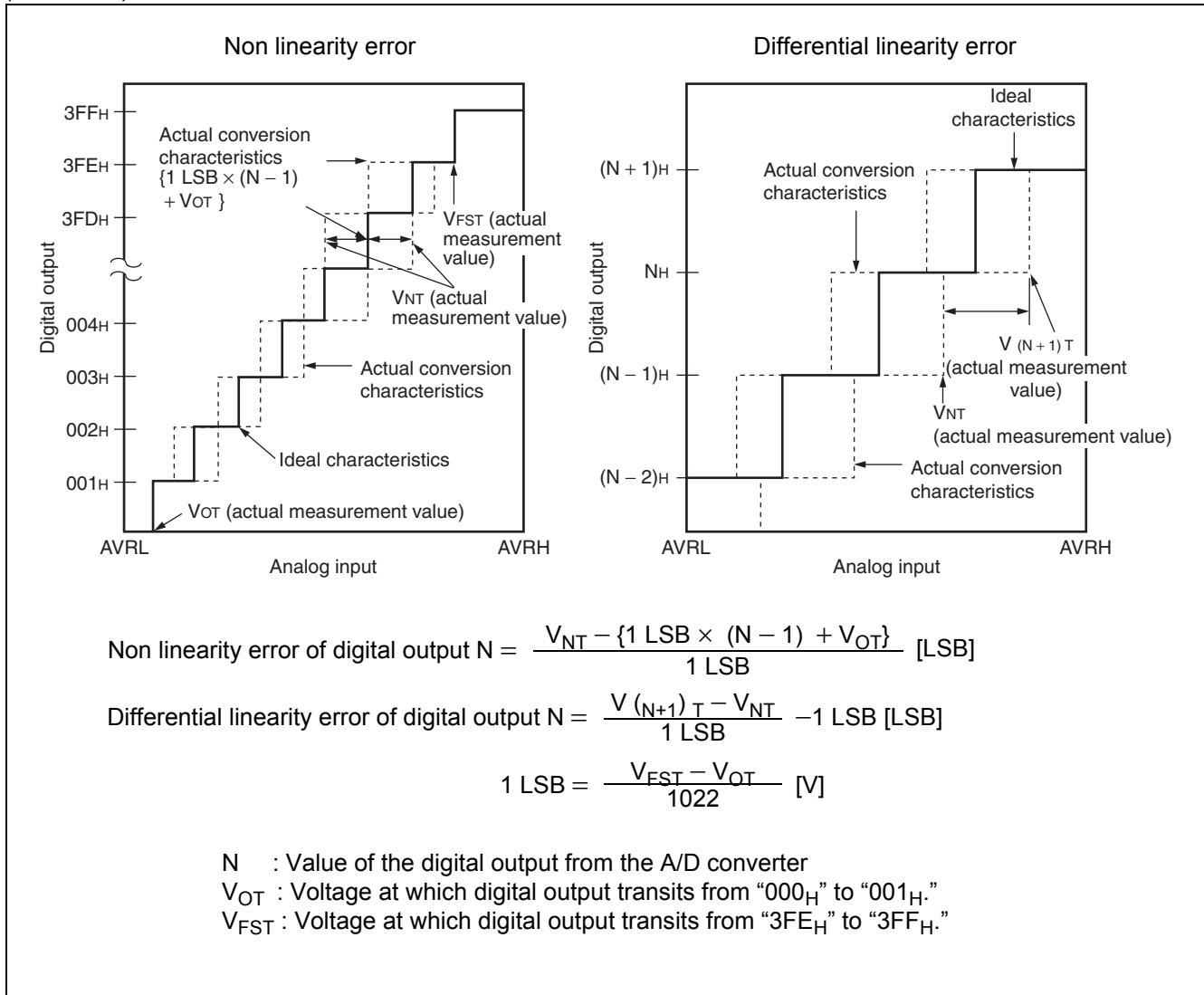
11.4.12 Timer Related Resource Output Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK $\uparrow \rightarrow T_{OUT}$ change time	t_{TO}	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns



(Continued)



11.7 Notes on A/D Converter Section

Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower ($4.0 \text{ V} \leq AV_{CC} \leq 5.5 \text{ V}$,
sampling period = 0.5 μs)

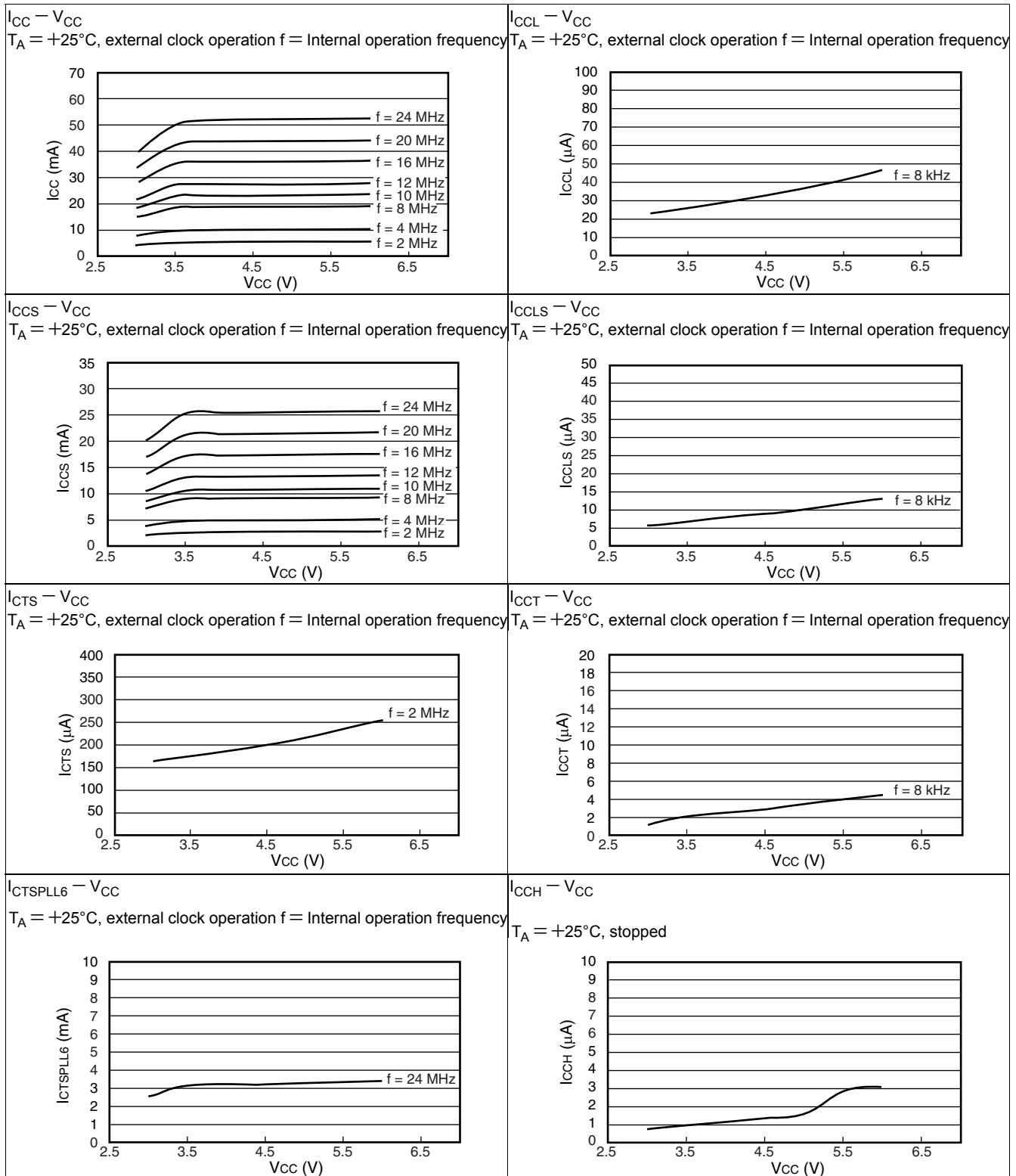
If an external capacitor is used, in consideration of the capacitive voltage dividing effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor be several thousand times greater than the capacitance of the internal capacitor.

11.8 Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25^{\circ}\text{C}$ $V_{CC} = 5.0\text{ V}$	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	μs	Except for the over head time of the system
Program/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average $T_A = +85^{\circ}\text{C}$	20	—	—	year	*

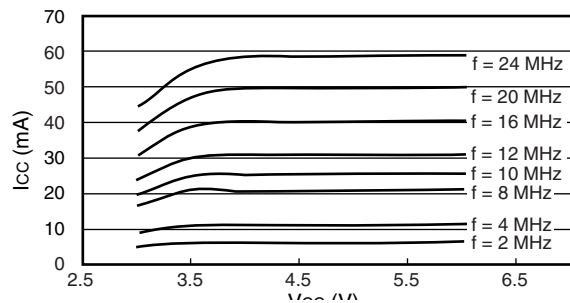
* : This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at $+85^{\circ}\text{C}$) .

■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES

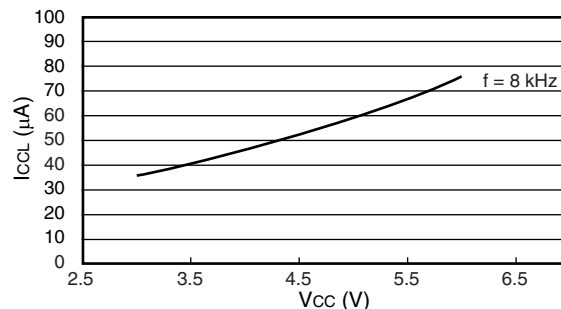


■ MB90F345E, MB90F345ES, MB90F345CE, MB90F345CES

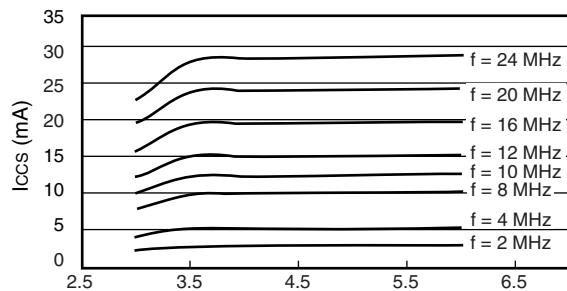
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



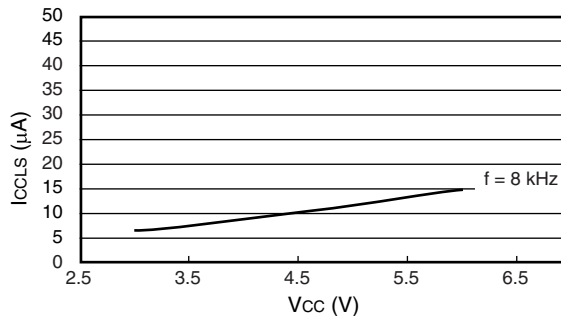
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



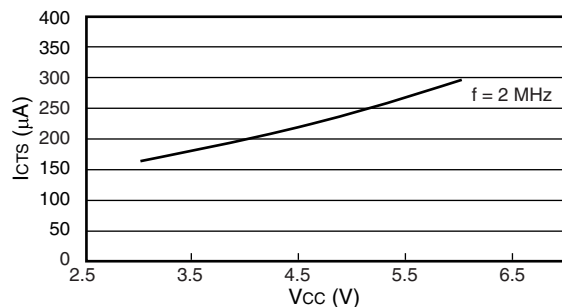
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



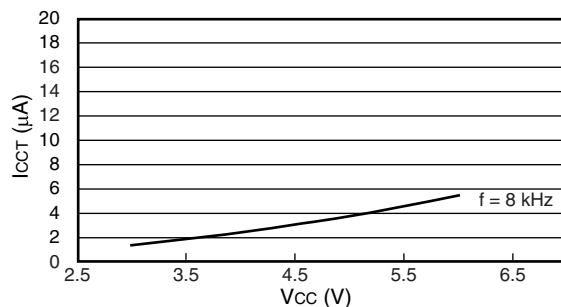
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



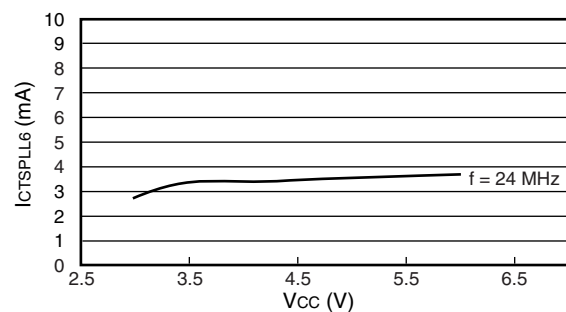
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



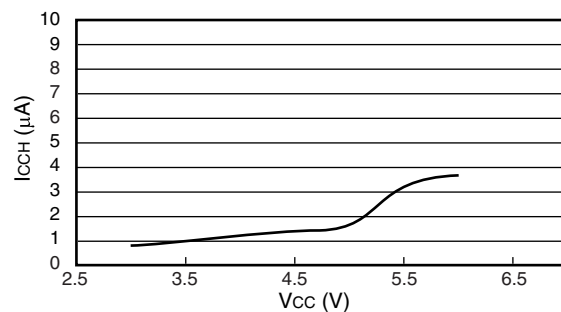
$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency

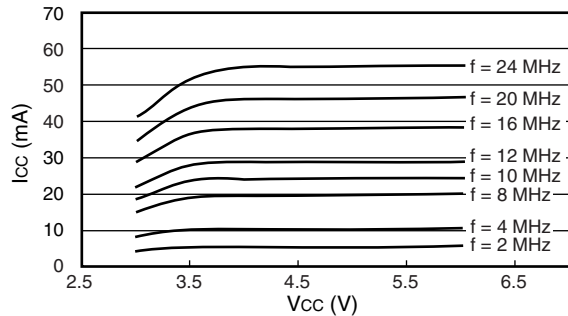


$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped

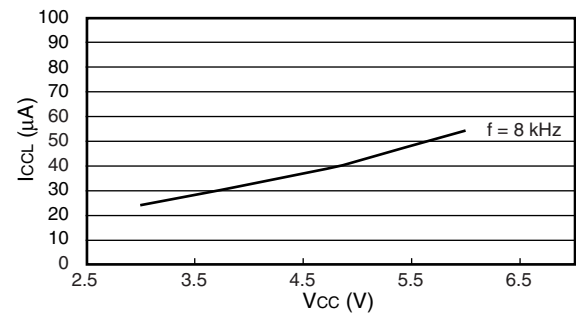


■ MB90347E, MB90347ES, MB90347CE, MB90347CES

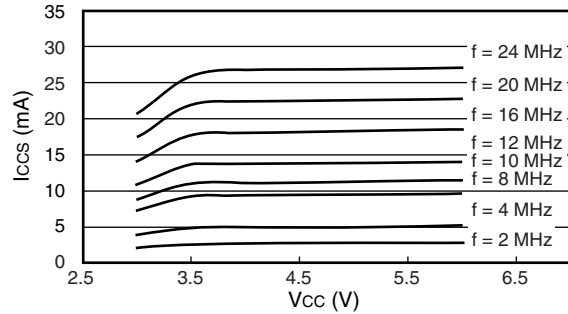
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



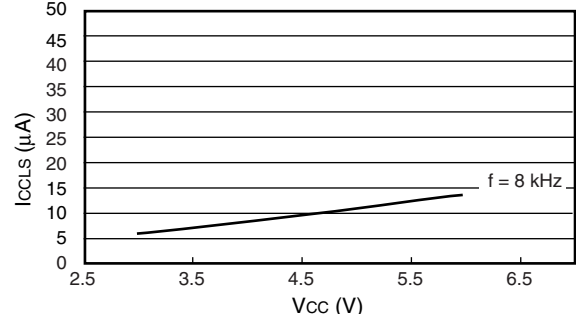
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



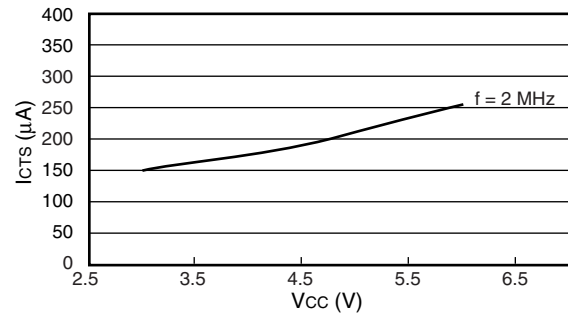
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



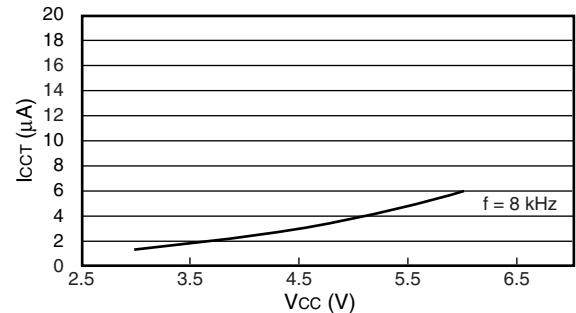
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



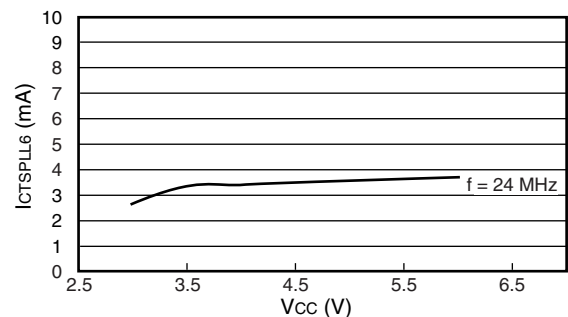
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped

