Infineon Technologies - MB90349CEPF-G-352E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 24x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90349cepf-g-352e1

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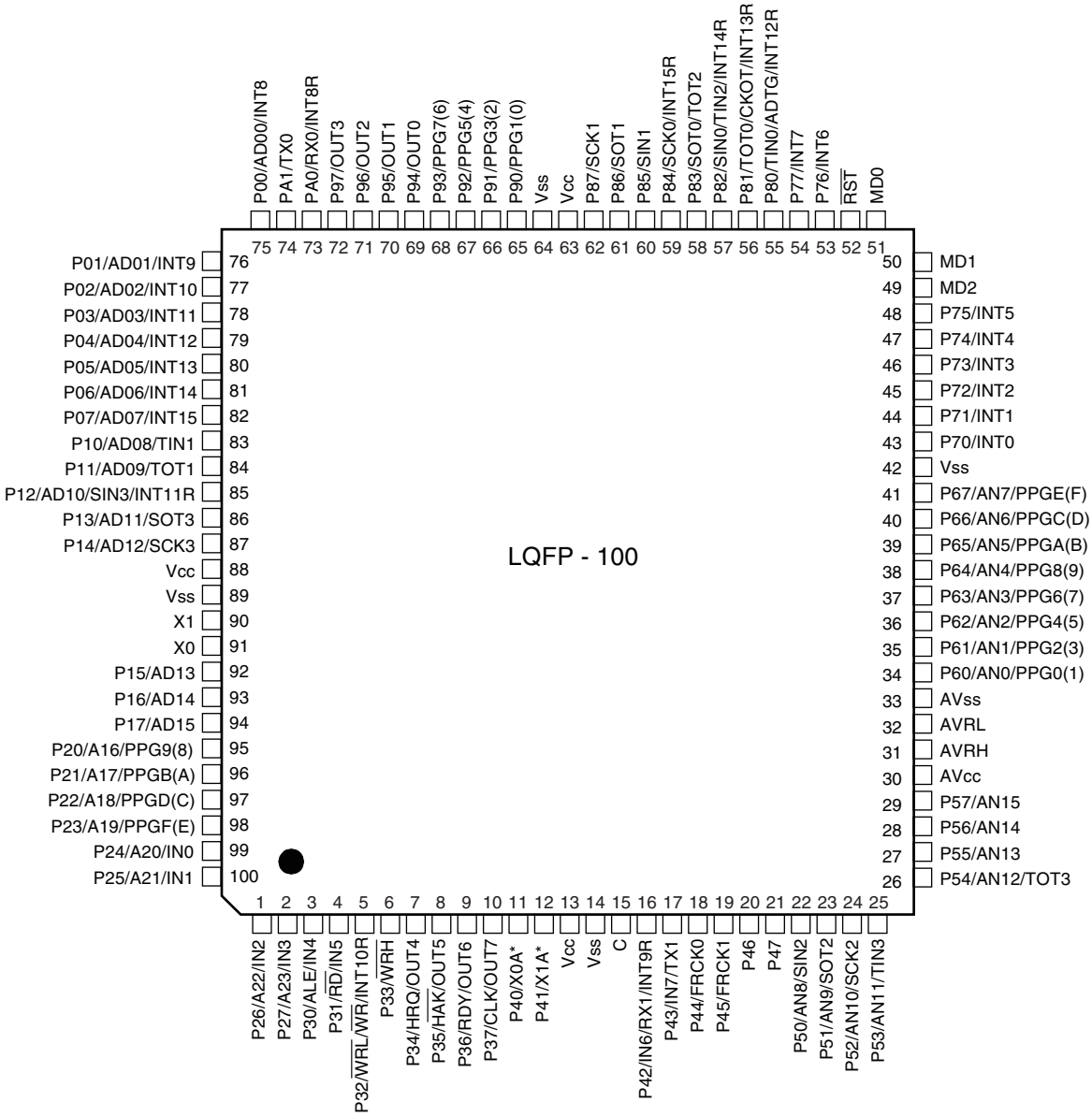
(TOP VIEW)



(FPT-100P-M20)

* : X0A, X1A : devices without an S suffix in the part number
P40, P4 : devices with an S suffix in the part number

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I^2C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I^2C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I^2C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I^2C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV_{CC}	K	Analog power input pin for the A/D Converter

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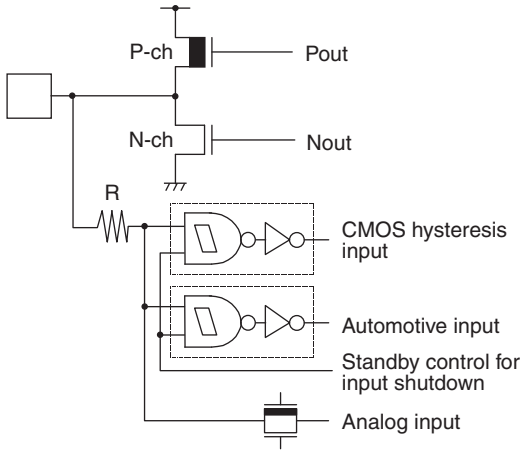
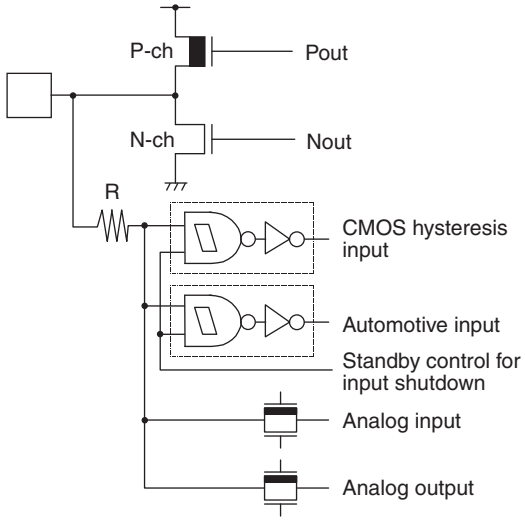
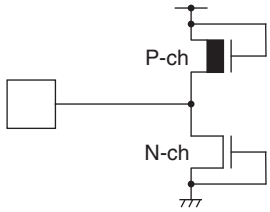
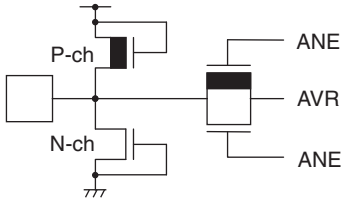
Type	Circuit	Remarks
I		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
J		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ D/A analog output ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
K		Power supply input protection circuit
L		■ A/D converter reference voltage power supply input pin, with the protection circuit ■ Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH

5. Handling Devices

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Handling unused pins

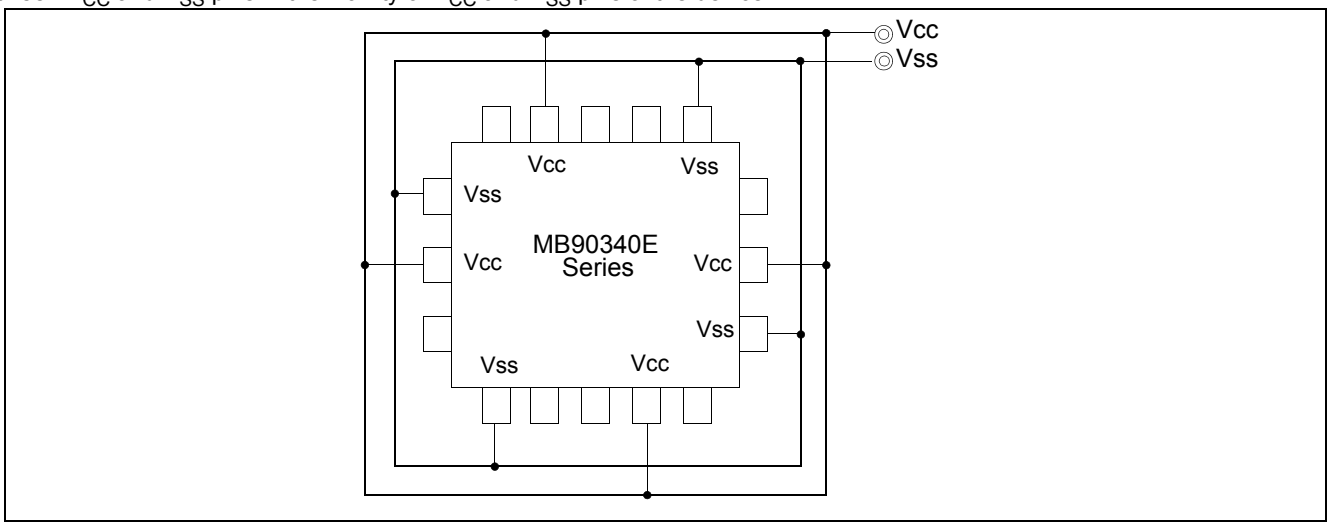
Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 kΩ or more.

3. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
Connect V_{CC} and V_{SS} pins to the device from the current supply source at a possibly low impedance.

- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.

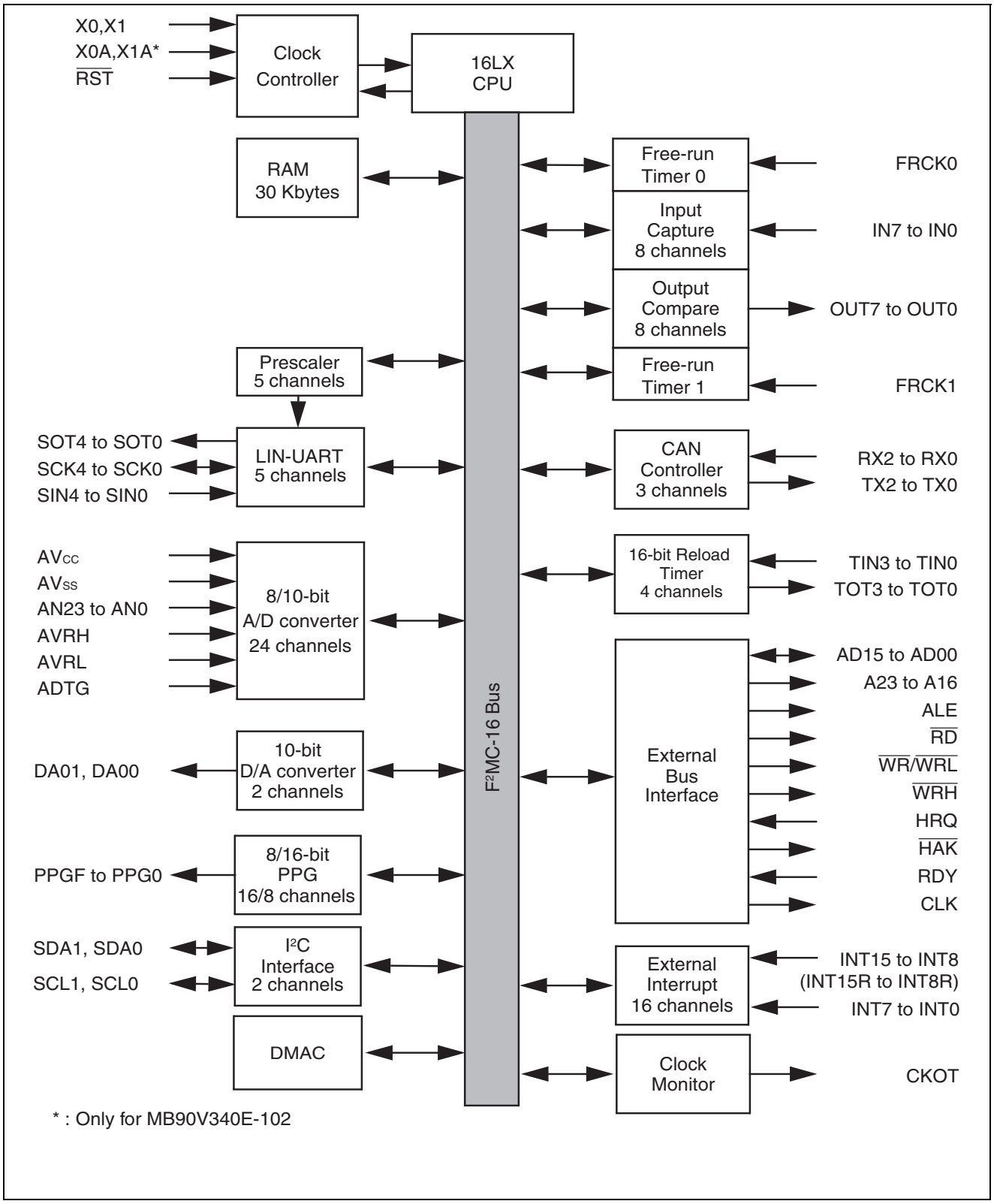


4. Mode Pins (MD0 to MD2)

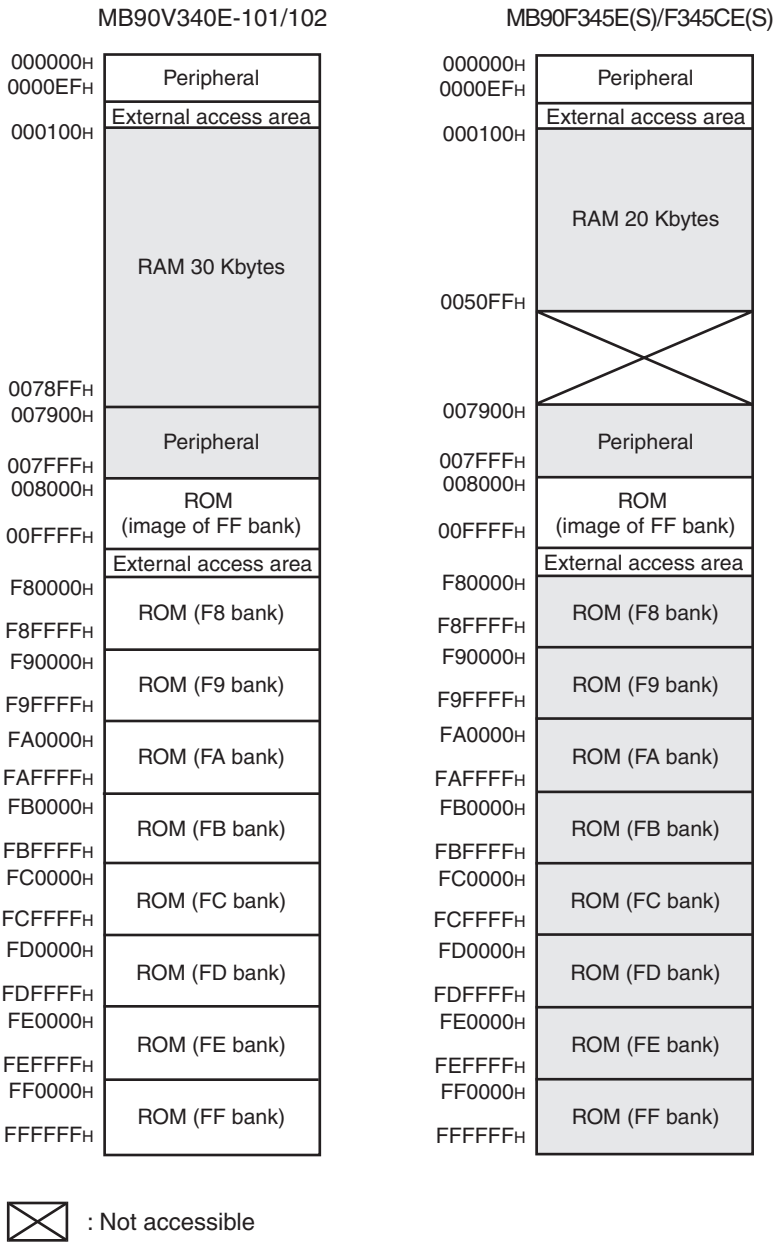
Connect the mode pins directly to V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

6. Block Diagrams

- MB90V340E-101/102



7. Memory Map


MB90V340E-101/102
000000H
0000EFH
Peripheral
External access area
000100H
RAM 30 Kbytes
0078FFH
007900H
Peripheral
007FFFH
008000H
ROM
(image of FF bank)
00FFFFH
External access area
F80000H
ROM (F8 bank)
F8FFFFH
F90000H
ROM (F9 bank)
F9FFFFH
FA0000H
ROM (FA bank)
FAFFFFH
FB0000H
ROM (FB bank)
FBFFFFH
FC0000H
ROM (FC bank)
FCFFFFH
FD0000H
ROM (FD bank)
FDFFFFH
FE0000H
ROM (FE bank)
FEFFFFH
FF0000H
ROM (FF bank)
FFFFFFH
MB90F345E(S)/F345CE(S)
000000H
0000EFH
Peripheral
External access area
000100H
RAM 20 Kbytes
0050FFH
007900H
Peripheral
007FFFH
008000H
ROM
(image of FF bank)
00FFFFH
External access area
F80000H
ROM (F8 bank)
F8FFFFH
F90000H
ROM (F9 bank)
F9FFFFH
FA0000H
ROM (FA bank)
FAFFFFH
FB0000H
ROM (FB bank)
FBFFFFH
FC0000H
ROM (FC bank)
FCFFFFH
FD0000H
ROM (FD bank)
FDFFFFH
FE0000H
ROM (FE bank)
FEFFFFH
FF0000H
ROM (FF bank)
FFFFFFH
: Not accessible

8. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
000000_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
000001_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
000002_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
000003_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
000004_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
000005_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
000006_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
000007_H	Port 7 Data Register	PDR7	R/W	Port 7	$XXXXXXXX_B$
000008_H	Port 8 Data Register	PDR8	R/W	Port 8	$XXXXXXXX_B$
000009_H	Port 9 Data Register	PDR9	R/W	Port 9	$XXXXXXXX_B$
$00000A_H$	Port A Data Register	PDRA	R/W	Port A	$XXXXXXXX_B$
$00000B_H$	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111_B
$00000C_H$	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111_B
$00000D_H$	Port 7 Analog Input Enable Register	ADER7	R/W	Port 7, A/D	11111111_B
$00000E_H$	Input Level Select Register 0	ILSR0	R/W	Ports	$XXXXXXXX_B$
$00000F_H$	Input Level Select Register 1	ILSR1	R/W	Ports	$XXXX0XXX_B$
000010_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
000011_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
000012_H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000_B
000013_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
000014_H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000_B
000015_H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000_B
000016_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
000017_H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000_B
000018_H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000_B
000019_H	Port 9 Direction Register	DDR9	R/W	Port 9	00000000_B
$00001A_H$	Port A Direction Register	DDRA	R/W	Port A	00000100_B
$00001B_H$	Reserved				
$00001C_H$	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000_B
$00001D_H$	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000_B
$00001E_H$	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000_B
$00001F_H$	Port 3 Pull-up Control Register	PUCR3	W, R/W	Port 3	00000000_B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$0000A5_H$	Automatic Ready Function Select Register	ARSR	W	External Memory Access	$0011XX00_B$
$0000A6_H$	External Address Output Control Register	HACR	W		00000000_B
$0000A7_H$	Bus Control Signal Selection Register	ECSR	W		$0000000X_B$
$0000A8_H$	Watchdog Control Register	WDTC	R,W	Watchdog Timer	$XXXXX111_B$
$0000A9_H$	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	$1XX00100_B$
$0000AA_H$	Watch Timer Control Register	WTC	R,R/W	Watch Timer	$1X001000_B$
$0000AB_H$	Reserved				
$0000AC_H$	DMA Enable L Register	DERL	R/W	DMA	00000000_B
$0000AD_H$	DMA Enable H Register	DERH	R/W		00000000_B
$0000AE_H$	Flash Control Status Register (Flash memory devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	$000X0000_B$
$0000AF_H$	Reserved				
$0000B0_H$	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111_B
$0000B1_H$	Interrupt Control Register 01	ICR01	W,R/W		00000111_B
$0000B2_H$	Interrupt Control Register 02	ICR02	W,R/W		00000111_B
$0000B3_H$	Interrupt Control Register 03	ICR03	W,R/W		00000111_B
$0000B4_H$	Interrupt Control Register 04	ICR04	W,R/W		00000111_B
$0000B5_H$	Interrupt Control Register 05	ICR05	W,R/W		00000111_B
$0000B6_H$	Interrupt Control Register 06	ICR06	W,R/W		00000111_B
$0000B7_H$	Interrupt Control Register 07	ICR07	W,R/W		00000111_B
$0000B8_H$	Interrupt Control Register 08	ICR08	W,R/W		00000111_B
$0000B9_H$	Interrupt Control Register 09	ICR09	W,R/W		00000111_B
$0000BA_H$	Interrupt Control Register 10	ICR10	W,R/W		00000111_B
$0000BB_H$	Interrupt Control Register 11	ICR11	W,R/W		00000111_B
$0000BC_H$	Interrupt Control Register 12	ICR12	W,R/W		00000111_B
$0000BD_H$	Interrupt Control Register 13	ICR13	W,R/W		00000111_B
$0000BE_H$	Interrupt Control Register 14	ICR14	W,R/W		00000111_B
$0000BF_H$	Interrupt Control Register 15	ICR15	W,R/W		00000111_B
$0000C0_H$	D/A Converter Data 0	DAT0	R/W	D/A Converter	$XXXXXXXX_B$
$0000C1_H$	D/A Converter Data 1	DAT1	R/W		$XXXXXXXX_B$
$0000C2_H$	D/A Control 0	DACR0	R/W		$XXXXXXX0_B$
$0000C3_H$	D/A Control 1	DACR1	R/W		$XXXXXXX0_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007900_H	Reload Register L0	PRLL0	R/W	16-bit PPG 0/1	$XXXXXXXX_B$
007901_H	Reload Register H0	PRLH0	R/W		$XXXXXXXX_B$
007902_H	Reload Register L1	PRLL1	R/W		$XXXXXXXX_B$
007903_H	Reload Register H1	PRLH1	R/W		$XXXXXXXX_B$
007904_H	Reload Register L2	PRLL2	R/W	16-bit PPG 2/3	$XXXXXXXX_B$
007905_H	Reload Register H2	PRLH2	R/W		$XXXXXXXX_B$
007906_H	Reload Register L3	PRLL3	R/W		$XXXXXXXX_B$
007907_H	Reload Register H3	PRLH3	R/W		$XXXXXXXX_B$
007908_H	Reload Register L4	PRLL4	R/W	16-bit PPG 4/5	$XXXXXXXX_B$
007909_H	Reload Register H4	PRLH4	R/W		$XXXXXXXX_B$
$00790A_H$	Reload Register L5	PRLL5	R/W		$XXXXXXXX_B$
$00790B_H$	Reload Register H5	PRLH5	R/W		$XXXXXXXX_B$
$00790C_H$	Reload Register L6	PRLL6	R/W	16-bit PPG 6/7	$XXXXXXXX_B$
$00790D_H$	Reload Register H6	PRLH6	R/W		$XXXXXXXX_B$
$00790E_H$	Reload Register L7	PRLL7	R/W		$XXXXXXXX_B$
$00790F_H$	Reload Register H7	PRLH7	R/W		$XXXXXXXX_B$
007910_H	Reload Register L8	PRLL8	R/W	16-bit PPG 8/9	$XXXXXXXX_B$
007911_H	Reload Register H8	PRLH8	R/W		$XXXXXXXX_B$
007912_H	Reload Register L9	PRLL9	R/W		$XXXXXXXX_B$
007913_H	Reload Register H9	PRLH9	R/W		$XXXXXXXX_B$
007914_H	Reload Register LA	PRLLA	R/W	16-bit PPG A/B	$XXXXXXXX_B$
007915_H	Reload Register HA	PRLHA	R/W		$XXXXXXXX_B$
007916_H	Reload Register LB	PRLLB	R/W		$XXXXXXXX_B$
007917_H	Reload Register HB	PRLHB	R/W		$XXXXXXXX_B$
007918_H	Reload Register LC	PRLLC	R/W	16-bit PPG C/D	$XXXXXXXX_B$
007919_H	Reload Register HC	PRLHC	R/W		$XXXXXXXX_B$
$00791A_H$	Reload Register LD	PRLLD	R/W		$XXXXXXXX_B$
$00791B_H$	Reload Register HD	PRLHD	R/W		$XXXXXXXX_B$
$00791C_H$	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	$XXXXXXXX_B$
$00791D_H$	Reload Register HE	PRLHE	R/W		$XXXXXXXX_B$
$00791E_H$	Reload Register LF	PRLLF	R/W		$XXXXXXXX_B$
$00791F_H$	Reload Register HF	PRLHF	R/W		$XXXXXXXX_B$
007920_H	Input Capture 0	IPCP0	R	Input Capture 0/1	$XXXXXXXX_B$
007921_H	Input Capture 0	IPCP0	R		$XXXXXXXX_B$
007922_H	Input Capture 1	IPCP1	R		$XXXXXXXX_B$
007923_H	Input Capture 1	IPCP1	R		$XXXXXXXX_B$

(Continued)

List of Control Registers (2)

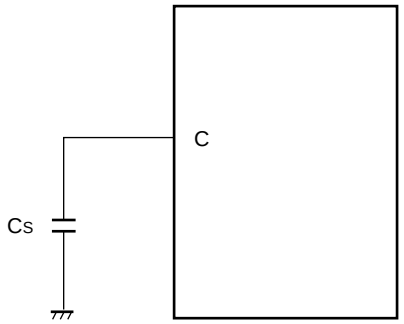
Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007B00_H$	$007D00_H$	Control Status Register	CSR	R/W, W R/W, R	$0XXXX0X1_B$ $00XXX000_B$
$007B01_H$	$007D01_H$				
$007B02_H$	$007D02_H$	Last Event Indicator Register	LEIR	R/W	$000X0000_B$ $XXXXXXXX_B$
$007B03_H$	$007D03_H$				
$007B04_H$	$007D04_H$	Receive And Transmit Error Counter	RTEC	R	00000000_B 00000000_B
$007B05_H$	$007D05_H$				
$007B06_H$	$007D06_H$	Bit Timing Register	BTR	R/W	11111111_B $X1111111_B$
$007B07_H$	$007D07_H$				
$007B08_H$	$007D08_H$	IDE Register	IDER	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B09_H$	$007D09_H$				
$007B0A_H$	$007D0A_H$	Transmit RTR Register	TRTRR	R/W	00000000_B 00000000_B
$007B0B_H$	$007D0B_H$				
$007B0C_H$	$007D0C_H$	Remote Frame Receive Waiting Register	RFWTR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B0D_H$	$007D0D_H$				
$007B0E_H$	$007D0E_H$	Transmit Interrupt Enable Register	TIER	R/W	00000000_B 00000000_B
$007B0F_H$	$007D0F_H$				
$007B10_H$	$007D10_H$	Acceptance Mask Select Register	AMSR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B11_H$	$007D11_H$				
$007B12_H$	$007D12_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B13_H$	$007D13_H$				
$007B14_H$	$007D14_H$	Acceptance Mask Register 0	AMR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B15_H$	$007D15_H$				
$007B16_H$	$007D16_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B17_H$	$007D17_H$				
$007B18_H$	$007D18_H$	Acceptance Mask Register 1	AMR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B19_H$	$007D19_H$				
$007B1A_H$	$007D1A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B1B_H$	$007D1B_H$				

11.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	µF	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.
Operating temperature	T_A	−40	—	+105	°C	

C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

11.4 AC Characteristics

11.4.1 Clock Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP}≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	When using an oscillation circuit
			4	—	16	MHz	PLL multiplied by 1 When using an oscillation circuit
			4	—	12	MHz	PLL multiplied by 2 When using an oscillation circuit
			4	—	8	MHz	PLL multiplied by 3 When using an oscillation circuit
			4	—	6	MHz	PLL multiplied by 4 When using an oscillation circuit
			—	—	4	MHz	PLL multiplied by 6 When using an oscillation circuit
			3	—	24	MHz	When using an external clock*
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	µs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	µs	When using sub clock

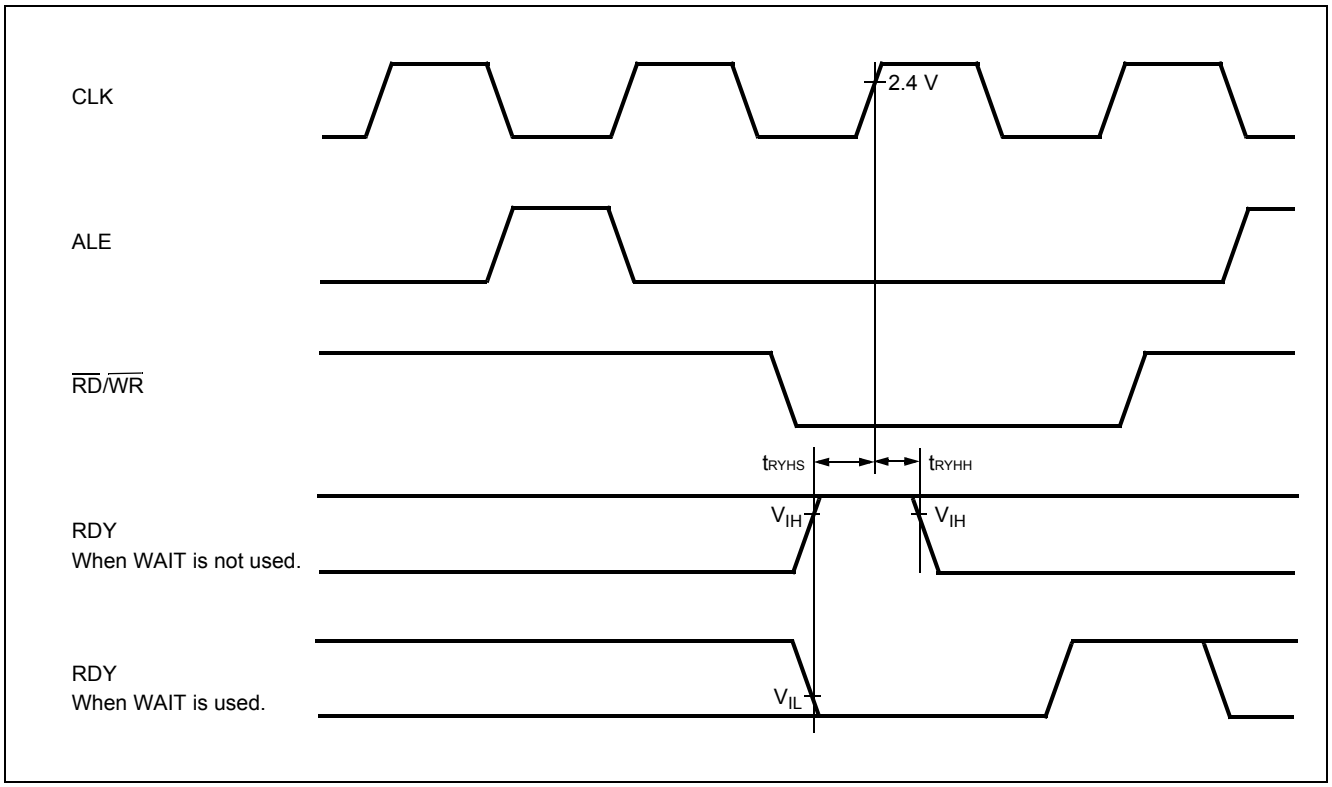
* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in “Relation between the external clock frequency and machine clock frequency”.

11.4.7 Ready Input Timing

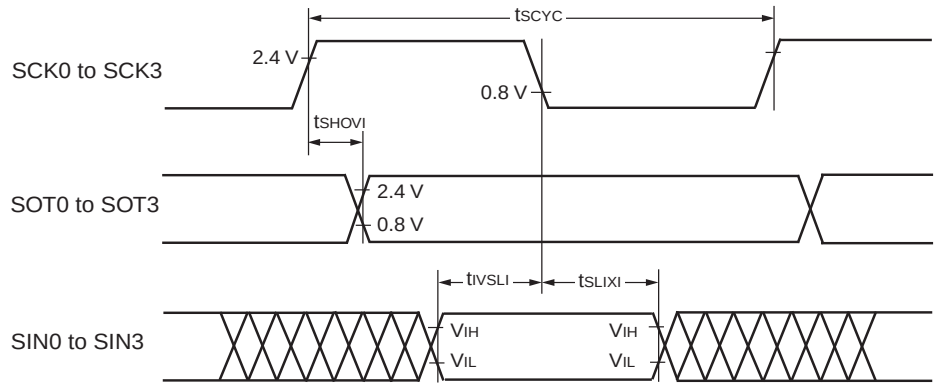
(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Test Condition	Rated Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	f_{CP} = 16 MHz
				32	—	ns	f_{CP} = 24 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

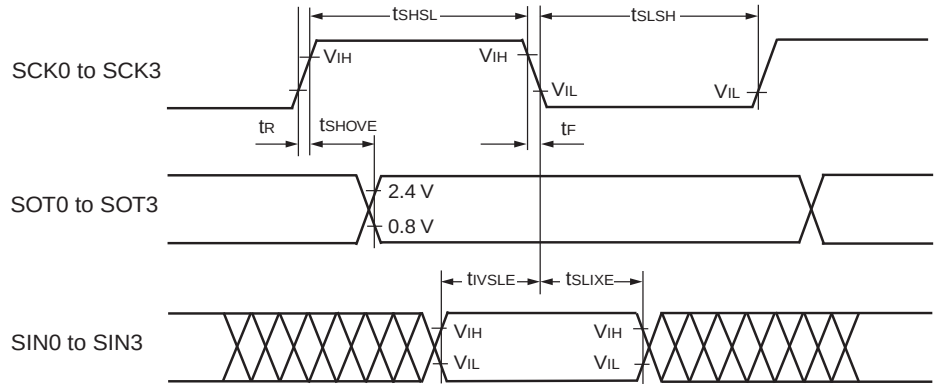
Note: : If the RDY setup time is insufficient, use the auto-ready function.



- Internal Shift Clock Mode



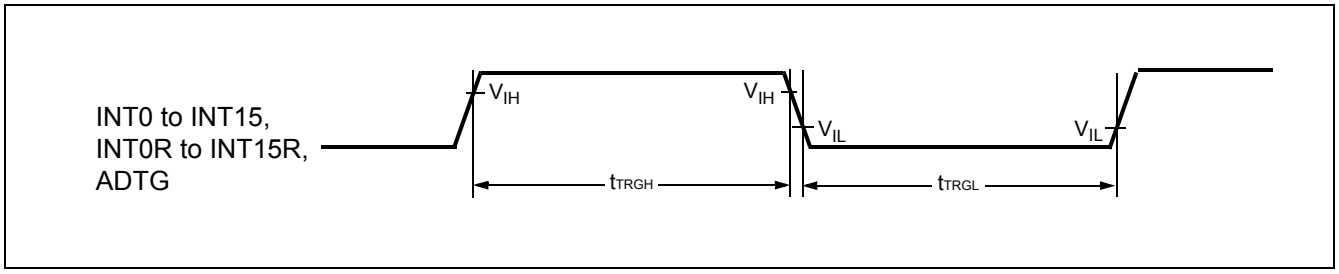
- External Shift Clock Mode



11.4.10 Trigger Input Timing

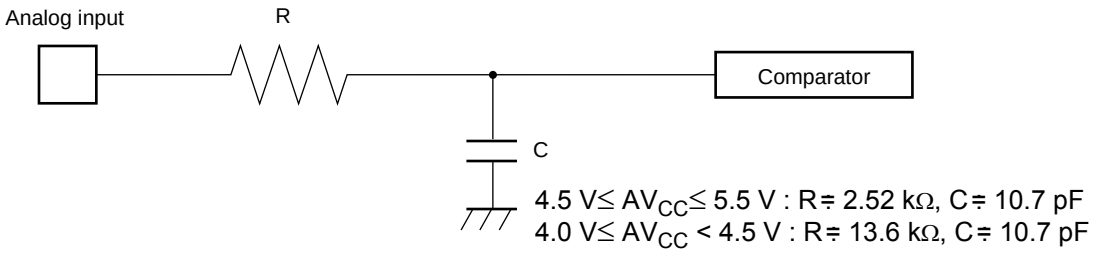
(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT15, INT0R to INT15R, ADTG	—	5 t_{CP}	—	ns



If the output impedance of the external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model

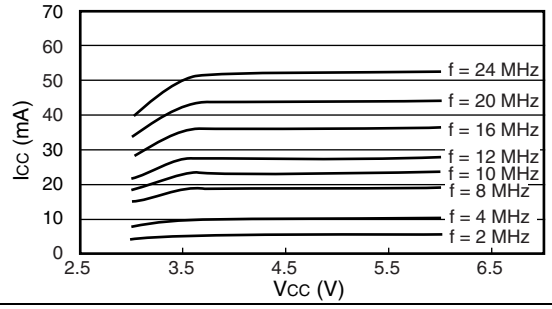


Note: : Use the values in the figure only as a guideline.

■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES

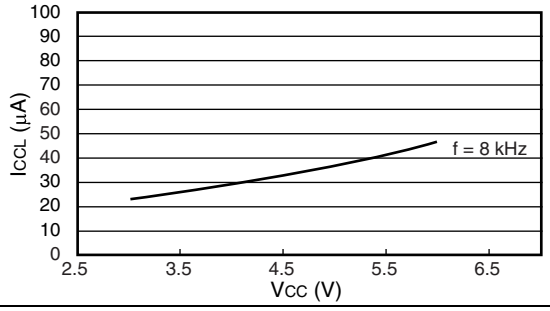
$I_{CC} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



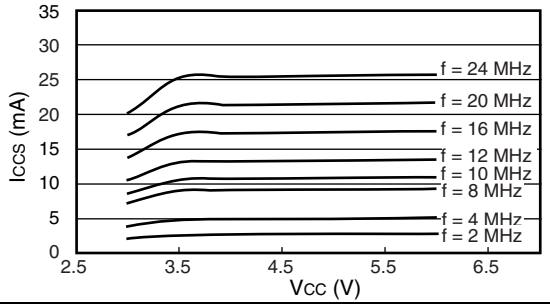
$I_{CCL} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



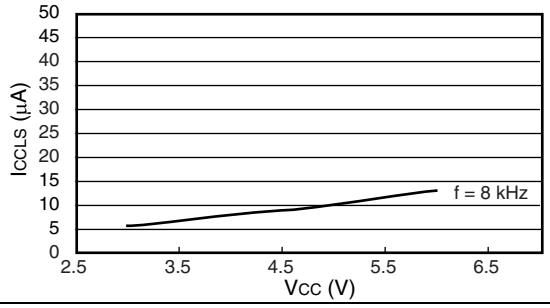
$I_{CCS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



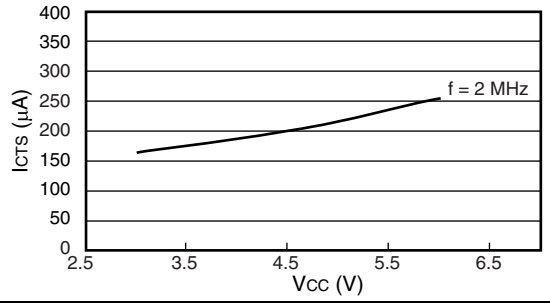
$I_{CCLS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



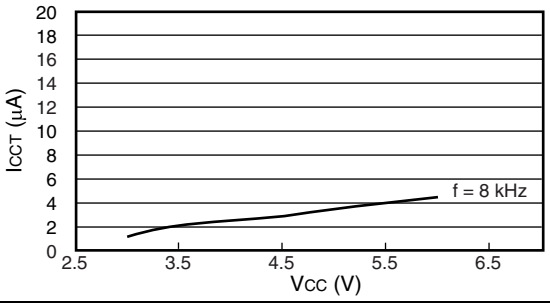
$I_{CTS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



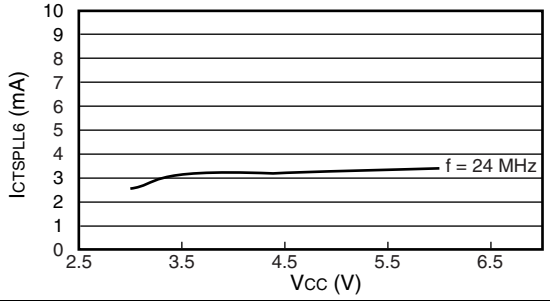
$I_{CCT} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



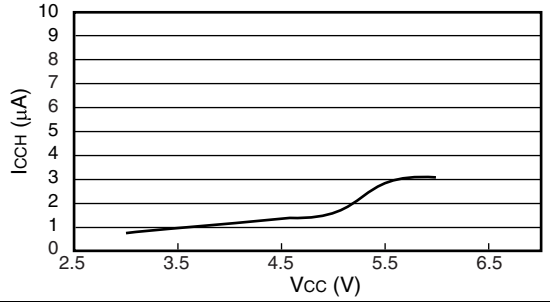
$I_{CTSPLL6} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



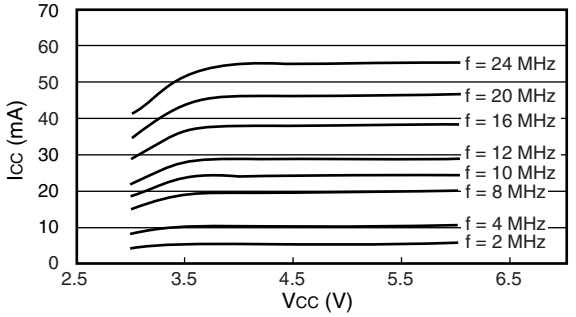
$I_{CCH} - V_{CC}$

$T_A = +25°C$, stopped

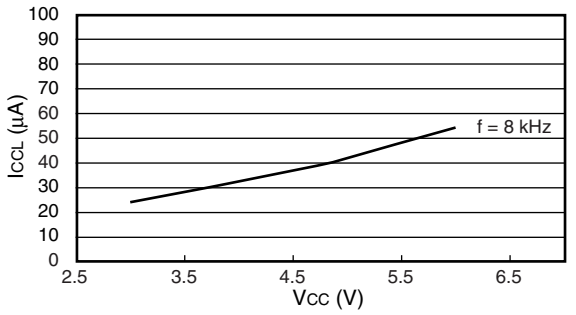


■ MB90346E, MB90346ES, MB90346CE, MB90346CES

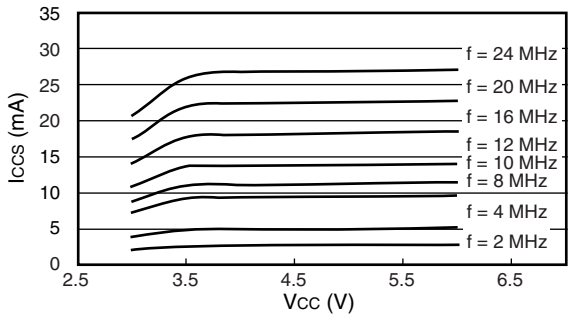
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



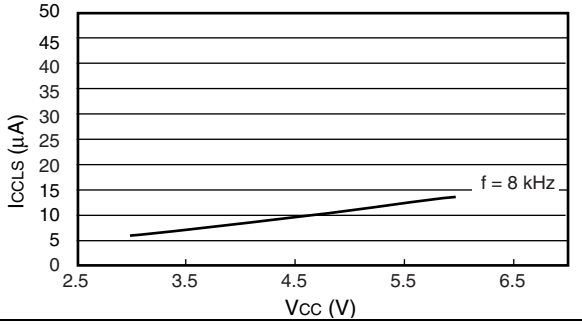
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



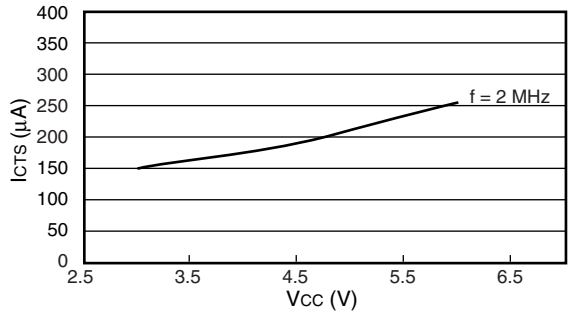
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



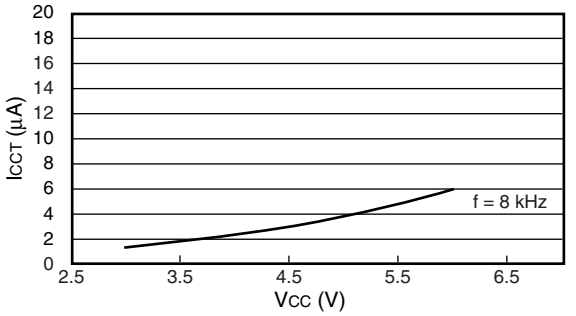
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



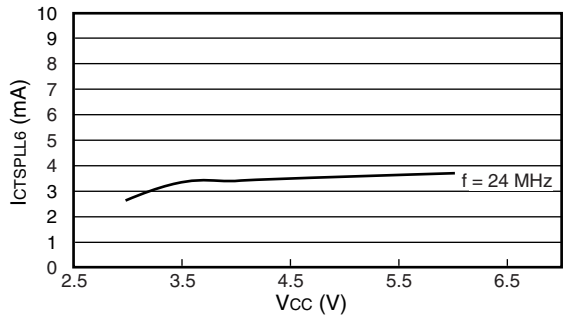
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



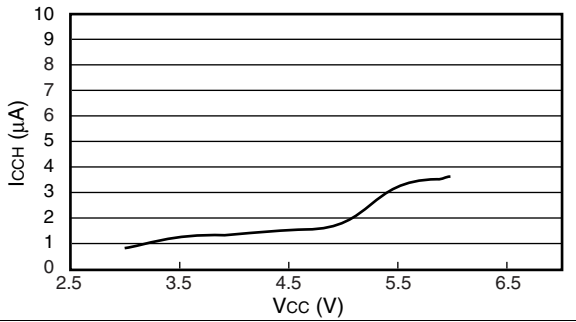
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped



Part number	Package	Remarks
MB90F347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F347ESPF		
MB90F347CEPF		
MB90F347CESPF		
MB90F347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F347ESPMC		
MB90F347CEPMC		
MB90F347CESPMC		
MB90F349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F349ESPF		
MB90F349CEPF		
MB90F349CESPF		
MB90F349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F349ESPMC		
MB90F349CEPMC		
MB90F349CESPMC		
MB90341EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90341ESPF		
MB90341CEPF		
MB90341CESPF		
MB90341EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90341ESPMC		
MB90341CEPMC		
MB90341CESPMC		
MB90342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90342ESPF		
MB90342CEPF		
MB90342CESPF		
MB90342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90342ESPMC		
MB90342CEPMC		
MB90342CESPMC		

(Continued)

15. Major Changes

Spansiion Publication Number: DS07-13747-4E

Page	Section	Change Results
___	___	Deleted the part numbers; MB90F343E(S), MB90F343CE(S)
51	Electrical Characteristics Absolute Maximum Ratings	Added “*6” in remark for “L" level maximum output current and “H” level maximum output current. Added “*7” in remark for “L" level average output current and “H” level average output current. Added “*8” in remark for “L"level average overall output current and “H” level average overall output current.
52		Added as follows. “*6:The maximum output current is defined as the peak value of the current of any one of the corresponding pins.” “*7:The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.” “*8:The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.”

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90340E Series F2MC-16LX 16-bit Microcontroller Datasheet Document Number: 002-04498				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	08/23/2010	Migrated to Cypress and assigned document number 002-04498. No change to document contents or format.
*A	5221535	AKIH	05/04/2016	Updated to Cypress template