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What is "[Embedded - Microcontrollers](#)"?

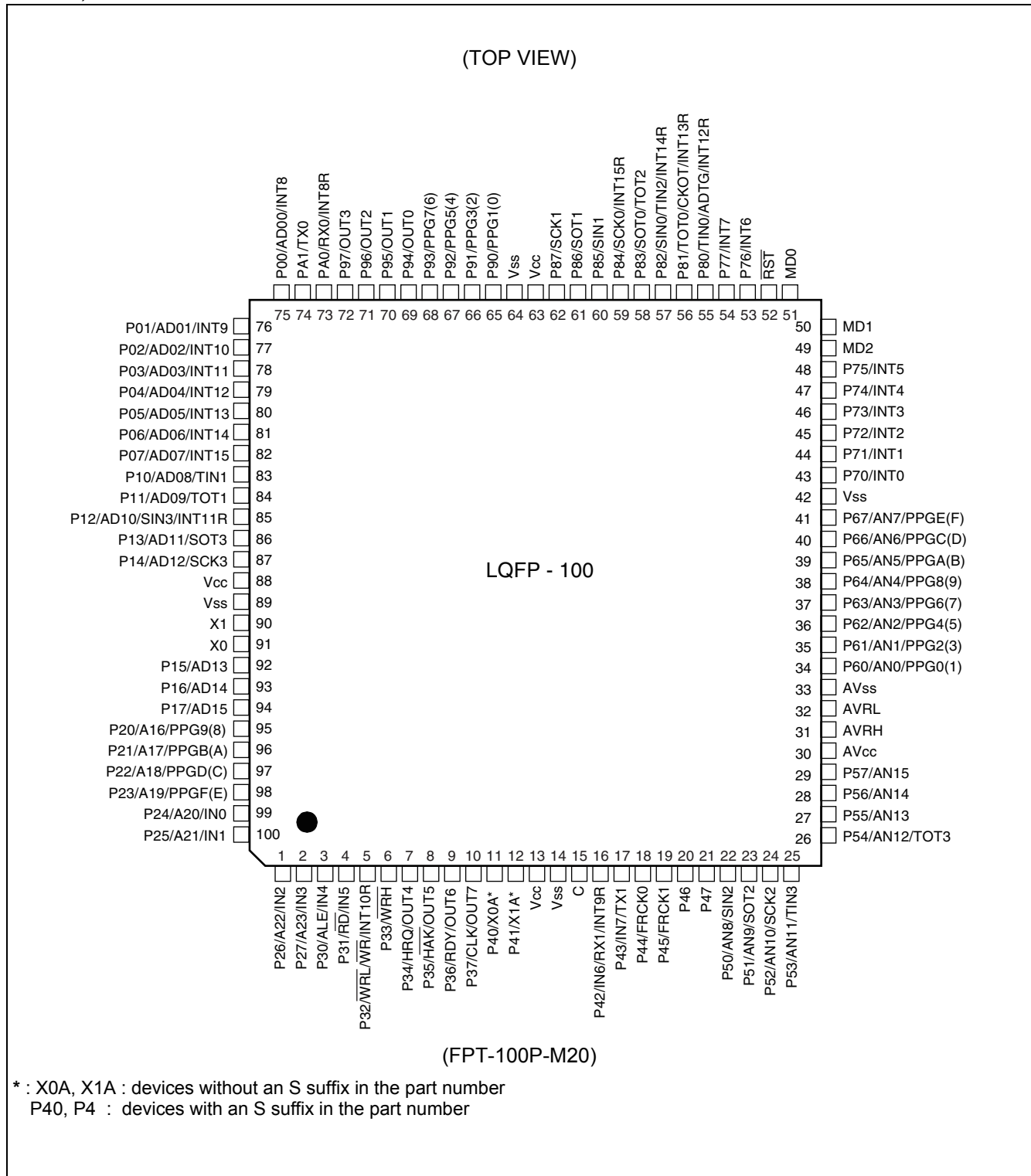
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

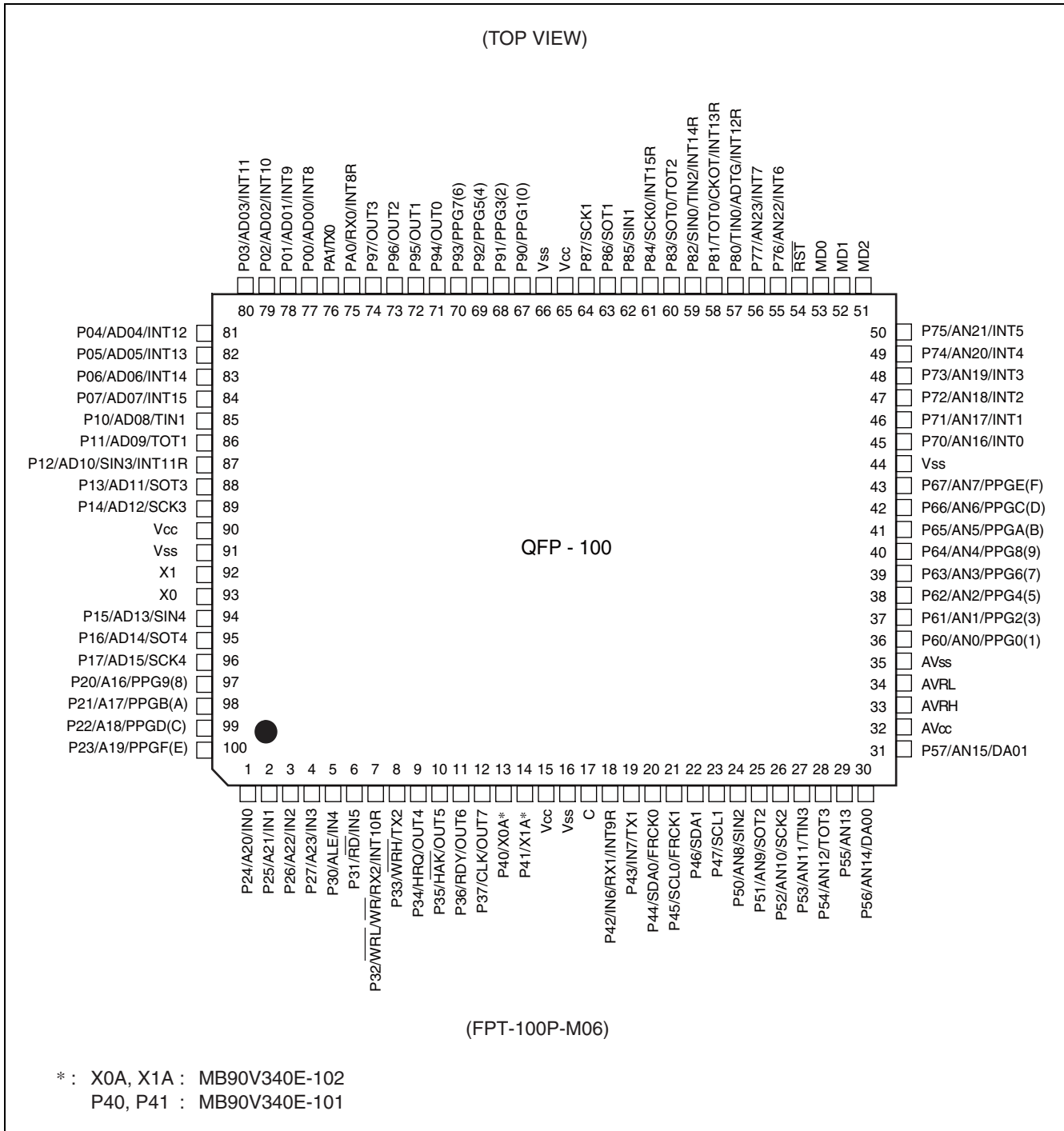
Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 24x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90349cepf-g-353e1

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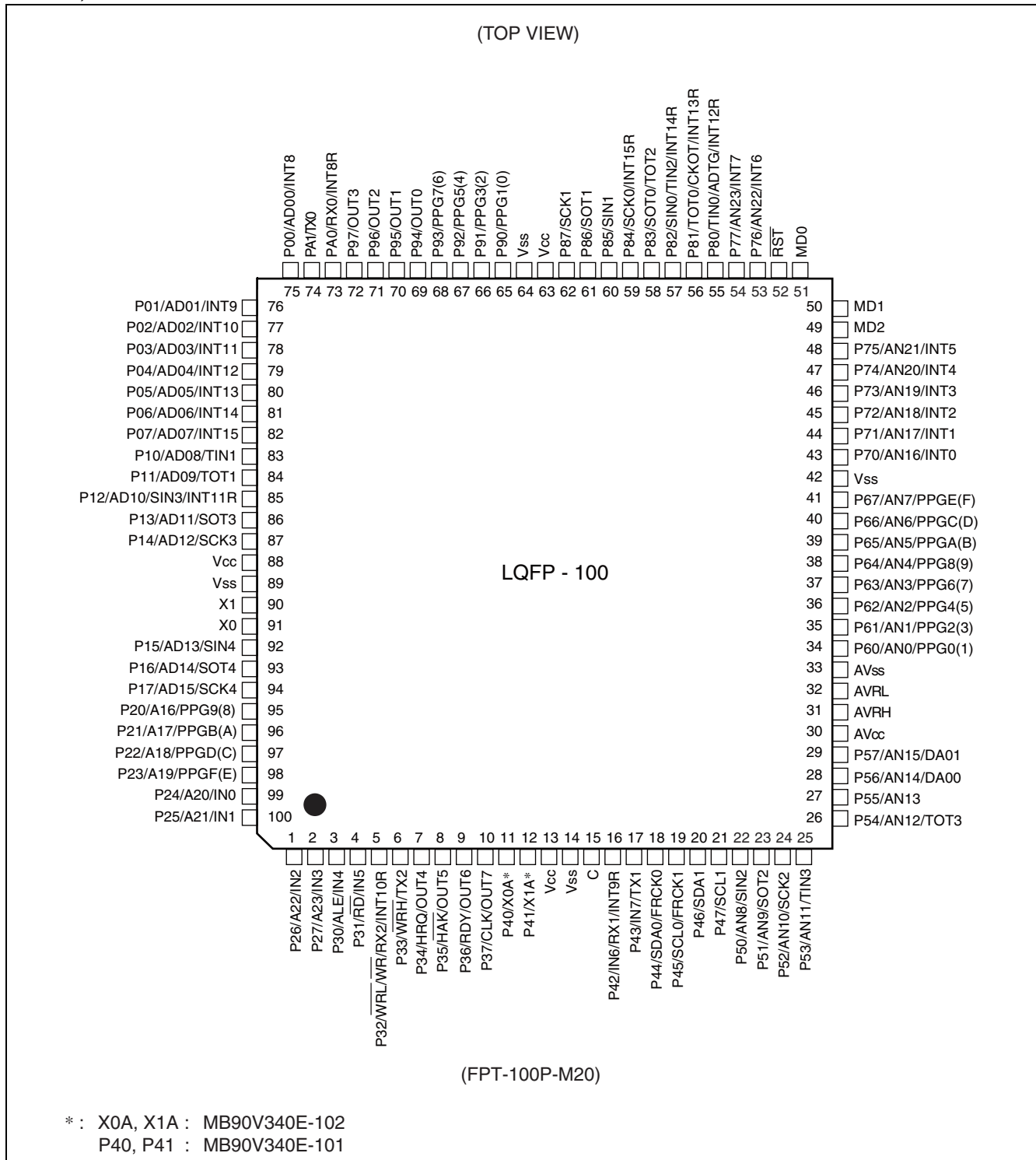
■ MB90V340E-101/MB90V340E-102



This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

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This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101)
		X0A, X1A	B	Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102)
15	13	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
16	14	V _{SS}	—	GND pin
17	15	C	K	This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 μF .
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture.
		RX1		RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only)
		INT9R		External interrupt request input pin

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV _{CC}	K	Analog power input pin for the A/D Converter

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Address	Register	Abbreviation	Access	Resource name	Initial value
0000A5 _H	Automatic Ready Function Select Register	ARSR	W	External Memory Access	0011XX00 _B
0000A6 _H	External Address Output Control Register	HACR	W		00000000 _B
0000A7 _H	Bus Control Signal Selection Register	ECSR	W		0000000X _B
0000A8 _H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXXX11 _B
0000A9 _H	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	1XX00100 _B
0000AA _H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 _B
0000AB _H	Reserved				
0000AC _H	DMA Enable L Register	DERL	R/W	DMA	00000000 _B
0000AD _H	DMA Enable H Register	DERH	R/W		00000000 _B
0000AE _H	Flash Control Status Register (Flash memory devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000 _B
0000AF _H	Reserved				
0000B0 _H	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111 _B
0000B1 _H	Interrupt Control Register 01	ICR01	W,R/W		00000111 _B
0000B2 _H	Interrupt Control Register 02	ICR02	W,R/W		00000111 _B
0000B3 _H	Interrupt Control Register 03	ICR03	W,R/W		00000111 _B
0000B4 _H	Interrupt Control Register 04	ICR04	W,R/W		00000111 _B
0000B5 _H	Interrupt Control Register 05	ICR05	W,R/W		00000111 _B
0000B6 _H	Interrupt Control Register 06	ICR06	W,R/W		00000111 _B
0000B7 _H	Interrupt Control Register 07	ICR07	W,R/W		00000111 _B
0000B8 _H	Interrupt Control Register 08	ICR08	W,R/W		00000111 _B
0000B9 _H	Interrupt Control Register 09	ICR09	W,R/W		00000111 _B
0000BA _H	Interrupt Control Register 10	ICR10	W,R/W		00000111 _B
0000BB _H	Interrupt Control Register 11	ICR11	W,R/W		00000111 _B
0000BC _H	Interrupt Control Register 12	ICR12	W,R/W		00000111 _B
0000BD _H	Interrupt Control Register 13	ICR13	W,R/W		00000111 _B
0000BE _H	Interrupt Control Register 14	ICR14	W,R/W		00000111 _B
0000BF _H	Interrupt Control Register 15	ICR15	W,R/W		00000111 _B
0000C0 _H	D/A Converter Data 0	DAT0	R/W	D/A Converter	XXXXXXXX _B
0000C1 _H	D/A Converter Data 1	DAT1	R/W		XXXXXXXX _B
0000C2 _H	D/A Control 0	DACR0	R/W		XXXXXXXX0 _B
0000C3 _H	D/A Control 1	DACR1	R/W		XXXXXXXX0 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007900 _H	Reload Register L0	PRL0	R/W	16-bit PPG 0/1	XXXXXXXX _B
007901 _H	Reload Register H0	PRLH0	R/W		XXXXXXXX _B
007902 _H	Reload Register L1	PRL1	R/W		XXXXXXXX _B
007903 _H	Reload Register H1	PRLH1	R/W		XXXXXXXX _B
007904 _H	Reload Register L2	PRL2	R/W	16-bit PPG 2/3	XXXXXXXX _B
007905 _H	Reload Register H2	PRLH2	R/W		XXXXXXXX _B
007906 _H	Reload Register L3	PRL3	R/W		XXXXXXXX _B
007907 _H	Reload Register H3	PRLH3	R/W		XXXXXXXX _B
007908 _H	Reload Register L4	PRL4	R/W	16-bit PPG 4/5	XXXXXXXX _B
007909 _H	Reload Register H4	PRLH4	R/W		XXXXXXXX _B
00790A _H	Reload Register L5	PRL5	R/W		XXXXXXXX _B
00790B _H	Reload Register H5	PRLH5	R/W		XXXXXXXX _B
00790C _H	Reload Register L6	PRL6	R/W	16-bit PPG 6/7	XXXXXXXX _B
00790D _H	Reload Register H6	PRLH6	R/W		XXXXXXXX _B
00790E _H	Reload Register L7	PRL7	R/W		XXXXXXXX _B
00790F _H	Reload Register H7	PRLH7	R/W		XXXXXXXX _B
007910 _H	Reload Register L8	PRL8	R/W	16-bit PPG 8/9	XXXXXXXX _B
007911 _H	Reload Register H8	PRLH8	R/W		XXXXXXXX _B
007912 _H	Reload Register L9	PRL9	R/W		XXXXXXXX _B
007913 _H	Reload Register H9	PRLH9	R/W		XXXXXXXX _B
007914 _H	Reload Register LA	PRLA	R/W	16-bit PPG A/B	XXXXXXXX _B
007915 _H	Reload Register HA	PRLHA	R/W		XXXXXXXX _B
007916 _H	Reload Register LB	PRLB	R/W		XXXXXXXX _B
007917 _H	Reload Register HB	PRLHB	R/W		XXXXXXXX _B
007918 _H	Reload Register LC	PRLC	R/W	16-bit PPG C/D	XXXXXXXX _B
007919 _H	Reload Register HC	PRLHC	R/W		XXXXXXXX _B
00791A _H	Reload Register LD	PRLD	R/W		XXXXXXXX _B
00791B _H	Reload Register HD	PRLHD	R/W		XXXXXXXX _B
00791C _H	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	XXXXXXXX _B
00791D _H	Reload Register HE	PRLHE	R/W		XXXXXXXX _B
00791E _H	Reload Register LF	PRLLF	R/W		XXXXXXXX _B
00791F _H	Reload Register HF	PRLHF	R/W		XXXXXXXX _B
007920 _H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
007921 _H	Input Capture 0	IPCP0	R		XXXXXXXX _B
007922 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
007923 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B

(Continued)

List of Message Buffers (ID Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A00 _H to 007A1F _H	007C00 _H to 007C1F _H	General- Purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
007A20 _H	007C20 _H	ID Register 0	IDR0	R/W	XXXXXXXX _B XXXXXXXX _B
007A21 _H	007C21 _H				XXXXXXXX _B XXXXXXXX _B
007A22 _H	007C22 _H				XXXXXXXX _B XXXXXXXX _B
007A23 _H	007C23 _H				XXXXXXXX _B XXXXXXXX _B
007A24 _H	007C24 _H	ID Register 1	IDR1	R/W	XXXXXXXX _B XXXXXXXX _B
007A25 _H	007C25 _H				XXXXXXXX _B XXXXXXXX _B
007A26 _H	007C26 _H				XXXXXXXX _B XXXXXXXX _B
007A27 _H	007C27 _H				XXXXXXXX _B XXXXXXXX _B
007A28 _H	007C28 _H	ID Register 2	IDR2	R/W	XXXXXXXX _B XXXXXXXX _B
007A29 _H	007C29 _H				XXXXXXXX _B XXXXXXXX _B
007A2A _H	007C2A _H				XXXXXXXX _B XXXXXXXX _B
007A2B _H	007C2B _H				XXXXXXXX _B XXXXXXXX _B
007A2C _H	007C2C _H	ID Register 3	IDR3	R/W	XXXXXXXX _B XXXXXXXX _B
007A2D _H	007C2D _H				XXXXXXXX _B XXXXXXXX _B
007A2E _H	007C2E _H				XXXXXXXX _B XXXXXXXX _B
007A2F _H	007C2F _H				XXXXXXXX _B XXXXXXXX _B
007A30 _H	007C30 _H	ID Register 4	IDR4	R/W	XXXXXXXX _B XXXXXXXX _B
007A31 _H	007C31 _H				XXXXXXXX _B XXXXXXXX _B
007A32 _H	007C32 _H				XXXXXXXX _B XXXXXXXX _B
007A33 _H	007C33 _H				XXXXXXXX _B XXXXXXXX _B
007A34 _H	007C34 _H	ID Register 5	IDR5	R/W	XXXXXXXX _B XXXXXXXX _B
007A35 _H	007C35 _H				XXXXXXXX _B XXXXXXXX _B
007A36 _H	007C36 _H				XXXXXXXX _B XXXXXXXX _B
007A37 _H	007C37 _H				XXXXXXXX _B XXXXXXXX _B
007A38 _H	007C38 _H	ID Register 6	IDR6	R/W	XXXXXXXX _B XXXXXXXX _B
007A39 _H	007C39 _H				XXXXXXXX _B XXXXXXXX _B
007A3A _H	007C3A _H				XXXXXXXX _B XXXXXXXX _B
007A3B _H	007C3B _H				XXXXXXXX _B XXXXXXXX _B
007A3C _H	007C3C _H	ID Register 7	IDR7	R/W	XXXXXXXX _B XXXXXXXX _B
007A3D _H	007C3D _H				XXXXXXXX _B XXXXXXXX _B
007A3E _H	007C3E _H				XXXXXXXX _B XXXXXXXX _B
007A3F _H	007C3F _H				XXXXXXXX _B XXXXXXXX _B

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A60 _H	007C60 _H	DLC Register 0	DLCR0	R/W	XXXXXXXX _B
007A61 _H	007C61 _H				
007A62 _H	007C62 _H				
007A63 _H	007C63 _H	DLC Register 1	DLCR1	R/W	XXXXXXXX _B
007A64 _H	007C64 _H				
007A65 _H	007C65 _H				
007A66 _H	007C66 _H	DLC Register 2	DLCR2	R/W	XXXXXXXX _B
007A67 _H	007C67 _H				
007A68 _H	007C68 _H				
007A69 _H	007C69 _H	DLC Register 3	DLCR3	R/W	XXXXXXXX _B
007A6A _H	007C6A _H				
007A6B _H	007C6B _H				
007A6C _H	007C6C _H	DLC Register 4	DLCR4	R/W	XXXXXXXX _B
007A6D _H	007C6D _H				
007A6E _H	007C6E _H				
007A6F _H	007C6F _H	DLC Register 5	DLCR5	R/W	XXXXXXXX _B
007A70 _H	007C70 _H				
007A71 _H	007C71 _H				
007A72 _H	007C72 _H	DLC Register 6	DLCR6	R/W	XXXXXXXX _B
007A73 _H	007C73 _H				
007A74 _H	007C74 _H				
007A75 _H	007C75 _H	DLC Register 7	DLCR7	R/W	XXXXXXXX _B
007A76 _H	007C76 _H				
007A77 _H	007C77 _H				
007A78 _H	007C78 _H	DLC Register 8	DLCR8	R/W	XXXXXXXX _B
007A79 _H	007C79 _H				
007A7A _H	007C7A _H				
007A7B _H	007C7B _H	DLC Register 9	DLCR9	R/W	XXXXXXXX _B
007A7C _H	007C7C _H				
007A7D _H	007C7D _H				
007A7E _H	007C7E _H	DLC Register 10	DLCR10	R/W	XXXXXXXX _B
007A7F _H	007C7F _H				
007A70 _H	007C70 _H	DLC Register 11	DLCR11	R/W	XXXXXXXX _B
007A71 _H	007C71 _H				
007A72 _H	007C72 _H				
007A73 _H	007C73 _H	DLC Register 12	DLCR12	R/W	XXXXXXXX _B
007A74 _H	007C74 _H				
007A75 _H	007C75 _H				
007A76 _H	007C76 _H	DLC Register 13	DLCR13	R/W	XXXXXXXX _B
007A77 _H	007C77 _H				
007A78 _H	007C78 _H				
007A79 _H	007C79 _H	DLC Register 14	DLCR14	R/W	XXXXXXXX _B
007A7A _H	007C7A _H				
007A7B _H	007C7B _H				
007A7C _H	007C7C _H	DLC Register 15	DLCR15	R/W	XXXXXXXX _B
007A7D _H	007C7D _H				
007A7E _H	007C7E _H				
007A7F _H	007C7F _H				

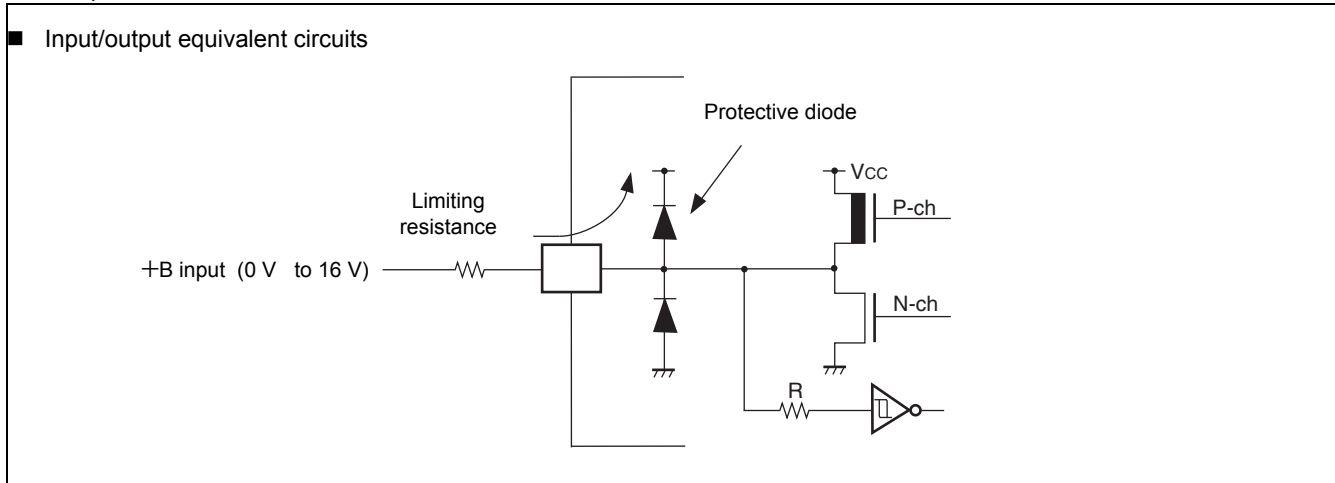
10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI ² OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC _H	—	—
INT9 instruction	N	—	#09	FFFFD8 _H	—	—
Exception	N	—	#10	FFFFD4 _H	—	—
CAN 0 RX	N	—	#11	FFFFD0 _H	ICR00	0000B0 _H
CAN 0 TX/NS	N	—	#12	FFFFCC _H		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4 _H		
CAN 2 RX / I ² C0	N	—	#15	FFFFC0 _H	ICR02	0000B2 _H
CAN 2 TX/NS	N	—	#16	FFFFBC _H		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8 _H	ICR03	0000B3 _H
16-bit Reload Timer 1	Y1	1	#18	FFFFB4 _H		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0 _H	ICR04	0000B4 _H
16-bit Reload Timer 3	Y1	—	#20	FFFFAC _H		
PPG 0/1/4/5	N	—	#21	FFFFA8 _H	ICR05	0000B5 _H
PPG 2/3/6/7	N	—	#22	FFFFA4 _H		
PPG 8/9/C/D	N	—	#23	FFFFA0 _H	ICR06	0000B6 _H
PPG A/B/E/F	N	—	#24	FFFF9C _H		
Time Base Timer	N	—	#25	FFFF98 _H	ICR07	0000B7 _H
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94 _H		
Watch Timer	N	—	#27	FFFF90 _H	ICR08	0000B8 _H
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C _H		
A/D Converter	Y1	5	#29	FFFF88 _H	ICR09	0000B9 _H
Free-run Timer 0 / Free-run Timer 1	N	—	#30	FFFF84 _H		
Input Capture 4/5 / I ² C1	Y1	6	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C _H		
Input Capture 0 to 3	Y1	8	#33	FFFF78 _H	ICR11	0000BB _H
Output Compare 2/3/6/7	Y1	9	#34	FFFF74 _H		
UART 0 RX	Y2	10	#35	FFFF70 _H	ICR12	0000BC _H
UART 0 TX	Y1	11	#36	FFFF6C _H		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68 _H	ICR13	0000BD _H
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64 _H		

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- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:



*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

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($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

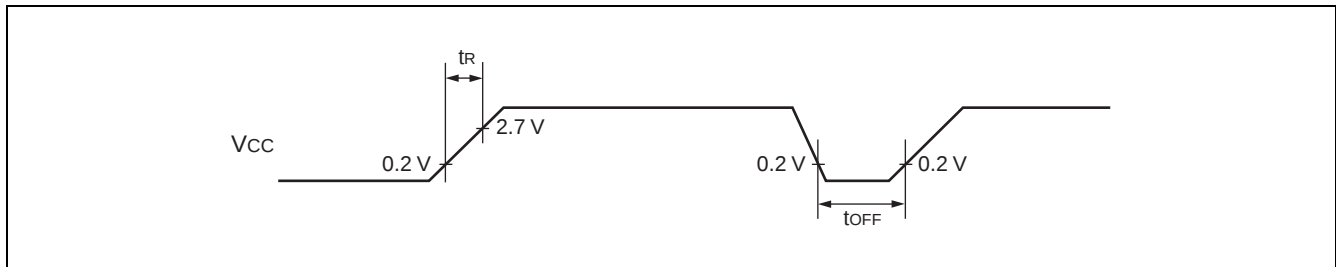
Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	—	$V_{CC} = 5.5\text{ V}$, $V_{SS} < V_I < V_{CC}$	-1	—	+1	μA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{\text{RST}}$	—	25	50	100	$\text{k}\Omega$	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	$\text{k}\Omega$	Except Flash memory devices
Power supply current*	I_{CC}	V_{CC}	$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At normal operation.	—	55	70	mA	
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At writing Flash memory.	—	70	85	mA	Flash memory devices
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At erasing Flash memory.	—	75	90	mA	Flash memory devices
	I_{CCS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, In Sleep mode.	—	25	35	mA	
	I_{CTS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 2 MHz, In Main Timer mode	—	0.3	0.8	mA	
	$I_{CTSPLL6}$		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, In PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In sub operation $T_A = +25^{\circ}\text{C}$	—	70	140	μA	
	I_{CCLS}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In sub sleep $T_A = +25^{\circ}\text{C}$	—	20	50	μA	
	I_{CCT}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In watch mode $T_A = +25^{\circ}\text{C}$	—	10	35	μA	
	I_{CCH}		$V_{CC} = 5.0\text{ V}$, In Stop mode, $T_A = +25^{\circ}\text{C}$	—	7	25	μA	
Input capacitance	C_{IN}	Other than C, AV_{CC} , AV_{SS} , $AVRH$, $AVRL$, V_{CC} , V_{SS}	—	—	5	15	pF	

* : The power supply current is measured with an external clock.

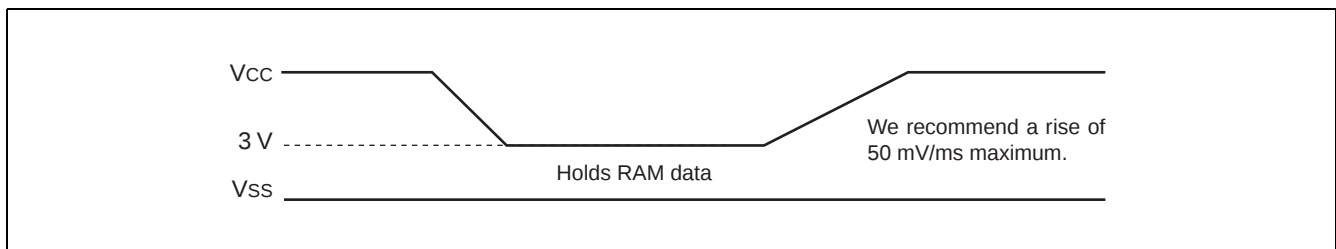
11.4.3 Power On Reset

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}	—	1	—	ms	Waiting time until power-on



Note: : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



11.4.4 Clock Output Timing

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	$f_{CP} = 16\text{ MHz}$
				41.67	—	ns	$f_{CP} = 24\text{ MHz}$
CLK $\uparrow \rightarrow$ CLK $\downarrow$	t_{CHCL}	CLK	—	20	—	ns	$f_{CP} = 16\text{ MHz}$
				13	—	ns	$f_{CP} = 24\text{ MHz}$

11.4.9 LIN-UART0/1/2/3

■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0

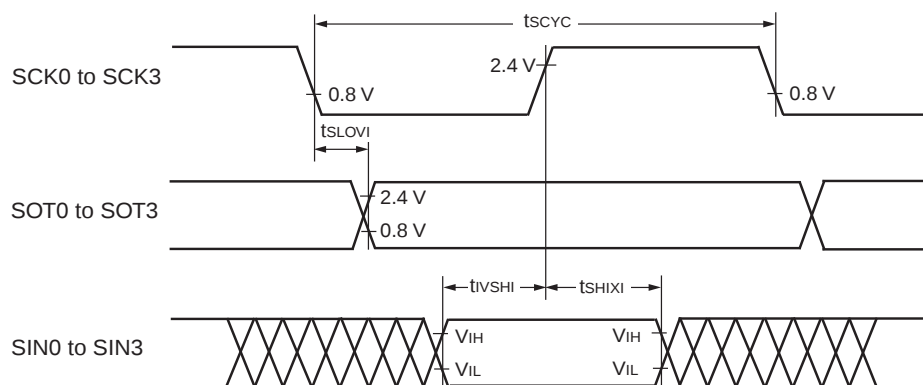
($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock "L" pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$3 t_{CP} - t_R$	—	ns
Serial clock "H" pulse width	t_{SLSH}	SCK0 to SCK3		$t_{CP} + 10$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	$2 t_{CP} + 60$	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SIN0 to SIN3		$t_{CP} + 30$	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

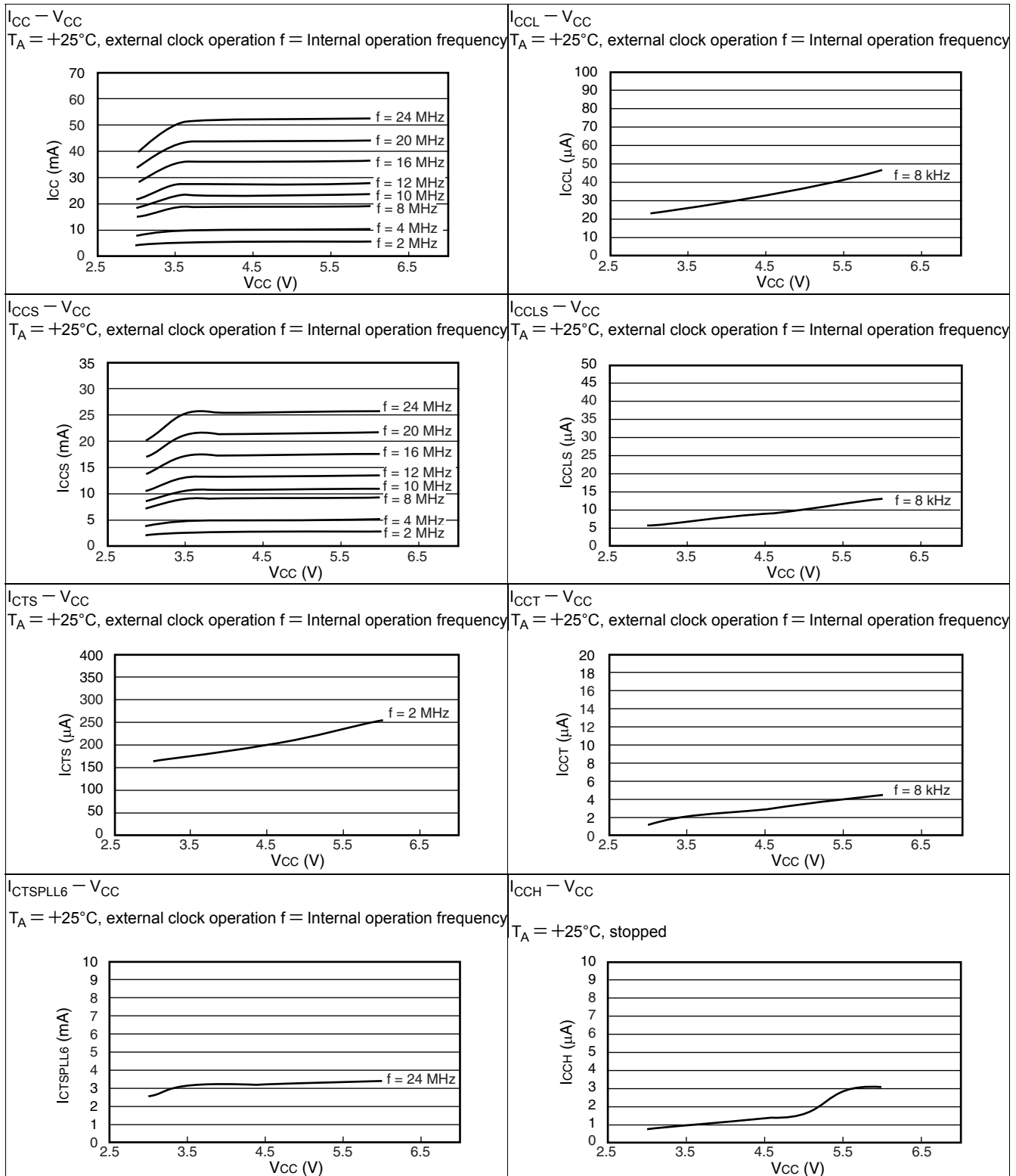
Note:

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “(1) Clock Timing”.

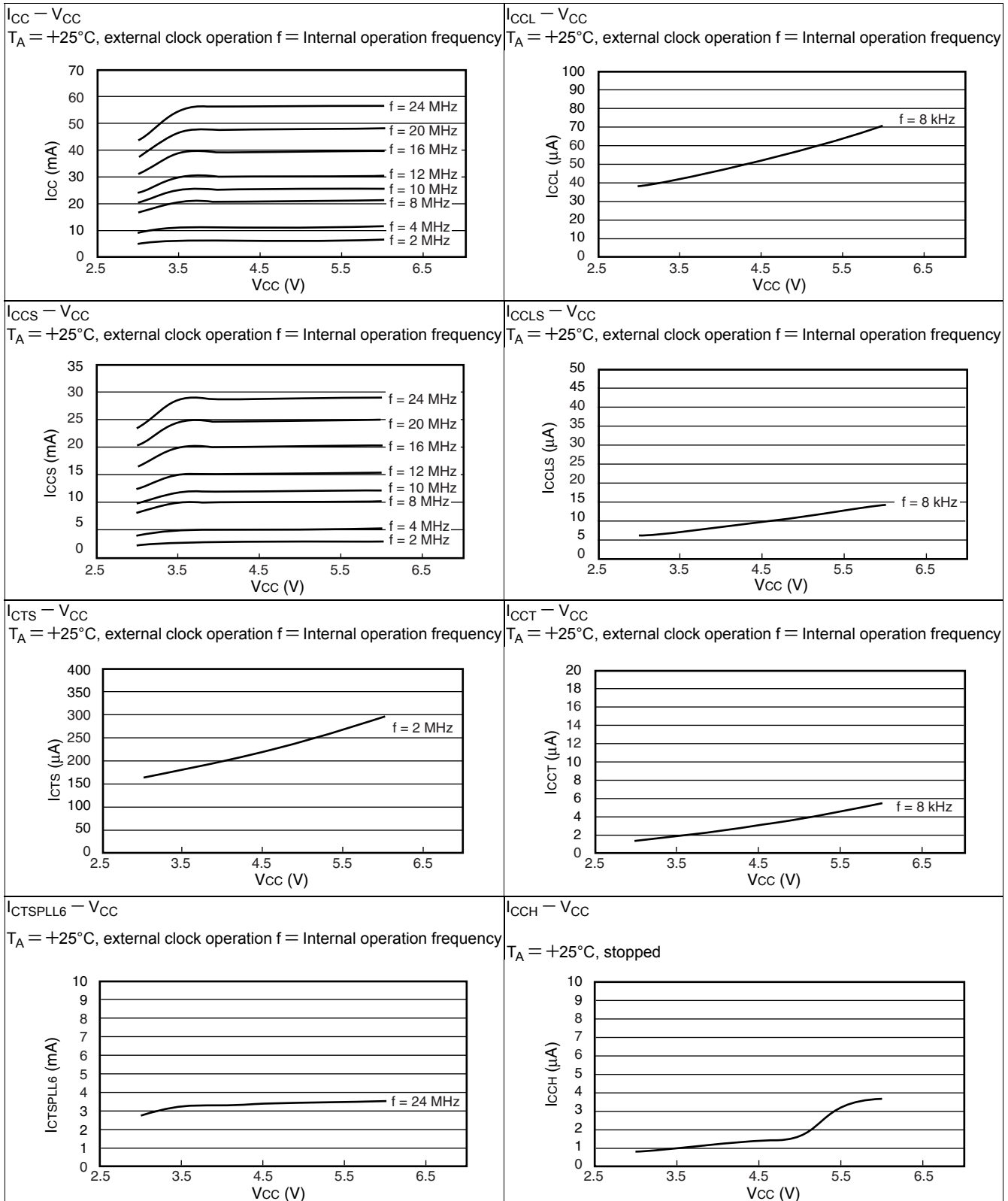
• Internal Shift Clock Mode



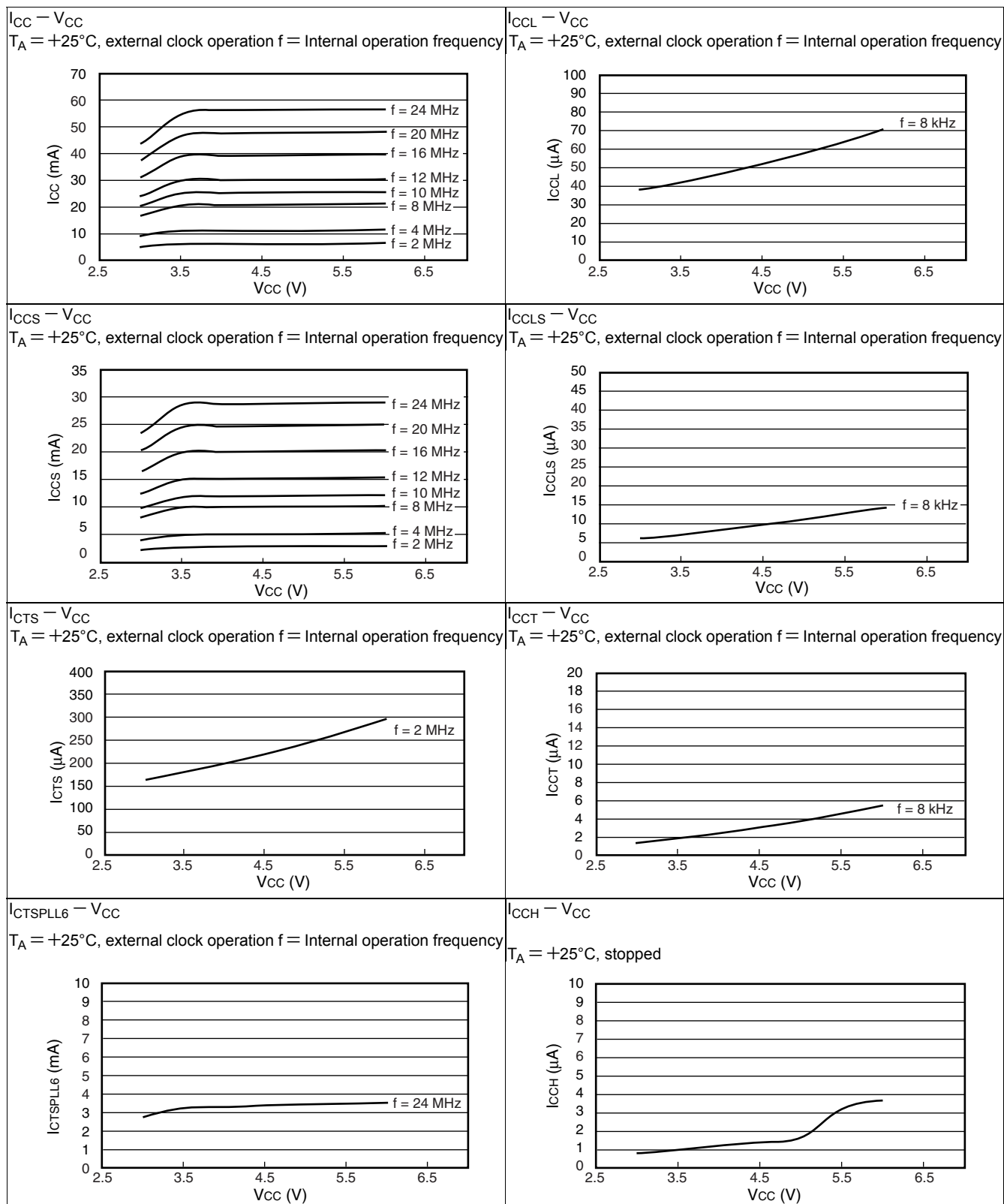
■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES



■ MB90F349E, MB90F349ES, MB90F349CE, MB90F349CES

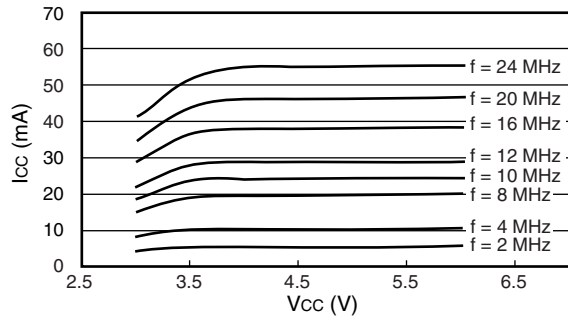


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

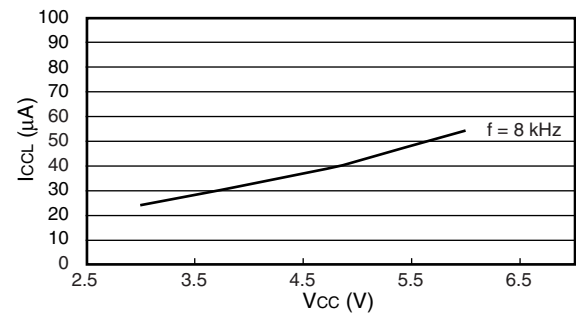


■ MB90347E, MB90347ES, MB90347CE, MB90347CES

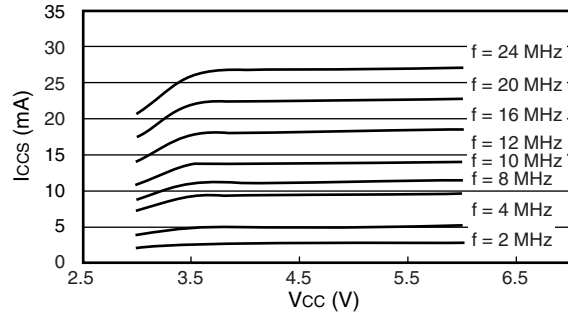
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



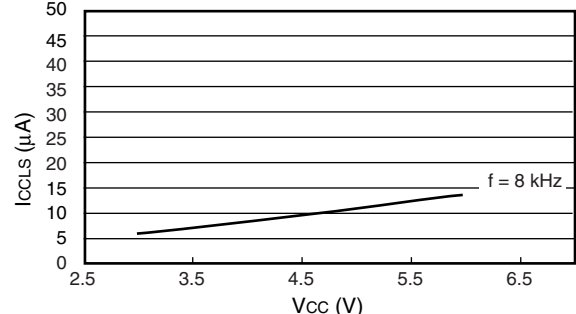
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



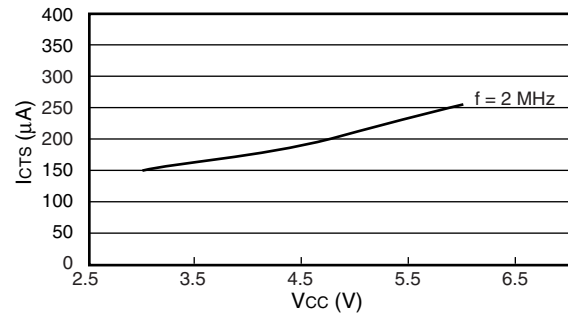
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



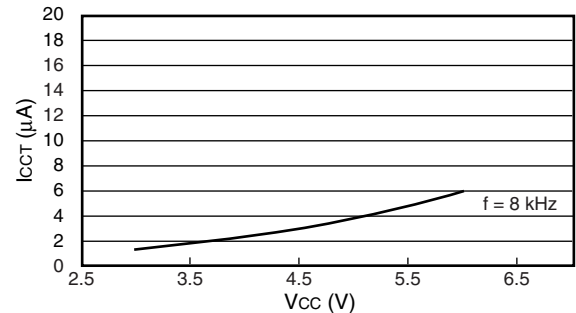
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



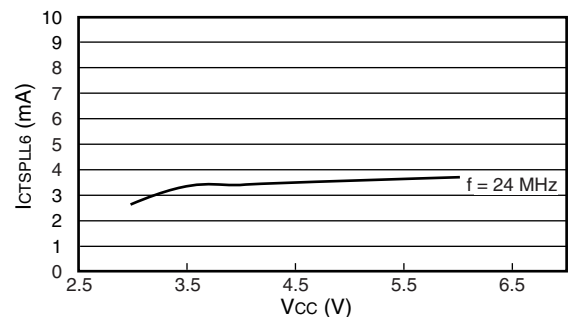
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



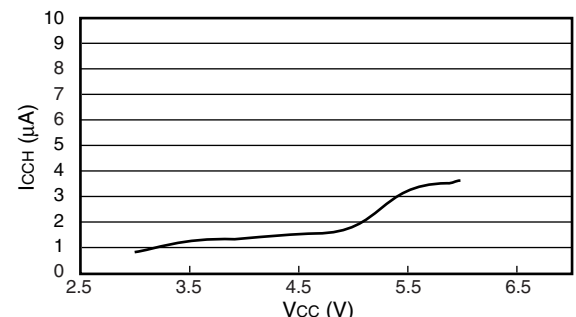
$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped



Part number	Package	Remarks
MB90F347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F347ESPF		
MB90F347CEPF		
MB90F347CESPF		
MB90F347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F347ESPMC		
MB90F347CEPMC		
MB90F347CESPMC		
MB90F349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F349ESPF		
MB90F349CEPF		
MB90F349CESPF		
MB90F349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F349ESPMC		
MB90F349CEPMC		
MB90F349CESPMC		
MB90341EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90341ESPF		
MB90341CEPF		
MB90341CESPF		
MB90341EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90341ESPMC		
MB90341CEPMC		
MB90341CESPMC		
MB90342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90342ESPF		
MB90342CEPF		
MB90342CESPF		
MB90342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90342ESPMC		
MB90342CEPMC		
MB90342CESPMC		

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