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What is "Embedded - Microcontrollers"?

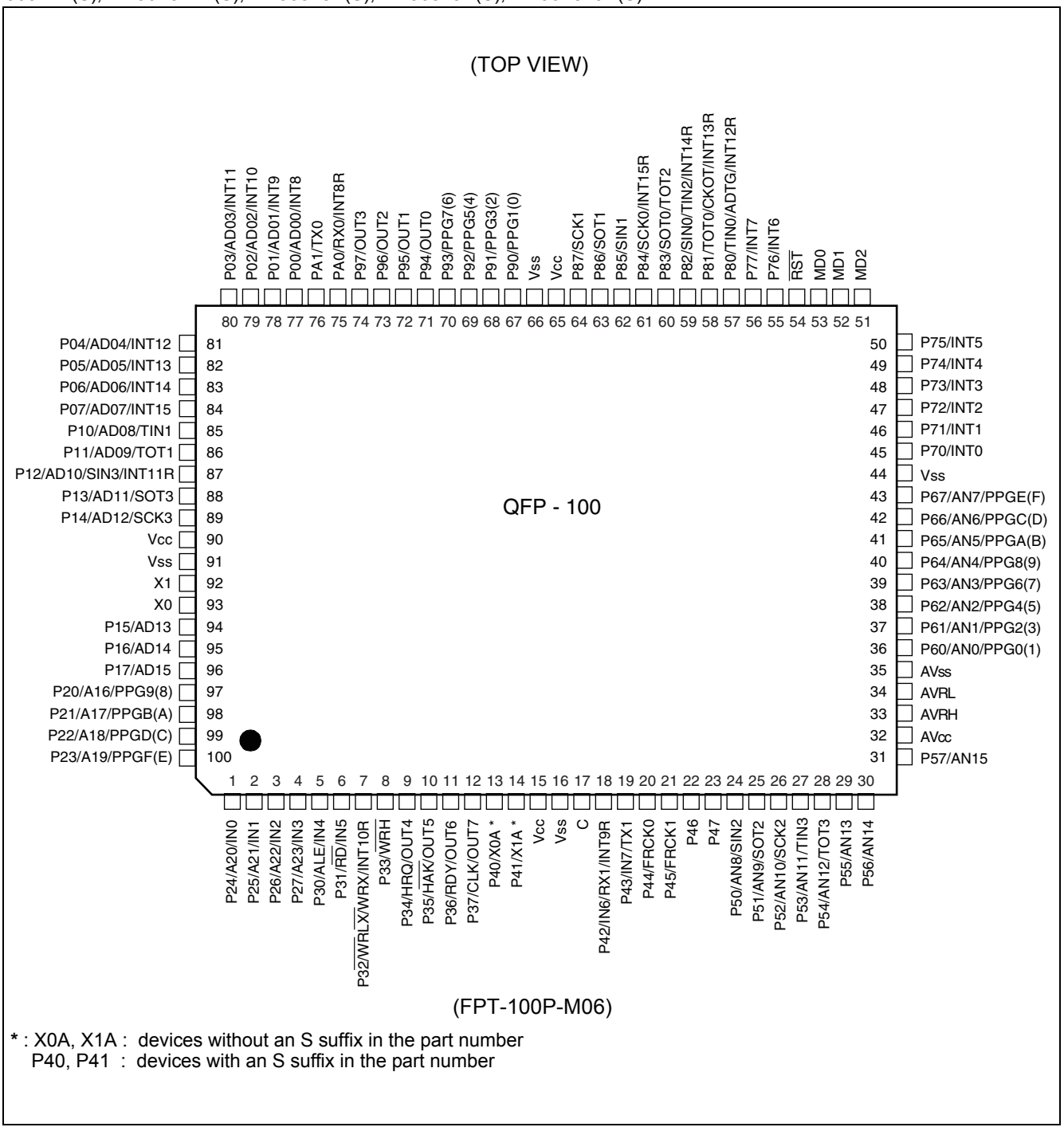
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 24x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90349cepf-g-408e1

2. Pin Assignments

■ MB90341E(S), MB90342E(S), MB90F342E(S), MB90F345E(S), MB90346E(S), MB90F346E(S), MB90347E(S), MB90F347E(S), MB90348E(S), MB90349E(S), MB90F349E(S)



(FPT-100P-M06)

***** : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter
35	33	AV_{SS}	K	Analog GND pin for the A/D Converter
36 to 43	34 to 41	P60 to P67	I	General purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
44	42	V_{SS}	—	GND pin
45 to 50	43 to 48	P70 to P75	I	General purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT0 to INT5		External interrupt request input pins
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	$\overline{RST}$	E	Reset input pin
55, 56	53, 54	P76, P77	I	General purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT6, INT7		External interrupt request input pins
57	55	P80	F	General purpose I/O pin.
		TIN0		Event input pin for the reload timer
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin
58	56	P81	F	General purpose I/O pin.
		TOT0		Output pin for the reload timer
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin
59	57	P82	M	General purpose I/O pin.
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer
		INT14R		External interrupt request input pin
60	58	P83	F	General purpose I/O pin.
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer

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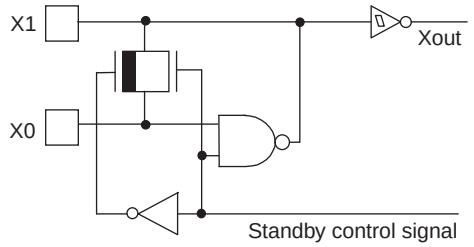
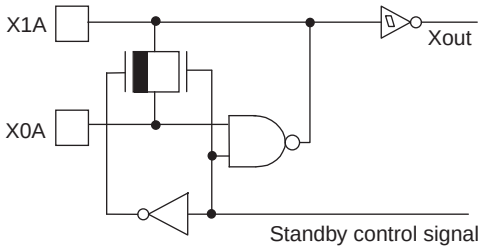
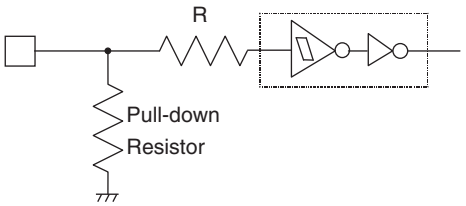
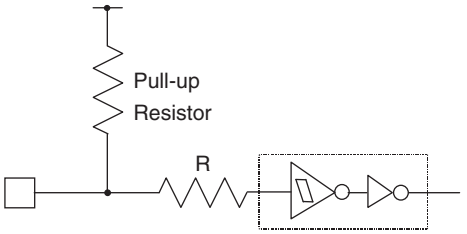
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
96	94	P17	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
97 to 100	95 to 98	P20 to P23	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9,PPGB,PPGD,PPGF		Output pins for PPGs

1 : FPT-100P-M06

2 : FPT-100P-M20

3 : For I/O circuit type, refer to “I/O Circuit Type”.

4. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		■ MASK ROM and evaluation products: CMOS hysteresis input pin ■ Flash memory products: CMOS input pin
D		MASK ROM and evaluation products: ■ CMOS hysteresis input pin ■ Pull-down resistor value: approx. 50 kΩ Flash memory products: ■ CMOS input pin ■ No pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ

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5. Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN23) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

6. Connection of Unused A/D Converter Pins when the A/D Converter is Used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

7. Crystal Oscillator Circuit

The X0, X1 pins and X0A, X1A pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

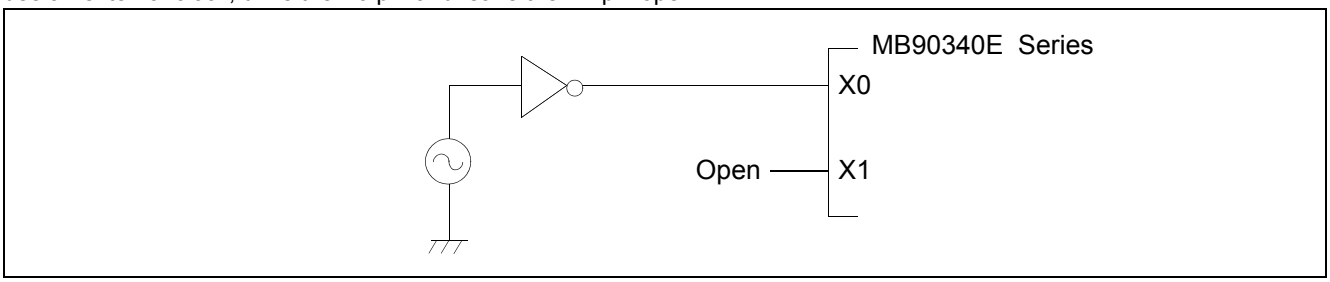
For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

8. Pull-up/down resistors

The MB90340E Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

9. Using external clock

To use an external clock, drive the X0 pin and leave the X1 pin open.



10. Precautions when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

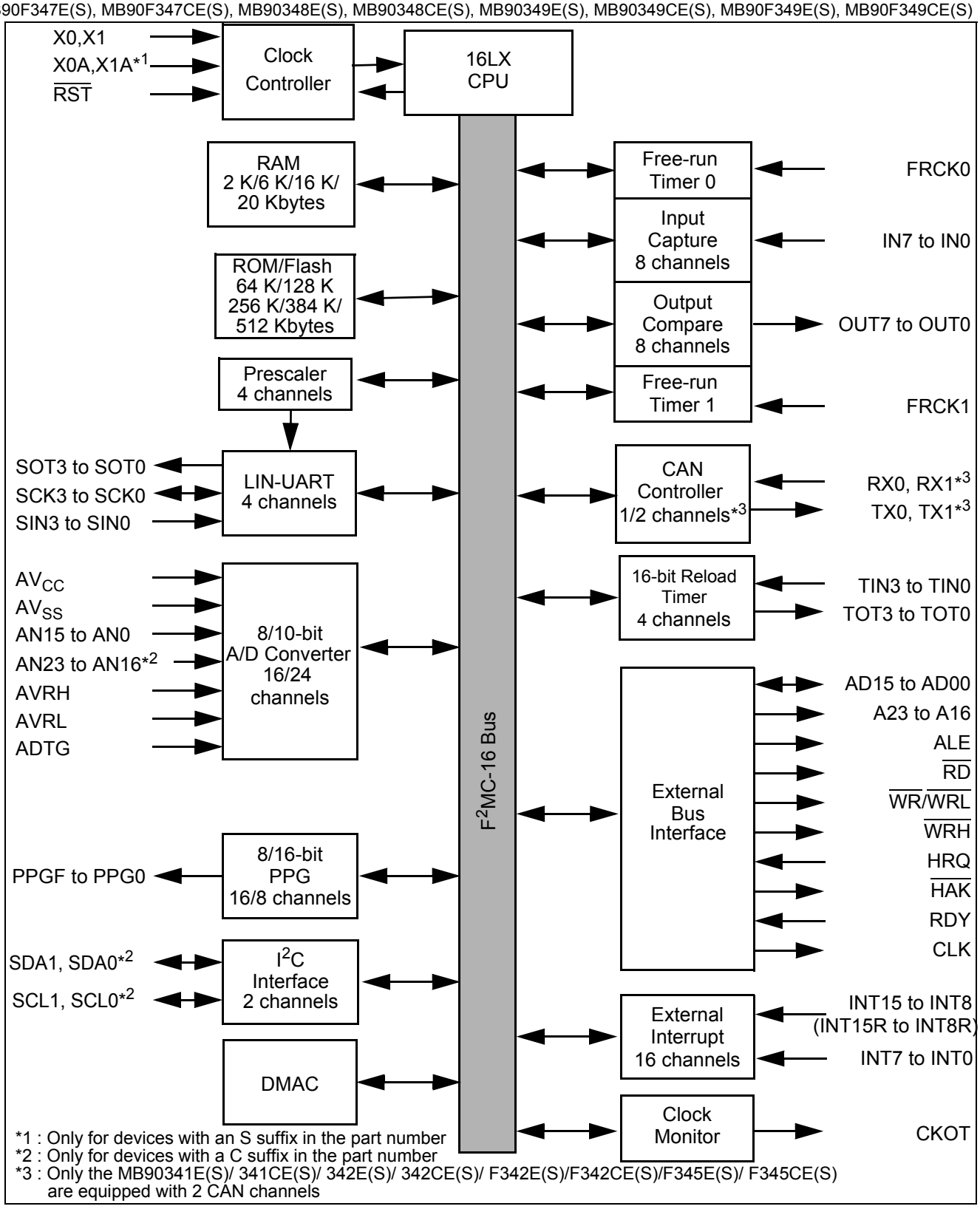
11. Notes on operation in PLL clock mode

If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

12. Notes on Power-On

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50 µs or more (0.2 V to 2.7 V)

■ MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)



Address	Register	Abbreviation	Access	Resource name	Initial value
000040_H	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	$0X000XX1_B$
000041_H	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		$0X000001_B$
000042_H	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		$000000X0_B$
000043_H	Reserved				
000044_H	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	$0X000XX1_B$
000045_H	PPG B Operation Mode Control Register	PPGCB	W,R/W		$0X000001_B$
000046_H	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		$000000X0_B$
000047_H	Reserved				
000048_H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	$0X000XX1_B$
000049_H	PPG D Operation Mode Control Register	PPGCD	W,R/W		$0X000001_B$
$00004A_H$	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		$000000X0_B$
$00004B_H$	Reserved				
$00004C_H$	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	$0X000XX1_B$
$00004D_H$	PPG F Operation Mode Control Register	PPGCF	W,R/W		$0X000001_B$
$00004E_H$	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		$000000X0_B$
$00004F_H$	Reserved				
000050_H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000_B
000051_H	Input Capture Edge 0/1	ICE01	R/W, R		$XXX0X0XX_B$
000052_H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000_B
000053_H	Input Capture Edge 2/3	ICE23	R		$XXXXXXXX_B$
000054_H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000_B
000055_H	Input Capture Edge 4/5	ICE45	R		$XXXXXXXX_B$
000056_H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000_B
000057_H	Input Capture Edge 6/7	ICE67	R/W, R		$XXX000XX_B$
000058_H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	$0000XX00_B$
000059_H	Output Compare Control Status 1	OCS1	R/W		$0XX00000_B$
$00005A_H$	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	$0000XX00_B$
$00005B_H$	Output Compare Control Status 3	OCS3	R/W		$0XX00000_B$
$00005C_H$	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	$0000XX00_B$
$00005D_H$	Output Compare Control Status 5	OCS5	R/W		$0XX00000_B$
$00005E_H$	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	$0000XX00_B$
$00005F_H$	Output Compare Control Status 7	OCS7	R/W		$0XX00000_B$

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9. CAN Controllers

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
- Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
- 29-bit ID and 8-byte data
- Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
- Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070_H	000080_H	Message Buffer Valid Register	BVALR	R/W	00000000_B 00000000_B
000071_H	000081_H				
000072_H	000082_H	Transmit Request Register	TREQR	R/W	00000000_B 00000000_B
000073_H	000083_H				
000074_H	000084_H	Transmit Cancel Register	TCANR	W	00000000_B 00000000_B
000075_H	000085_H				
000076_H	000086_H	Transmission Complete Register	TCR	R/W	00000000_B 00000000_B
000077_H	000087_H				
000078_H	000088_H	Receive Complete Register	RCR	R/W	00000000_B 00000000_B
000079_H	000089_H				
$00007A_H$	$00008A_H$	Remote Request Receiving Register	RRTRR	R/W	00000000_B 00000000_B
$00007B_H$	$00008B_H$				
$00007C_H$	$00008C_H$	Receive Overrun Register	ROVRR	R/W	00000000_B 00000000_B
$00007D_H$	$00008D_H$				
$00007E_H$	$00008E_H$	Reception Interrupt Enable Register	RIER	R/W	00000000_B 00000000_B
$00007F_H$	$00008F_H$				

List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A40_H$	$007C40_H$	ID Register 8	IDR8	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A41_H$	$007C41_H$				
$007A42_H$	$007C42_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A43_H$	$007C43_H$				
$007A44_H$	$007C44_H$	ID Register 9	IDR9	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A45_H$	$007C45_H$				
$007A46_H$	$007C46_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A47_H$	$007C47_H$				
$007A48_H$	$007C48_H$	ID Register 10	IDR10	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A49_H$	$007C49_H$				
$007A4A_H$	$007C4A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4B_H$	$007C4B_H$				
$007A4C_H$	$007C4C_H$	ID Register 11	IDR11	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4D_H$	$007C4D_H$				
$007A4E_H$	$007C4E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4F_H$	$007C4F_H$				
$007A50_H$	$007C50_H$	ID Register 12	IDR12	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A51_H$	$007C51_H$				
$007A52_H$	$007C52_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A53_H$	$007C53_H$				
$007A54_H$	$007C54_H$	ID Register 13	IDR13	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A55_H$	$007C55_H$				
$007A56_H$	$007C56_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A57_H$	$007C57_H$				
$007A58_H$	$007C58_H$	ID Register 14	IDR14	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A59_H$	$007C59_H$				
$007A5A_H$	$007C5A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5B_H$	$007C5B_H$				
$007A5C_H$	$007C5C_H$	ID Register 15	IDR15	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5D_H$	$007C5D_H$				
$007A5E_H$	$007C5E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5F_H$	$007C5F_H$				

List of Message Buffers (DLC Registers and Data Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A80_H$ to $007A87_H$	$007C80_H$ to $007C87_H$	Data Register 0 (8 bytes)	DTR0	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A88_H$ to $007A8F_H$	$007C88_H$ to $007C8F_H$	Data Register 1 (8 bytes)	DTR1	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A90_H$ to $007A97_H$	$007C90_H$ to $007C97_H$	Data Register 2 (8 bytes)	DTR2	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A98_H$ to $007A9F_H$	$007C98_H$ to $007C9F_H$	Data Register 3 (8 bytes)	DTR3	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AA0_H$ to $007AA7_H$	$007CA0_H$ to $007CA7_H$	Data Register 4 (8 bytes)	DTR4	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AA8_H$ to $007AAF_H$	$007CA8_H$ to $007CAF_H$	Data Register 5 (8 bytes)	DTR5	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AB0_H$ to $007AB7_H$	$007CB0_H$ to $007CB7_H$	Data Register 6 (8 bytes)	DTR6	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AB8_H$ to $007ABF_H$	$007CB8_H$ to $007CBF_H$	Data Register 7 (8 bytes)	DTR7	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AC0_H$ to $007AC7_H$	$007CC0_H$ to $007CC7_H$	Data Register 8 (8 bytes)	DTR8	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AC8_H$ to $007ACF_H$	$007CC8_H$ to $007CCF_H$	Data Register 9 (8 bytes)	DTR9	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AD0_H$ to $007AD7_H$	$007CD0_H$ to $007CD7_H$	Data Register 10 (8 bytes)	DTR10	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AD8_H$ to $007ADF_H$	$007CD8_H$ to $007CDF_H$	Data Register 11 (8 bytes)	DTR11	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AE0_H$ to $007AE7_H$	$007CE0_H$ to $007CE7_H$	Data Register 12 (8 bytes)	DTR12	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AE8_H$ to $007AEF_H$	$007CE8_H$ to $007CEF_H$	Data Register 13 (8 bytes)	DTR13	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI^{2}OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC$_H$	—	—
INT9 instruction	N	—	#09	FFFFD8$_H$	—	—
Exception	N	—	#10	FFFFD4$_H$	—	—
CAN 0 RX	N	—	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN 0 TX/NS	N	—	#12	FFFFCC$_H$		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4$_H$		
CAN 2 RX / I^{2}C0	N	—	#15	FFFFC0$_H$	ICR02	0000B2$_H$
CAN 2 TX/NS	N	—	#16	FFFFBC$_H$		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8$_H$	ICR03	0000B3$_H$
16-bit Reload Timer 1	Y1	1	#18	FFFFB4$_H$		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit Reload Timer 3	Y1	—	#20	FFFFAC$_H$		
PPG 0/1/4/5	N	—	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG 2/3/6/7	N	—	#22	FFFFA4$_H$		
PPG 8/9/C/D	N	—	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPG A/B/E/F	N	—	#24	FFFF9C$_H$		
Time Base Timer	N	—	#25	FFFF98$_H$	ICR07	0000B7$_H$
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94$_H$		
Watch Timer	N	—	#27	FFFF90$_H$	ICR08	0000B8$_H$
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C$_H$		
A/D Converter	Y1	5	#29	FFFF88$_H$	ICR09	0000B9$_H$
Free-run Timer 0 / Free-run Timer 1	N	—	#30	FFFF84$_H$		
Input Capture 4/5 / I^{2}C1	Y1	6	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C$_H$		
Input Capture 0 to 3	Y1	8	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output Compare 2/3/6/7	Y1	9	#34	FFFF74$_H$		
UART 0 RX	Y2	10	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART 0 TX	Y1	11	#36	FFFF6C$_H$		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64$_H$		

(Continued)

11.3 DC Characteristics

($T_A = -40°C$ to $+105°C$, $V_{CC} = 5.0\ V \pm 10\%$, $f_{CP} \leq 24$ MHz, $V_{SS} = AV_{SS} = 0\ V$)

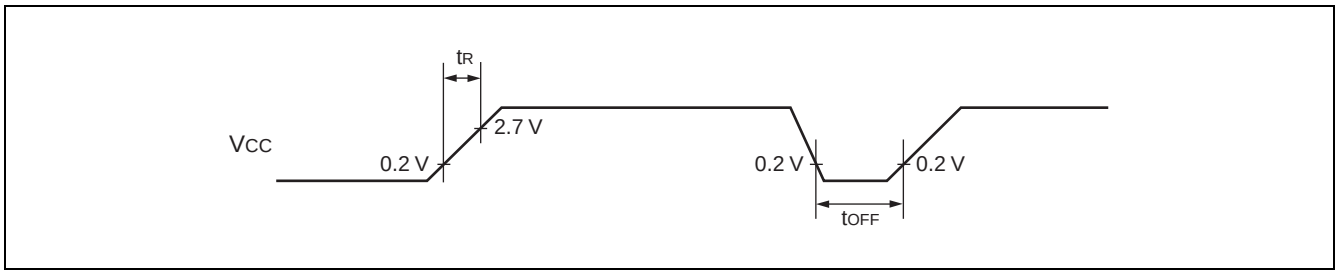
Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At V_{CC} = 5 V ± 10%)	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	V_{CC} + 0.3	V	Port inputs if TTL input levels are selected
	V_{IHS}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHI}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	V_{CC} − 0.3	—	V_{CC} + 0.3	V	MD input pin
Input L voltage (At V_{CC} = 5 V ± 10%)	V_{ILS}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{ILA}	—	—	V_{SS} − 0.3	—	0.5 V_{CC}	V	Port inputs if Automotive input levels are selected
	V_{ILT}	—	—	V_{SS} − 0.3	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILI}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	V_{SS} − 0.3	—	V_{SS} + 0.3	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	V_{CC} − 0.5	—	—	V	
Output H voltage	V_{OHI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OH} = −3.0 mA	V_{CC} − 0.5	—	—	V	
Output L voltage	V_{OL}	Normal outputs	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Output L voltage	V_{OLI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OL} = 3.0 mA	—	—	0.4	V	

(Continued)

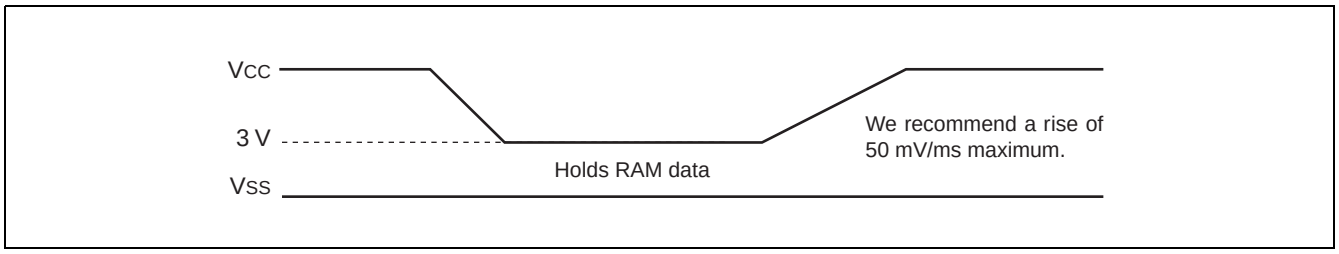
11.4.3 Power On Reset

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Waiting time until power-on



Note: : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



11.4.4 Clock Output Timing

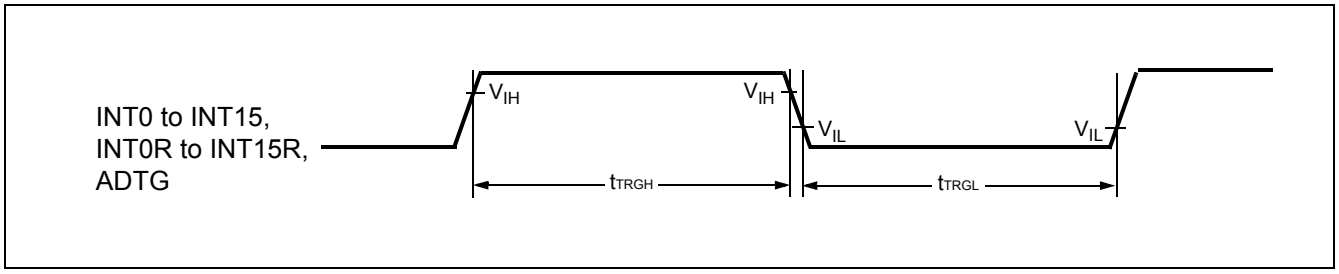
(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	f_{CP} = 16 MHz
				41.67	—	ns	f_{CP} = 24 MHz
CLK ↑ → CLK ↓	t_{CHCL}	CLK	—	20	—	ns	f_{CP} = 16 MHz
				13	—	ns	f_{CP} = 24 MHz

11.4.10 Trigger Input Timing

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT15, INT0R to INT15R, ADTG	—	5 t_{CP}	—	ns



11.5 A/D Converter

(T_A = −40°C to +105°C, 3.0 V≤ AVRH − AVRL, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP}≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	AVRL − 1.5 × LSB	AVRL + 0.5 × LSB	AVRL + 2.5 × LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	AVRH − 3.5 × LSB	AVRH − 1.5 × LSB	AVRH + 0.5 × LSB	V	
Compare time	—	—	1.0	—	16500	µs	4.5 V≤ AV_{CC}≤ 5.5 V
			2.0				4.0 V≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	∞	µs	4.5 V≤ AV_{CC}≤ 5.5 V
			1.2				4.0 V≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN23	−0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 2.7	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

*: If the A/D convertor is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .
Note: : The accuracy gets worse as |AVRH − AVRL| becomes smaller.

11.8 Flash Memory Program/Erase Characteristics

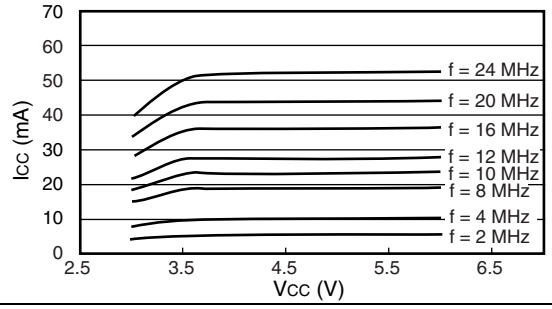
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25°C$ $V_{CC} = 5.0$ V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	µs	Except for the over head time of the system
Program/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average $T_A = +85°C$	20	—	—	year	*

* : This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85°C) .

■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES

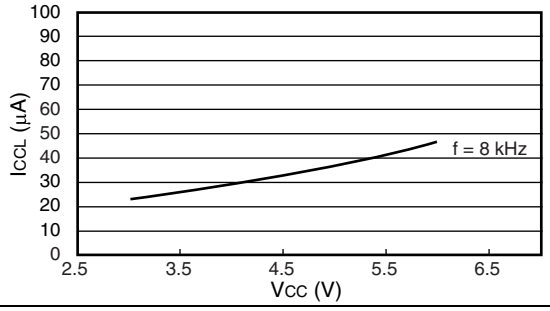
$I_{CC} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



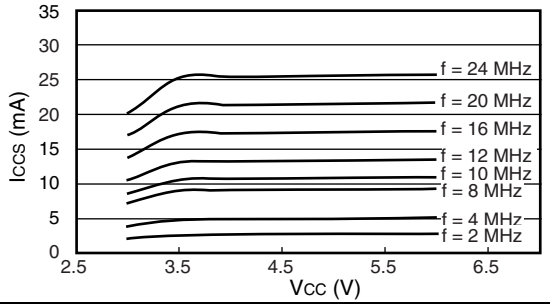
$I_{CCL} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



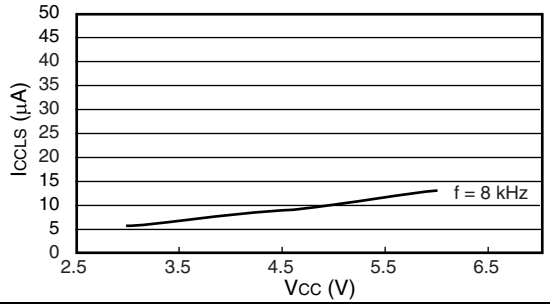
$I_{CCS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



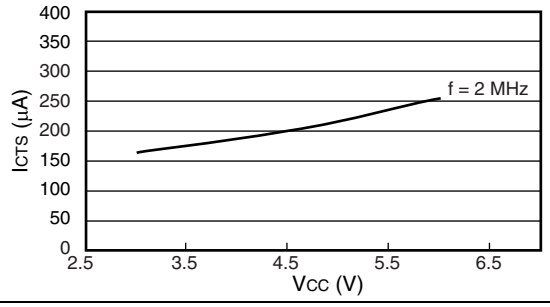
$I_{CCLS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CCT} - V_{CC}$

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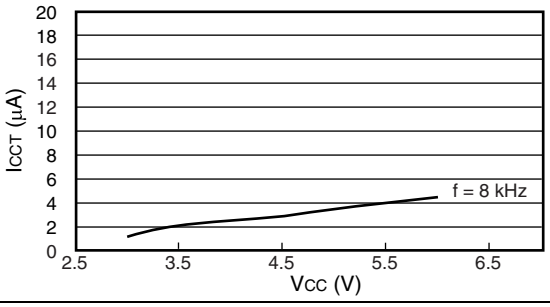
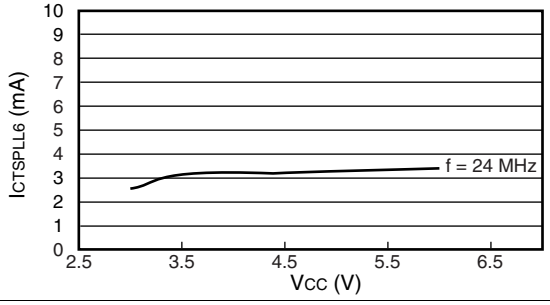


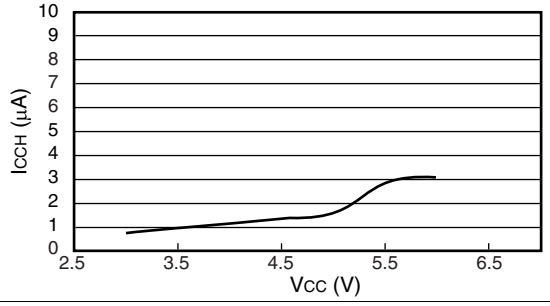
$I_{CTSPLL6} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



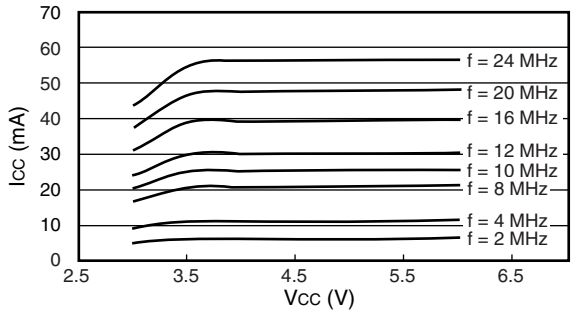
$I_{CCH} - V_{CC}$

$T_A = +25°C$, stopped

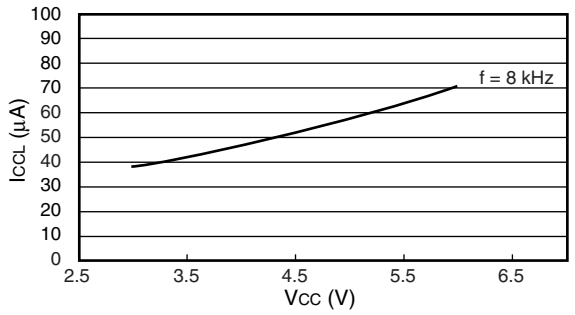


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

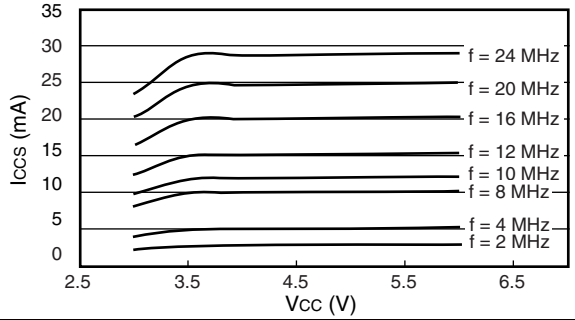
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



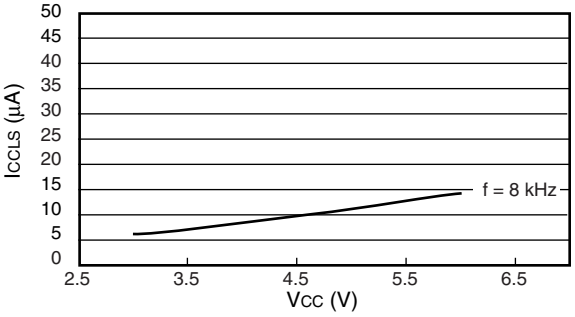
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



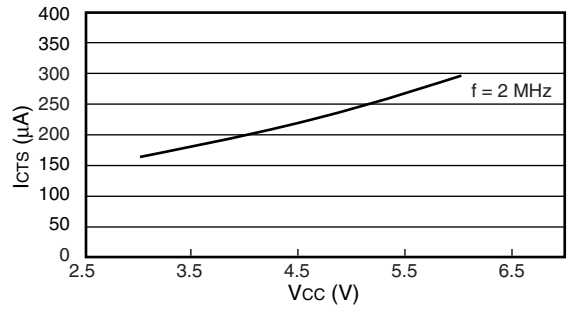
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



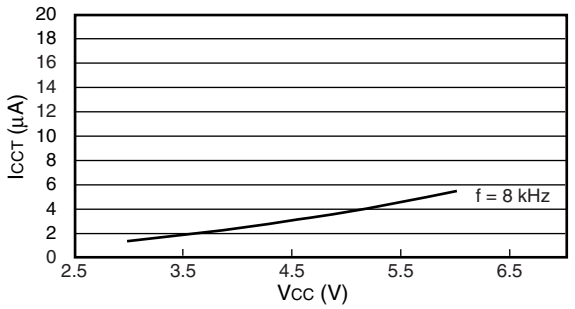
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



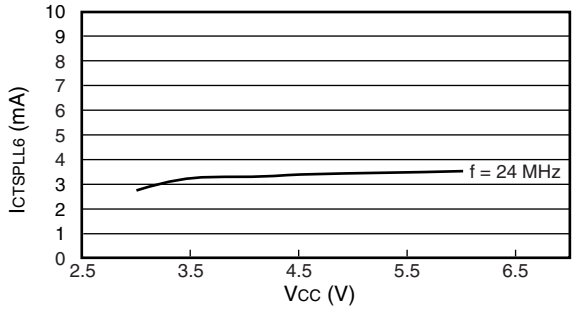
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



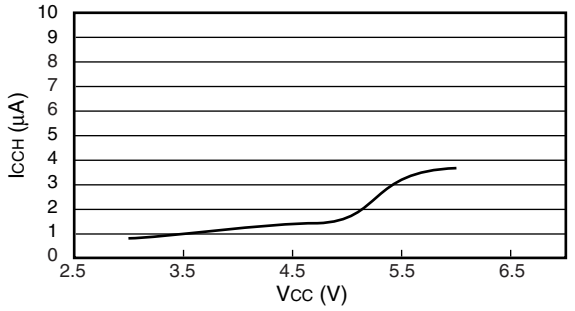
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped



(Continued)

Part number	Package	Remarks
MB90346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90346ESPF		
MB90346CEPF		
MB90346CESPF		
MB90346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90346ESPMC		
MB90346CEPMC		
MB90346CESPMC		
MB90347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90347ESPF		
MB90347CEPF		
MB90347CESPF		
MB90347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90347ESPMC		
MB90347CEPMC		
MB90347CESPMC		
MB90348EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90348ESPF		
MB90348CEPF		
MB90348CESPF		
MB90348EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90348ESPMC		
MB90348CEPMC		
MB90348CESPMC		
MB90349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90349ESPF		
MB90349CEPF		
MB90349CESPF		
MB90349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90349ESPMC		
MB90349CEPMC		
MB90349CESPMC		
MB90V340E-101CR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation
MB90V340E-102CR		

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