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What is "Embedded - Microcontrollers"?

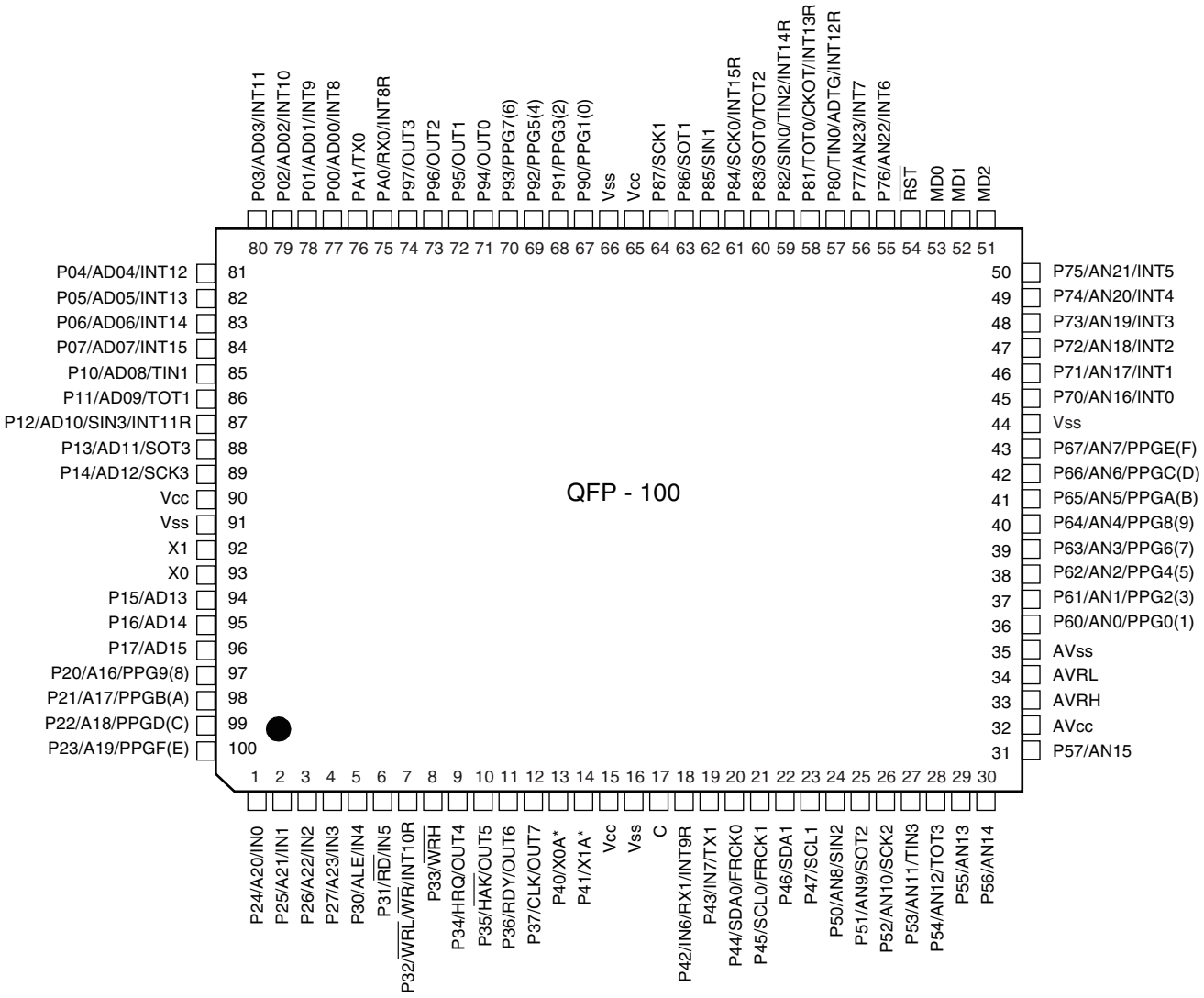
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 24x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90349cepf-g-409e1

■ MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)

(TOP VIEW)



(FPT-100P-M06)

* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

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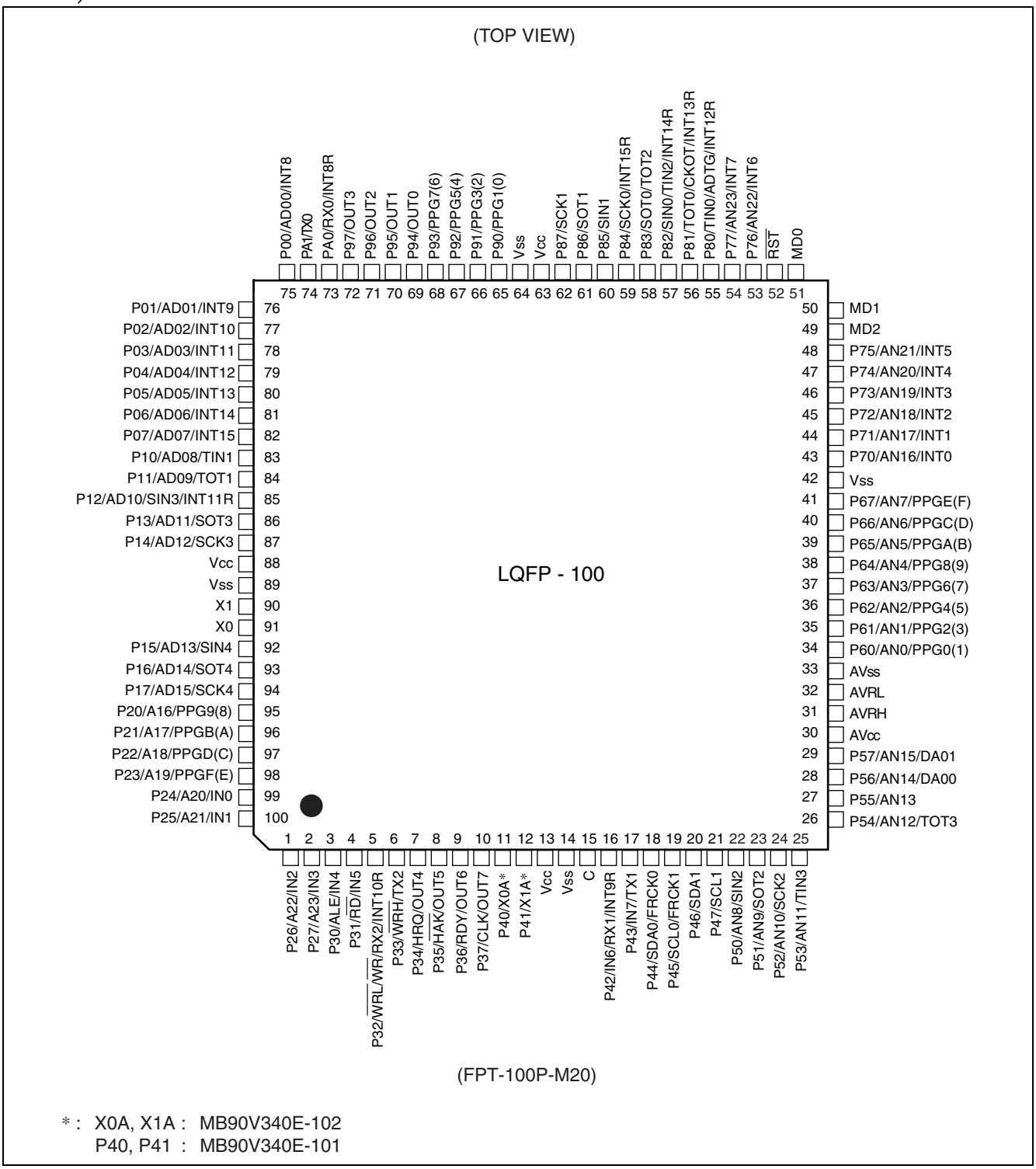

This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

3. Pin Description

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
1 to 4	99 to 2	P24 to P27	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Trigger input pins for input captures.
5	3	P30	G	General purpose I/O pin.The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Trigger input pin for input capture.
6	4	P31	G	General purpose I/O pin.The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		$\overline{RD}$		External read strobe output pin. This function is enabled when the external bus is enabled.
		IN5		Trigger input pin for input capture.
7	5	P32	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the WR/WRL pin output is disabled.
		$\overline{WR}$ / $\overline{WRL}$		Write strobe output pin for the external data bus. This function is enabled when both the external bus and the WR/WRL pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
		INT10R		External interrupt request input pin.
8	6	P33	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or when the WRH pin output is disabled.
		$\overline{WRH}$		Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter
35	33	AV_{SS}	K	Analog GND pin for the A/D Converter
36 to 43	34 to 41	P60 to P67	I	General purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
44	42	V_{SS}	—	GND pin
45 to 50	43 to 48	P70 to P75	I	General purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT0 to INT5		External interrupt request input pins
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	$\overline{RST}$	E	Reset input pin
55, 56	53, 54	P76, P77	I	General purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT6, INT7		External interrupt request input pins
57	55	P80	F	General purpose I/O pin.
		TIN0		Event input pin for the reload timer
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin
58	56	P81	F	General purpose I/O pin.
		TOT0		Output pin for the reload timer
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin
59	57	P82	M	General purpose I/O pin.
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer
		INT14R		External interrupt request input pin
60	58	P83	F	General purpose I/O pin.
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
66	64	V_{SS}	—	GND pin
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pins
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pins
		OUT0 to OUT3		Waveform output pins for output compares. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin
76	74	PA1	F	General purpose I/O pin.
		TX0		TX Output pin for CAN0
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer

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Address	Register	Abbreviation	Access	Resource name	Initial value
$0000A5_H$	Automatic Ready Function Select Register	ARSR	W	External Memory Access	$0011XX00_B$
$0000A6_H$	External Address Output Control Register	HACR	W		00000000_B
$0000A7_H$	Bus Control Signal Selection Register	ECSR	W		$0000000X_B$
$0000A8_H$	Watchdog Control Register	WDTC	R,W	Watchdog Timer	$XXXXX111_B$
$0000A9_H$	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	$1XX00100_B$
$0000AA_H$	Watch Timer Control Register	WTC	R,R/W	Watch Timer	$1X001000_B$
$0000AB_H$	Reserved				
$0000AC_H$	DMA Enable L Register	DERL	R/W	DMA	00000000_B
$0000AD_H$	DMA Enable H Register	DERH	R/W		00000000_B
$0000AE_H$	Flash Control Status Register (Flash memory devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	$000X0000_B$
$0000AF_H$	Reserved				
$0000B0_H$	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111_B
$0000B1_H$	Interrupt Control Register 01	ICR01	W,R/W		00000111_B
$0000B2_H$	Interrupt Control Register 02	ICR02	W,R/W		00000111_B
$0000B3_H$	Interrupt Control Register 03	ICR03	W,R/W		00000111_B
$0000B4_H$	Interrupt Control Register 04	ICR04	W,R/W		00000111_B
$0000B5_H$	Interrupt Control Register 05	ICR05	W,R/W		00000111_B
$0000B6_H$	Interrupt Control Register 06	ICR06	W,R/W		00000111_B
$0000B7_H$	Interrupt Control Register 07	ICR07	W,R/W		00000111_B
$0000B8_H$	Interrupt Control Register 08	ICR08	W,R/W		00000111_B
$0000B9_H$	Interrupt Control Register 09	ICR09	W,R/W		00000111_B
$0000BA_H$	Interrupt Control Register 10	ICR10	W,R/W		00000111_B
$0000BB_H$	Interrupt Control Register 11	ICR11	W,R/W		00000111_B
$0000BC_H$	Interrupt Control Register 12	ICR12	W,R/W		00000111_B
$0000BD_H$	Interrupt Control Register 13	ICR13	W,R/W		00000111_B
$0000BE_H$	Interrupt Control Register 14	ICR14	W,R/W		00000111_B
$0000BF_H$	Interrupt Control Register 15	ICR15	W,R/W		00000111_B
$0000C0_H$	D/A Converter Data 0	DAT0	R/W	D/A Converter	$XXXXXXXX_B$
$0000C1_H$	D/A Converter Data 1	DAT1	R/W		$XXXXXXXX_B$
$0000C2_H$	D/A Control 0	DACR0	R/W		$XXXXXXX0_B$
$0000C3_H$	D/A Control 1	DACR1	R/W		$XXXXXXX0_B$

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Address	Register	Abbreviation	Access	Resource name	Initial value
007948_H	Timer 0/Reload 0	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	$XXXXXXXX_B$
007949_H			R/W		$XXXXXXXX_B$
$00794A_H$	Timer 1/Reload 1	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	$XXXXXXXX_B$
$00794B_H$			R/W		$XXXXXXXX_B$
$00794C_H$	Timer 2/Reload 2	TMR2/TMRLR2	R/W	16-bit Reload Timer 2	$XXXXXXXX_B$
$00794D_H$			R/W		$XXXXXXXX_B$
$00794E_H$	Timer 3/Reload 3	TMR3/TMRLR3	R/W	16-bit Reload Timer 3	$XXXXXXXX_B$
$00794F_H$			R/W		$XXXXXXXX_B$
007950_H	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000_B
007951_H	Serial Control Register 3	SCR3	W,R/W		00000000_B
007952_H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000_B
007953_H	Serial Status Register 3	SSR3	R,R/W		00001000_B
007954_H	Extended Communication Control Register 3	ECCR3	R,W, R/W		$000000XX_B$
007955_H	Extended Status Control Register	ESCR3	R/W		00000100_B
007956_H	Baud Rate Generator Register 30	BGR30	R/W		00000000_B
007957_H	Baud Rate Generator Register 31	BGR31	R/W		00000000_B
007958_H	Serial Mode Register 4	SMR4	W,R/W	UART4	00000000_B
007959_H	Serial Control Register 4	SCR4	W,R/W		00000000_B
$00795A_H$	Reception/Transmission Data Register 4	RDR4/TDR4	R/W		00000000_B
$00795B_H$	Serial Status Register 4	SSR4	R,R/W		00001000_B
$00795C_H$	Extended Communication Control Register 4	ECCR4	R,W, R/W		$000000XX_B$
$00795D_H$	Extended Status Control Register	ESCR4	R/W		00000100_B
$00795E_H$	Baud Rate Generator Register 40	BGR40	R/W		00000000_B
$00795F_H$	Baud Rate Generator Register 41	BGR41	R/W		00000000_B
007960_H to $00796B_H$	Reserved				
$00796C_H$	Clock Output Enable Register	CLKR	R/W	Clock Monitor	$XXXX0000_B$
$00796D_H$	Reserved				
$00796E_H$	CAN Direct Mode Register	CDMR	R/W	CAN Clock sync	$XXXXXXX0_B$
$00796F_H$	CAN Switch Register	CANSWR	R/W	CAN 0/1	$XXXXXX00_B$

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Address	Register	Abbreviation	Access	Resource name	Initial value
007970_H	I^2C Bus Status Register 0	IBSR0	R	I^2C Interface 0	00000000_B
007971_H	I^2C Bus Control Register 0	IBCR0	W,R/W		00000000_B
007972_H	I^2C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000_B
007973_H		ITBAH0	R/W		00000000_B
007974_H	I^2C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111_B
007975_H		ITMKH0	R/W		00111111_B
007976_H	I^2C 7-bit Slave Address Register 0	ISBA0	R/W		00000000_B
007977_H	I^2C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111_B
007978_H	I^2C Data Register 0	IDAR0	R/W		00000000_B
007979_H, $00797A_H$	Reserved				
$00797B_H$	I^2C Clock Control Register 0	ICCR0	R/W	I^2C Interface 0	00011111_B
$00797C_H$ to $00797F_H$	Reserved				
007980_H	I^2C Bus Status Register 1	IBSR1	R	I^2C Interface 1	00000000_B
007981_H	I^2C Bus Control Register 1	IBCR1	W,R/W		00000000_B
007982_H	I^2C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000_B
007983_H		ITBAH1	R/W		00000000_B
007984_H	I^2C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111_B
007985_H		ITMKH1	R/W		00111111_B
007986_H	I^2C 7-bit Slave Address Register 1	ISBA1	R/W		00000000_B
007987_H	I^2C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111_B
007988_H	I^2C Data Register 1	IDAR1	R/W		00000000_B
007989_H, $00798A_H$	Reserved				
$00798B_H$	I^2C Clock Control Register 1	ICCR1	R/W	I^2C Interface 1	00011111_B
$00798C_H$ to $0079C1_H$	Reserved				
$0079C2_H$	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	$0001X000_B$
$0079C3_H$ to $0079DF_H$	Reserved				

(Continued)

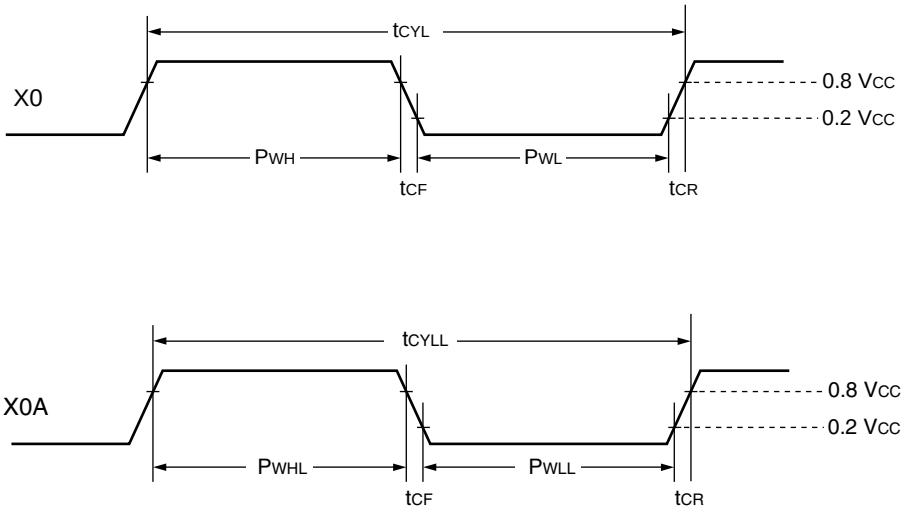
List of Control Registers (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007B00_H$	$007D00_H$	Control Status Register	CSR	R/W, W R/W, R	$0XXXX0X1_B$ $00XXX000_B$
$007B01_H$	$007D01_H$				
$007B02_H$	$007D02_H$	Last Event Indicator Register	LEIR	R/W	$000X0000_B$ $XXXXXXXX_B$
$007B03_H$	$007D03_H$				
$007B04_H$	$007D04_H$	Receive And Transmit Error Counter	RTEC	R	00000000_B 00000000_B
$007B05_H$	$007D05_H$				
$007B06_H$	$007D06_H$	Bit Timing Register	BTR	R/W	11111111_B $X1111111_B$
$007B07_H$	$007D07_H$				
$007B08_H$	$007D08_H$	IDE Register	IDER	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B09_H$	$007D09_H$				
$007B0A_H$	$007D0A_H$	Transmit RTR Register	TRTRR	R/W	00000000_B 00000000_B
$007B0B_H$	$007D0B_H$				
$007B0C_H$	$007D0C_H$	Remote Frame Receive Waiting Register	RFWTR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B0D_H$	$007D0D_H$				
$007B0E_H$	$007D0E_H$	Transmit Interrupt Enable Register	TIER	R/W	00000000_B 00000000_B
$007B0F_H$	$007D0F_H$				
$007B10_H$	$007D10_H$	Acceptance Mask Select Register	AMSR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B11_H$	$007D11_H$				
$007B12_H$	$007D12_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B13_H$	$007D13_H$				
$007B14_H$	$007D14_H$	Acceptance Mask Register 0	AMR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B15_H$	$007D15_H$				
$007B16_H$	$007D16_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B17_H$	$007D17_H$				
$007B18_H$	$007D18_H$	Acceptance Mask Register 1	AMR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B19_H$	$007D19_H$				
$007B1A_H$	$007D1A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B1B_H$	$007D1B_H$				

List of Message Buffers (ID Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A00_H$ to $007A1F_H$	$007C00_H$ to $007C1F_H$	General-Purpose RAM	——	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A20_H$	$007C20_H$	ID Register 0	IDR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A21_H$	$007C21_H$				
$007A22_H$	$007C22_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A23_H$	$007C23_H$				
$007A24_H$	$007C24_H$	ID Register 1	IDR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A25_H$	$007C25_H$				
$007A26_H$	$007C26_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A27_H$	$007C27_H$				
$007A28_H$	$007C28_H$	ID Register 2	IDR2	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A29_H$	$007C29_H$				
$007A2A_H$	$007C2A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A2B_H$	$007C2B_H$				
$007A2C_H$	$007C2C_H$	ID Register 3	IDR3	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A2D_H$	$007C2D_H$				
$007A2E_H$	$007C2E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A2F_H$	$007C2F_H$				
$007A30_H$	$007C30_H$	ID Register 4	IDR4	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A31_H$	$007C31_H$				
$007A32_H$	$007C32_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A33_H$	$007C33_H$				
$007A34_H$	$007C34_H$	ID Register 5	IDR5	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A35_H$	$007C35_H$				
$007A36_H$	$007C36_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A37_H$	$007C37_H$				
$007A38_H$	$007C38_H$	ID Register 6	IDR6	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A39_H$	$007C39_H$				
$007A3A_H$	$007C3A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A3B_H$	$007C3B_H$				
$007A3C_H$	$007C3C_H$	ID Register 7	IDR7	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A3D_H$	$007C3D_H$				
$007A3E_H$	$007C3E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A3F_H$	$007C3F_H$				

Clock Timing



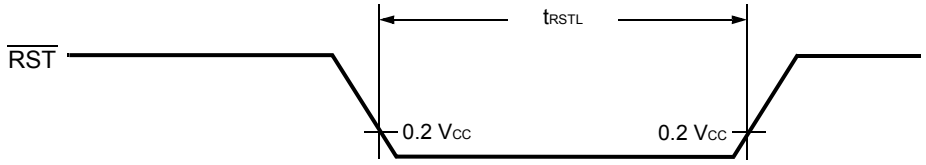
11.4.2 Reset Standby Input

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0.0 V)

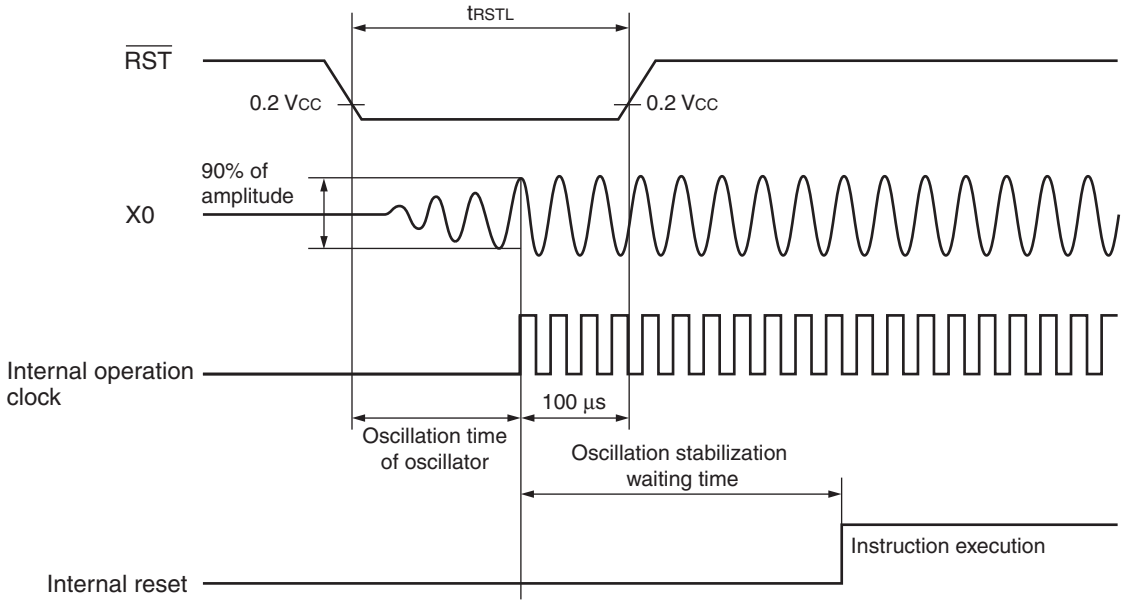
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 µs	—	µs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	µs	In Time Timer mode

* : The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

- **Under normal operation:**



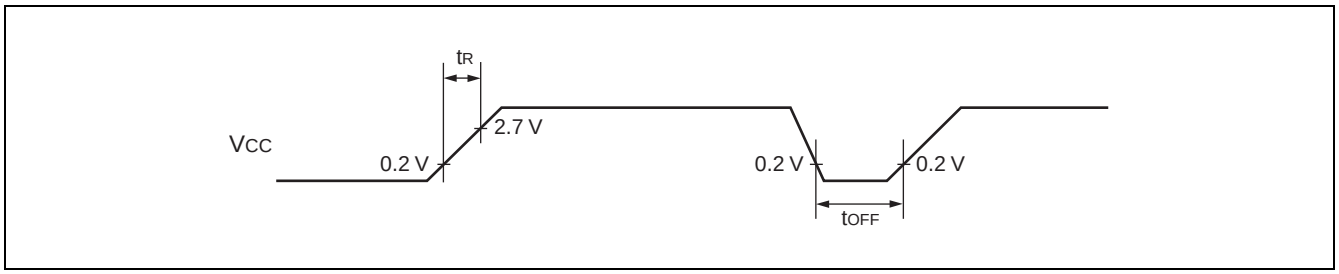
- **In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:**



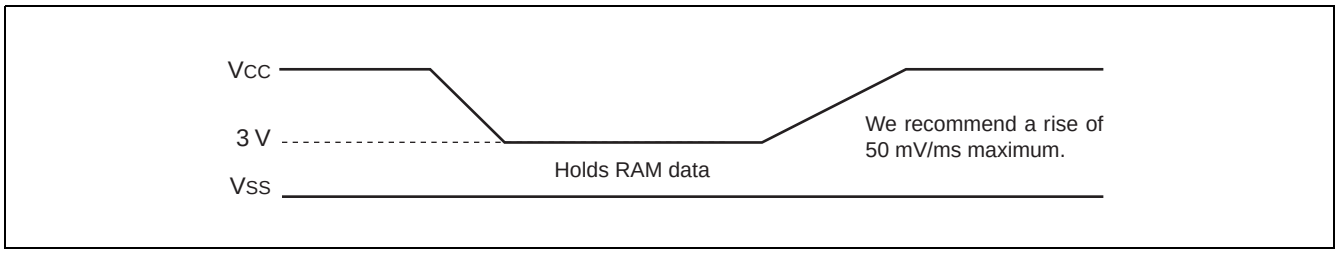
11.4.3 Power On Reset

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Waiting time until power-on



Note: : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.

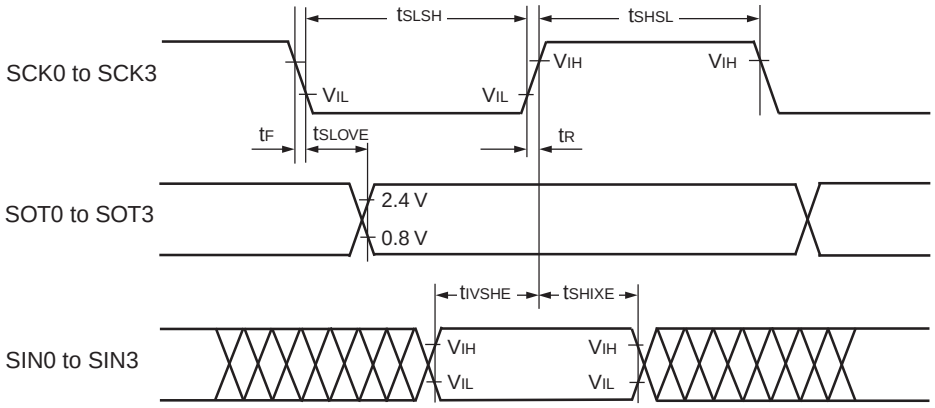


11.4.4 Clock Output Timing

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	f_{CP} = 16 MHz
				41.67	—	ns	f_{CP} = 24 MHz
CLK ↑ → CLK ↓	t_{CHCL}	CLK	—	20	—	ns	f_{CP} = 16 MHz
				13	—	ns	f_{CP} = 24 MHz

- External Shift Clock Mode



■ **Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0**

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

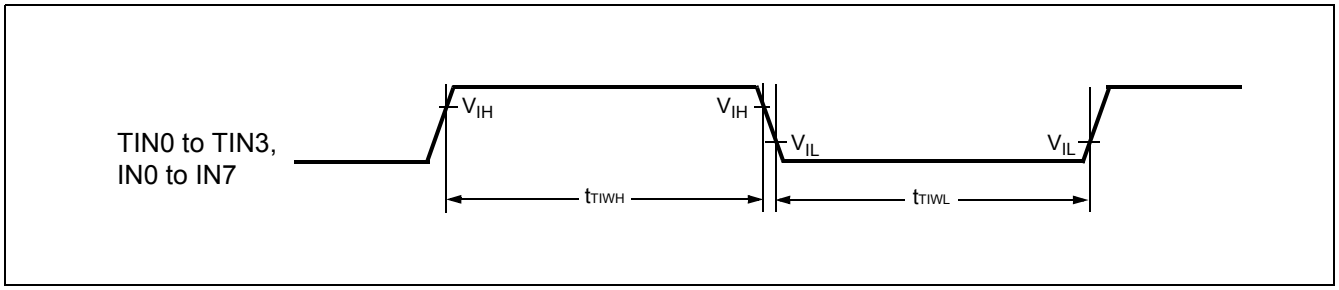
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		−50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK3		t_{CP} + 10	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXE}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

Note:
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

11.4.11 Timer Related Resource Input Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

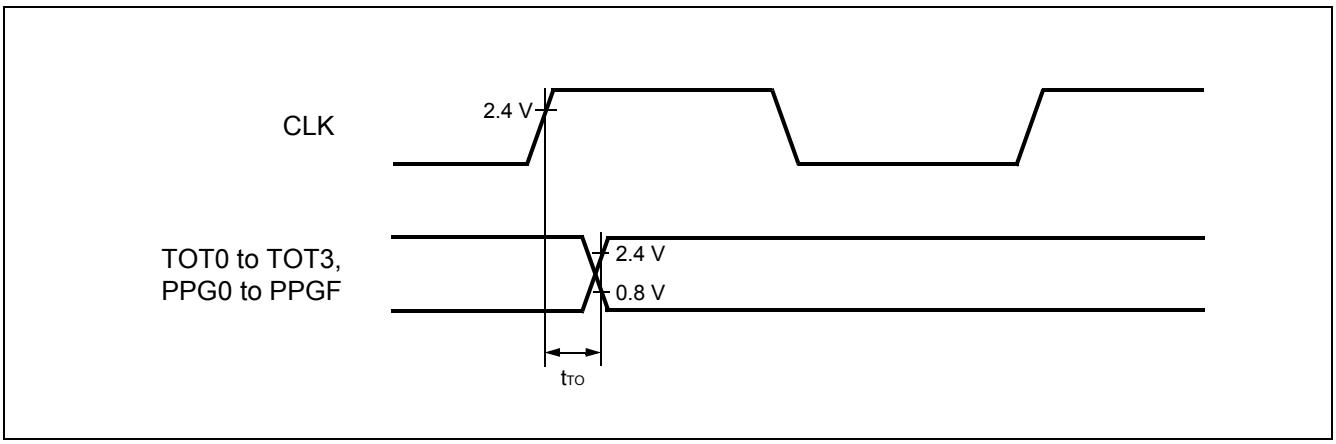
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN3, IN0 to IN7	—	4 t_{CP}	—	ns



11.4.12 Timer Related Resource Output Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns



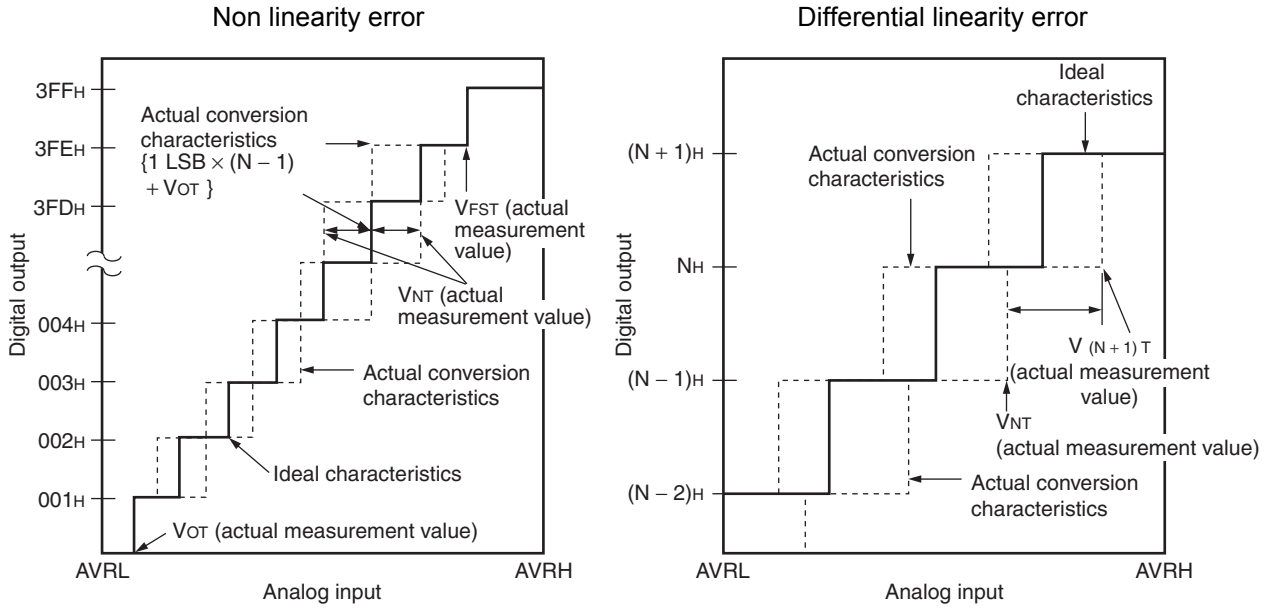
11.5 A/D Converter

(T_A = −40°C to +105°C, 3.0 V≤ AVRH − AVRL, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP}≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	AVRL − 1.5 × LSB	AVRL + 0.5 × LSB	AVRL + 2.5 × LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	AVRH − 3.5 × LSB	AVRH − 1.5 × LSB	AVRH + 0.5 × LSB	V	
Compare time	—	—	1.0	—	16500	µs	4.5 V≤ AV_{CC}≤ 5.5 V
			2.0				4.0 V≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	∞	µs	4.5 V≤ AV_{CC}≤ 5.5 V
			1.2				4.0 V≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN23	−0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 2.7	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

*: If the A/D convertor is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .
Note: : The accuracy gets worse as |AVRH − AVRL| becomes smaller.

(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : Value of the digital output from the A/D converter
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

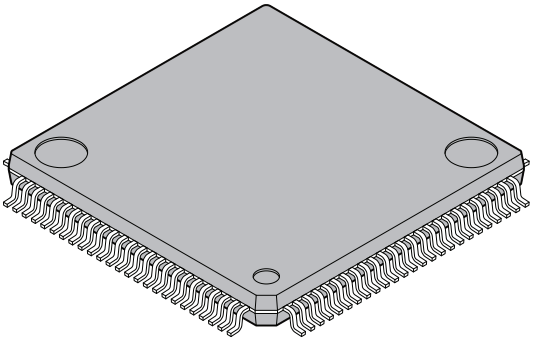
11.7 Notes on A/D Converter Section

Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower (4.0 V≤ AV_{CC}≤ 5.5 V, sampling period = 0.5 µs)

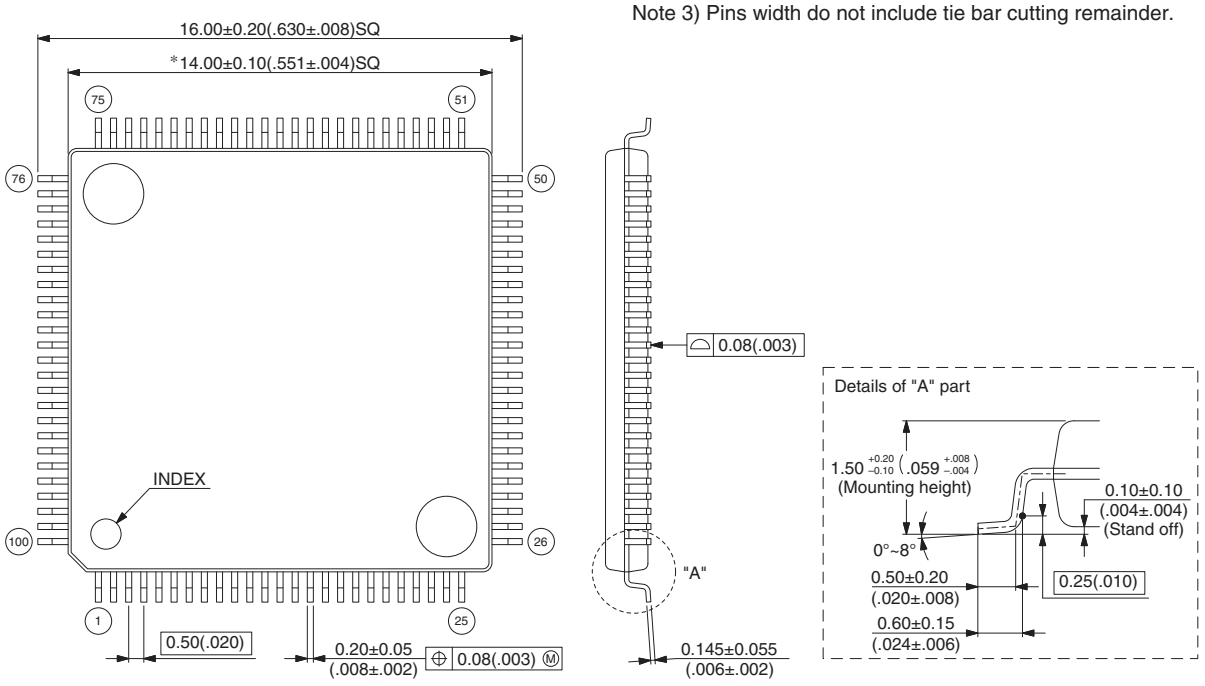
If an external capacitor is used, in consideration of the capacitive voltage dividing effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor be several thousand times greater than the capacitance of the internal capacitor.

14. Package Dimensions

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50

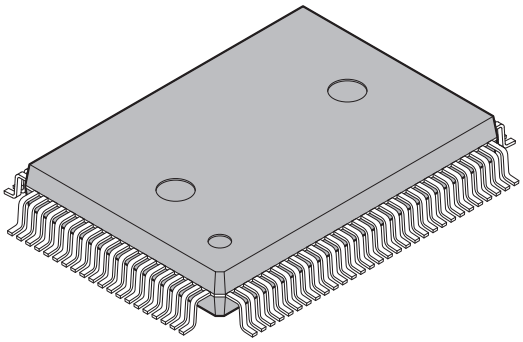
100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



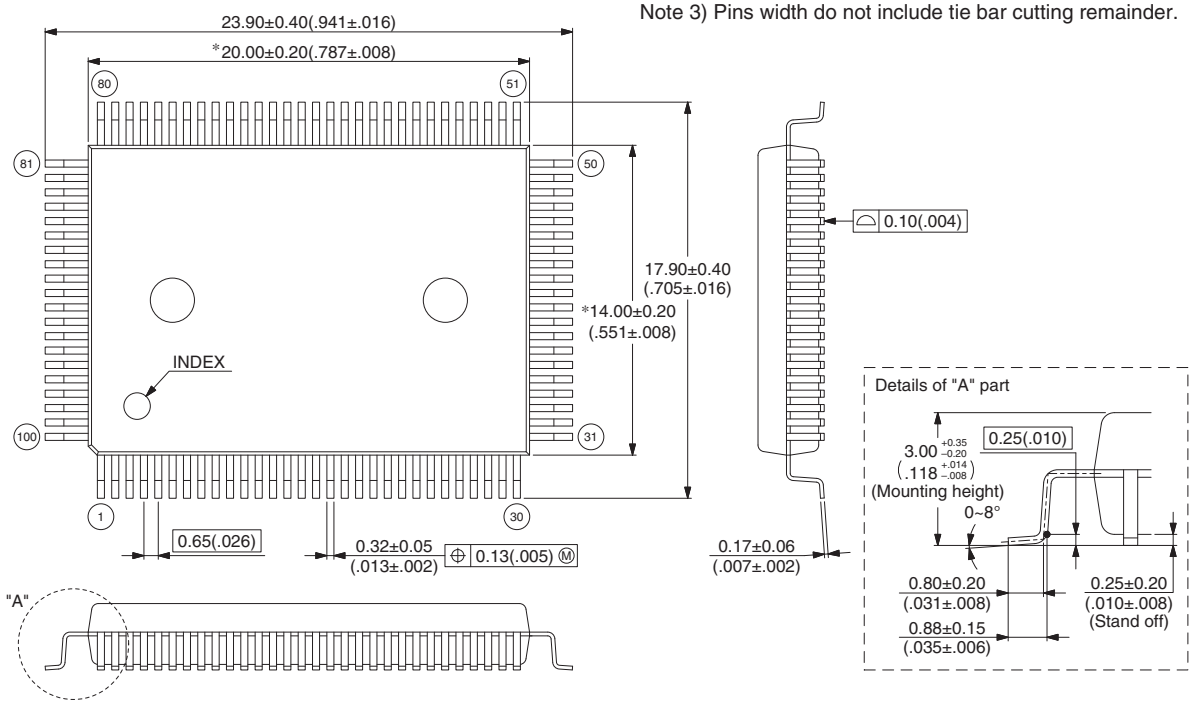
Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M06)		

100-pin plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

15. Major Changes

Spansiion Publication Number: DS07-13747-4E

Page	Section	Change Results
___	___	Deleted the part numbers; MB90F343E(S), MB90F343CE(S)
51	Electrical Characteristics Absolute Maximum Ratings	Added “*6” in remark for “L" level maximum output current and “H” level maximum output current. Added “*7” in remark for “L" level average output current and “H” level average output current. Added “*8” in remark for “L"level average overall output current and “H” level average overall output current.
52		Added as follows. “*6:The maximum output current is defined as the peak value of the current of any one of the corresponding pins.” “*7:The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.” “*8:The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.”

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90340E Series F2MC-16LX 16-bit Microcontroller Datasheet Document Number: 002-04498				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	08/23/2010	Migrated to Cypress and assigned document number 002-04498. No change to document contents or format.
*A	5221535	AKIH	05/04/2016	Updated to Cypress template