Infineon Technologies - MB90349ESPMC-GS-619E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90349espmc-gs-619e1

Part Number / Parameter	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
A/D Converter	24 input channels	Devices with a C suffix in the part number : 24 channels Devices without a C suffix in the part number : 16 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs include sample time (per one channel)		
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function		
16-bit Free-run Timer (2 channels)	Generates an interrupt signal on overflow Supports Timer Clear when the output compare finds a match Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock freq.) Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3 Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7		
16-bit Output Compare (8 channels)	Generates an interrupt signal when one of the 16-bit free-run timer matches the output compare register A pair of compare registers can be used to generate an output signal.		
16-bit Input Capture (8 channels)	Captures the value of the 16-bit free-run timer and generates an interrupt when triggered by a pin input (rising edge, falling edge, or both rising and falling edges).		
8/16-bit Programmable Pulse Generator	8 channels (16-bit) /16 channels (8-bit) Sixteen 8-bit reload counters Sixteen 8-bit reload registers for L pulse width Sixteen 8-bit reload registers for H pulse width		
	Supports 8-bit and 16-bit operation modes A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operating clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)		
CAN Interface	3 channels	2 channels : MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S) 1 channel : MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	2 channels : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S) 1 channel : MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission in response to Remote Frames Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		

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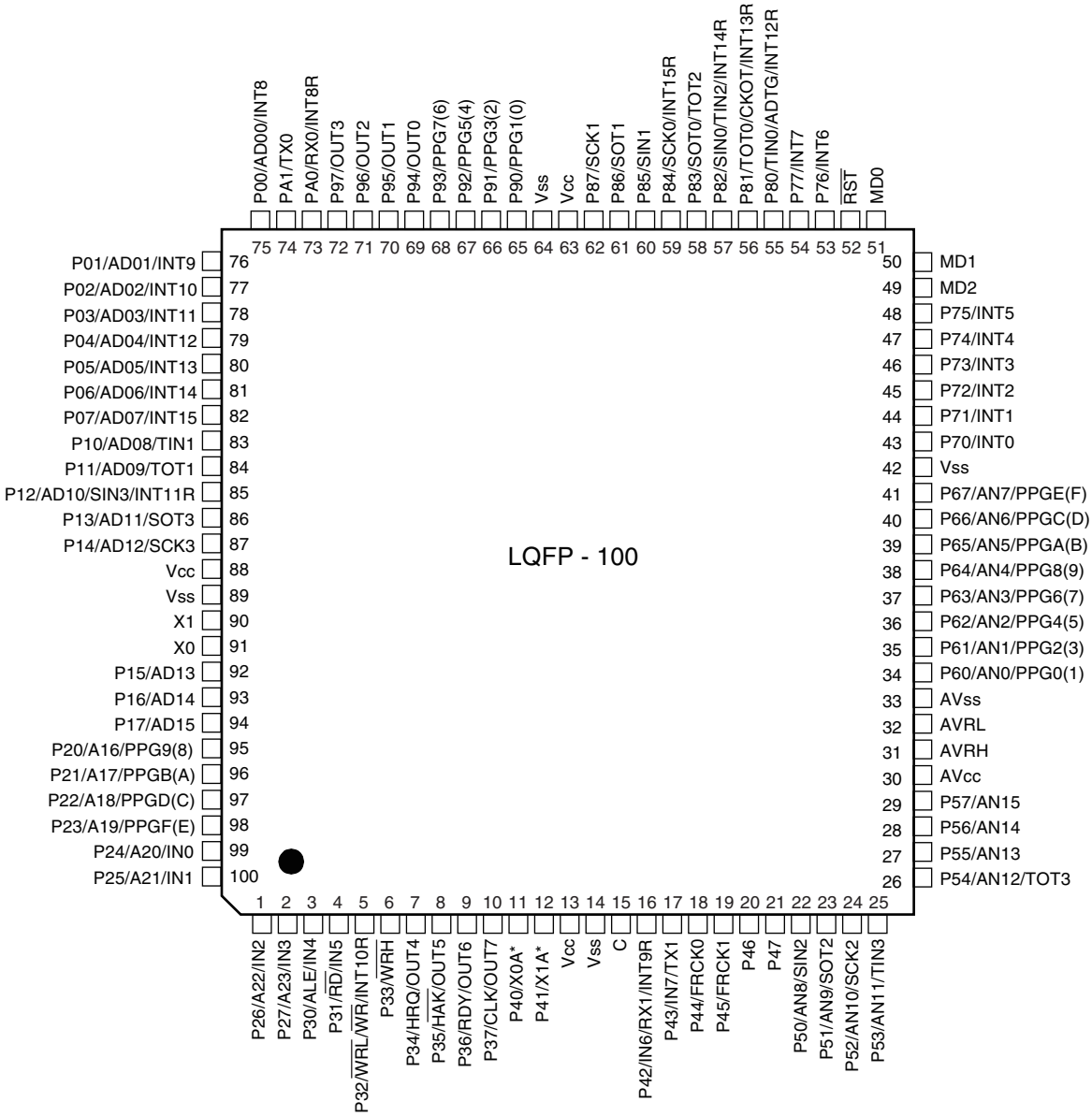
(TOP VIEW)



(FPT-100P-M20)

* : X0A, X1A : devices without an S suffix in the part number
P40, P4 : devices with an S suffix in the part number

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101)
		X0A, X1A	B	Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102)
15	13	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
16	14	V_{SS}	—	GND pin
17	15	C	K	This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 µF.
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture.
		RX1		RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only)
		INT9R		External interrupt request input pin

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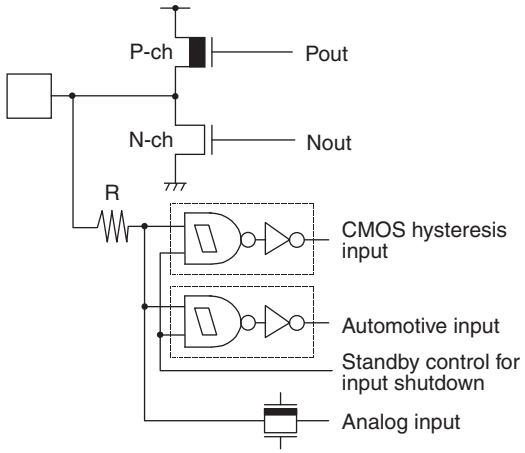
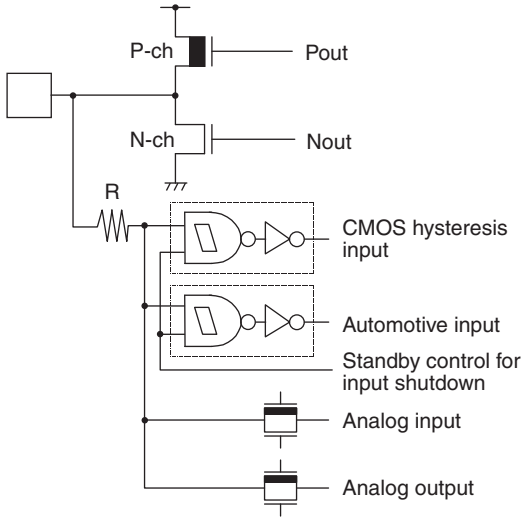
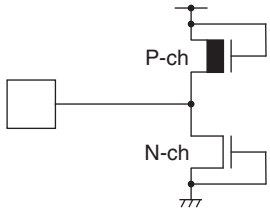
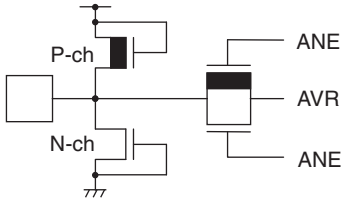
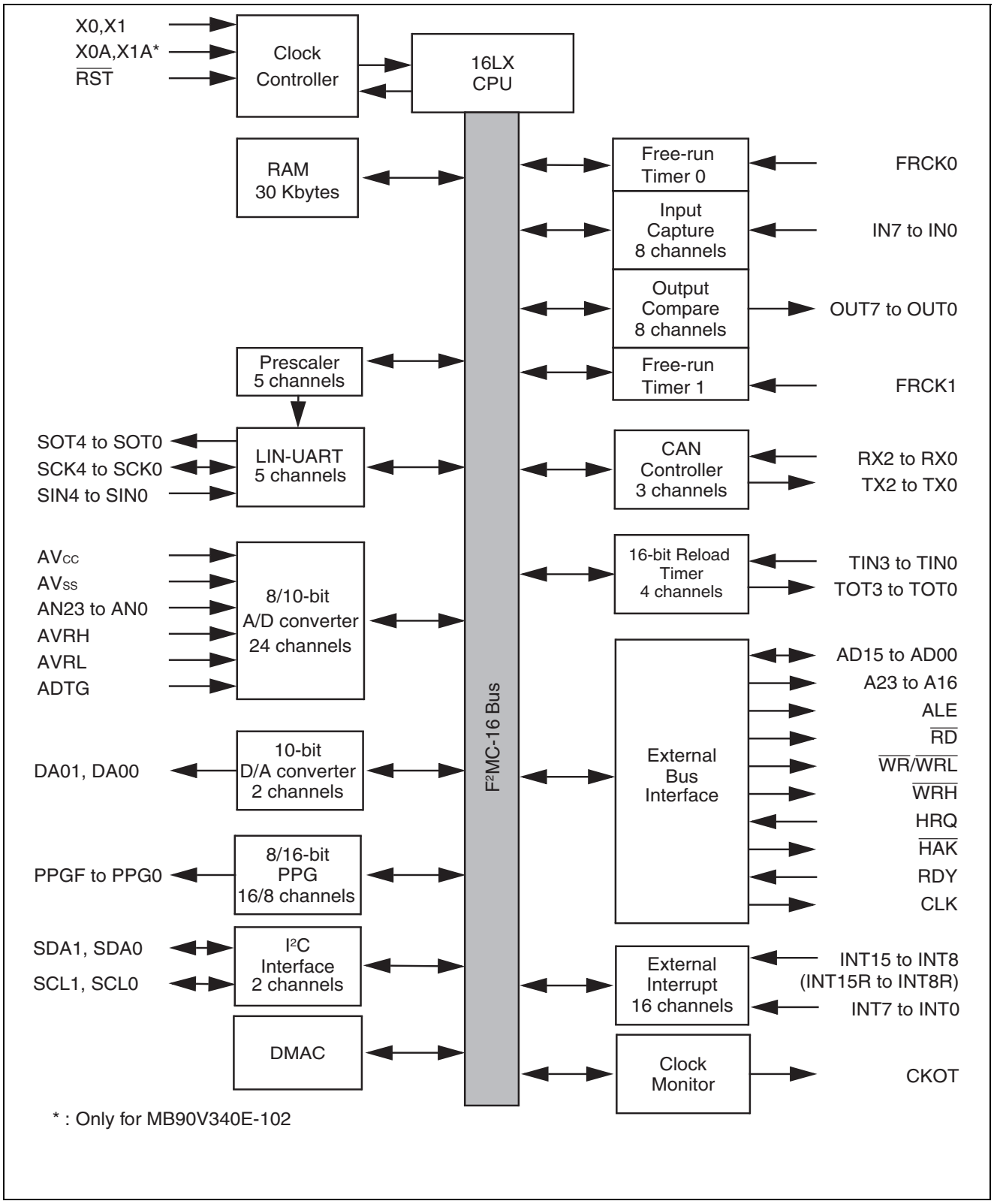
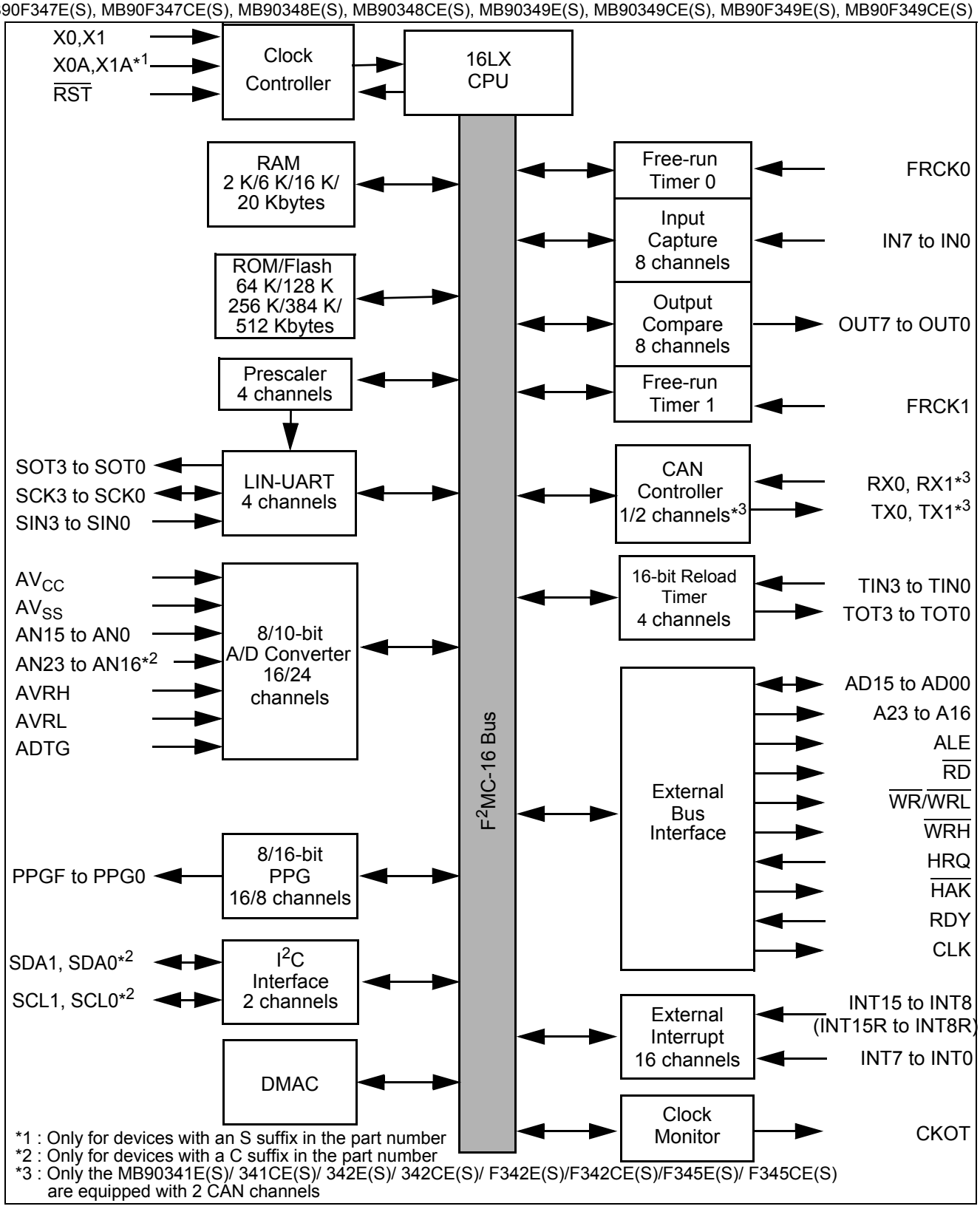
Type	Circuit	Remarks
I		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
J		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ D/A analog output ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input
K		Power supply input protection circuit
L		■ A/D converter reference voltage power supply input pin, with the protection circuit ■ Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH

6. Block Diagrams

- MB90V340E-101/102



■ MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)



Address	Register	Abbreviation	Access	Resource name	Initial value
000020_H	Serial Mode Register 0	SMR0	W,R/W	UART0	00000000_B
000021_H	Serial Control Register 0	SCR0	W,R/W		00000000_B
000022_H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000_B
000023_H	Serial Status Register 0	SSR0	R,R/W		00001000_B
000024_H	Extended Communication Control Register 0	ECCR0	R,W, R/W		$000000XX_B$
000025_H	Extended Status/Control Register 0	ESCR0	R/W		00000100_B
000026_H	Baud Rate Generator Register 00	BGR00	R/W		00000000_B
000027_H	Baud Rate Generator Register 01	BGR01	R/W		00000000_B
000028_H	Serial Mode Register 1	SMR1	W,R/W	UART1	00000000_B
000029_H	Serial Control Register 1	SCR1	W,R/W		00000000_B
$00002A_H$	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000_B
$00002B_H$	Serial Status Register 1	SSR1	R,R/W		00001000_B
$00002C_H$	Extended Communication Control Register 1	ECCR1	R,W, R/W		$000000XX_B$
$00002D_H$	Extended Status/Control Register 1	ESCR1	R/W		00000100_B
$00002E_H$	Baud Rate Generator Register 10	BGR10	R/W		00000000_B
$00002F_H$	Baud Rate Generator Register 11	BGR11	R/W		00000000_B
000030_H	PPG 0 Operation Mode Control Register	PPGC0	W,R/W	16-bit PPG 0/1	$0X000XX1_B$
000031_H	PPG 1 Operation Mode Control Register	PPGC1	W,R/W		$0X000001_B$
000032_H	PPG 0/PPG 1 Count Clock Select Register	PPG01	R/W		$000000X0_B$
000033_H	Reserved				
000034_H	PPG 2 Operation Mode Control Register	PPGC2	W,R/W	16-bit PPG 2/3	$0X000XX1_B$
000035_H	PPG 3 Operation Mode Control Register	PPGC3	W,R/W		$0X000001_B$
000036_H	PPG 2/PPG 3 Count Clock Select Register	PPG23	R/W		$000000X0_B$
000037_H	Reserved				
000038_H	PPG 4 Operation Mode Control Register	PPGC4	W,R/W	16-bit PPG 4/5	$0X000XX1_B$
000039_H	PPG 5 Operation Mode Control Register	PPGC5	W,R/W		$0X000001_B$
$00003A_H$	PPG 4/PPG 5 Clock Select Register	PPG45	R/W		$000000X0_B$
$00003B_H$	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000_B
$00003C_H$	PPG 6 Operation Mode Control Register	PPGC6	W,R/W	16-bit PPG 6/7	$0X000XX1_B$
$00003D_H$	PPG 7 Operation Mode Control Register	PPGC7	W,R/W		$0X000001_B$
$00003E_H$	PPG 6/PPG 7 Count Clock Control Register	PPG67	R/W		$000000X0_B$
$00003F_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000040_H	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	$0X000XX1_B$
000041_H	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		$0X000001_B$
000042_H	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		$000000X0_B$
000043_H	Reserved				
000044_H	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	$0X000XX1_B$
000045_H	PPG B Operation Mode Control Register	PPGCB	W,R/W		$0X000001_B$
000046_H	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		$000000X0_B$
000047_H	Reserved				
000048_H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	$0X000XX1_B$
000049_H	PPG D Operation Mode Control Register	PPGCD	W,R/W		$0X000001_B$
$00004A_H$	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		$000000X0_B$
$00004B_H$	Reserved				
$00004C_H$	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	$0X000XX1_B$
$00004D_H$	PPG F Operation Mode Control Register	PPGCF	W,R/W		$0X000001_B$
$00004E_H$	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		$000000X0_B$
$00004F_H$	Reserved				
000050_H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000_B
000051_H	Input Capture Edge 0/1	ICE01	R/W, R		$XXX0X0XX_B$
000052_H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000_B
000053_H	Input Capture Edge 2/3	ICE23	R		$XXXXXXXX_B$
000054_H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000_B
000055_H	Input Capture Edge 4/5	ICE45	R		$XXXXXXXX_B$
000056_H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000_B
000057_H	Input Capture Edge 6/7	ICE67	R/W, R		$XXX000XX_B$
000058_H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	$0000XX00_B$
000059_H	Output Compare Control Status 1	OCS1	R/W		$0XX00000_B$
$00005A_H$	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	$0000XX00_B$
$00005B_H$	Output Compare Control Status 3	OCS3	R/W		$0XX00000_B$
$00005C_H$	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	$0000XX00_B$
$00005D_H$	Output Compare Control Status 5	OCS5	R/W		$0XX00000_B$
$00005E_H$	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	$0000XX00_B$
$00005F_H$	Output Compare Control Status 7	OCS7	R/W		$0XX00000_B$

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Address	Register	Abbreviation	Access	Resource name	Initial value
000060_H	Timer Control Status 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000_B
000061_H	Timer Control Status 0	TMCSR0	R/W		$XXXX0000_B$
000062_H	Timer Control Status 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000_B
000063_H	Timer Control Status 1	TMCSR1	R/W		$XXXX0000_B$
000064_H	Timer Control Status 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000_B
000065_H	Timer Control Status 2	TMCSR2	R/W		$XXXX0000_B$
000066_H	Timer Control Status 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000_B
000067_H	Timer Control Status 3	TMCSR3	R/W		$XXXX0000_B$
000068_H	A/D Control Status 0	ADCS0	R/W	A/D Converter	$000XXXX0_B$
000069_H	A/D Control Status 1	ADCS1	R/W		$0000000X_B$
$00006A_H$	A/D Data 0	ADCR0	R		00000000_B
$00006B_H$	A/D Data 1	ADCR1	R		$XXXXXX00_B$
$00006C_H$	ADC Setting 0	ADSR0	R/W		00000000_B
$00006D_H$	ADC Setting 1	ADSR1	R/W		00000000_B
$00006E_H$	Reserved				
$00006F_H$	ROM Mirror Function Select	ROMM	W	ROM Mirror	$XXXXXXX1_B$
000070_H to $00008F_H$	Reserved for CAN Controller 0/1. Refer to "CAN Controllers"				
000090_H to $00009A_H$	Reserved				
$00009B_H$	DMA Descriptor Channel Specified Register	DCSR	R/W	DMA	00000000_B
$00009C_H$	DMA Status L Register	DSRL	R/W		00000000_B
$00009D_H$	DMA Status H Register	DSRH	R/W		00000000_B
$00009E_H$	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000_B
$00009F_H$	Delayed Interrupt Trigger/Release Register	DIRR	R/W	Delayed Interrupt	$XXXXXXX0_B$
$0000A0_H$	Low-power Mode Control Register	LPMCR	W,R/W	Low Power Control Circuit	00011000_B
$0000A1_H$	Clock Selection Register	CKSCR	R,R/W	Low Power Control Circuit	11111100_B
$0000A2_H$, $0000A3_H$	Reserved				
$0000A4_H$	DMA Stop Status Register	DSSR	R/W	DMA	00000000_B

(Continued)

List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A40_H$	$007C40_H$	ID Register 8	IDR8	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A41_H$	$007C41_H$				
$007A42_H$	$007C42_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A43_H$	$007C43_H$				
$007A44_H$	$007C44_H$	ID Register 9	IDR9	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A45_H$	$007C45_H$				
$007A46_H$	$007C46_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A47_H$	$007C47_H$				
$007A48_H$	$007C48_H$	ID Register 10	IDR10	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A49_H$	$007C49_H$				
$007A4A_H$	$007C4A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4B_H$	$007C4B_H$				
$007A4C_H$	$007C4C_H$	ID Register 11	IDR11	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4D_H$	$007C4D_H$				
$007A4E_H$	$007C4E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4F_H$	$007C4F_H$				
$007A50_H$	$007C50_H$	ID Register 12	IDR12	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A51_H$	$007C51_H$				
$007A52_H$	$007C52_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A53_H$	$007C53_H$				
$007A54_H$	$007C54_H$	ID Register 13	IDR13	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A55_H$	$007C55_H$				
$007A56_H$	$007C56_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A57_H$	$007C57_H$				
$007A58_H$	$007C58_H$	ID Register 14	IDR14	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A59_H$	$007C59_H$				
$007A5A_H$	$007C5A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5B_H$	$007C5B_H$				
$007A5C_H$	$007C5C_H$	ID Register 15	IDR15	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5D_H$	$007C5D_H$				
$007A5E_H$	$007C5E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5F_H$	$007C5F_H$				

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A60_H$	$007C60_H$	DLC Register 0	DLCR0	R/W	$XXXXXXXX_B$
$007A61_H$	$007C61_H$				
$007A62_H$	$007C62_H$	DLC Register 1	DLCR1	R/W	$XXXXXXXX_B$
$007A63_H$	$007C63_H$				
$007A64_H$	$007C64_H$	DLC Register 2	DLCR2	R/W	$XXXXXXXX_B$
$007A65_H$	$007C65_H$				
$007A66_H$	$007C66_H$	DLC Register 3	DLCR3	R/W	$XXXXXXXX_B$
$007A67_H$	$007C67_H$				
$007A68_H$	$007C68_H$	DLC Register 4	DLCR4	R/W	$XXXXXXXX_B$
$007A69_H$	$007C69_H$				
$007A6A_H$	$007C6A_H$	DLC Register 5	DLCR5	R/W	$XXXXXXXX_B$
$007A6B_H$	$007C6B_H$				
$007A6C_H$	$007C6C_H$	DLC Register 6	DLCR6	R/W	$XXXXXXXX_B$
$007A6D_H$	$007C6D_H$				
$007A6E_H$	$007C6E_H$	DLC Register 7	DLCR7	R/W	$XXXXXXXX_B$
$007A6F_H$	$007C6F_H$				
$007A70_H$	$007C70_H$	DLC Register 8	DLCR8	R/W	$XXXXXXXX_B$
$007A71_H$	$007C71_H$				
$007A72_H$	$007C72_H$	DLC Register 9	DLCR9	R/W	$XXXXXXXX_B$
$007A73_H$	$007C73_H$				
$007A74_H$	$007C74_H$	DLC Register 10	DLCR10	R/W	$XXXXXXXX_B$
$007A75_H$	$007C75_H$				
$007A76_H$	$007C76_H$	DLC Register 11	DLCR11	R/W	$XXXXXXXX_B$
$007A77_H$	$007C77_H$				
$007A78_H$	$007C78_H$	DLC Register 12	DLCR12	R/W	$XXXXXXXX_B$
$007A79_H$	$007C79_H$				
$007A7A_H$	$007C7A_H$	DLC Register 13	DLCR13	R/W	$XXXXXXXX_B$
$007A7B_H$	$007C7B_H$				
$007A7C_H$	$007C7C_H$	DLC Register 14	DLCR14	R/W	$XXXXXXXX_B$
$007A7D_H$	$007C7D_H$				
$007A7E_H$	$007C7E_H$	DLC Register 15	DLCR15	R/W	$XXXXXXXX_B$
$007A7F_H$	$007C7F_H$				

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$*2
	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH $\geq$ AVRL
Input voltage*1	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum Clamp Current	I_{CLAMP}	−4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	—	40	mA	*5
“L” level maximum output current	I_{OL}	—	15	mA	*4, *6
“L” level average output current	I_{OLAV}	—	4	mA	*4, *7
“L” level maximum overall output current	ΣI_{OL}	—	100	mA	*4
“L” level average overall output current	ΣI_{OLAV}	—	50	mA	*4, *8
“H” level maximum output current	I_{OH}	—	−15	mA	*4, *6
“H” level average output current	I_{OHAV}	—	−4	mA	*4, *7
“H” level maximum overall output current	ΣI_{OH}	—	−100	mA	*4
“H” level average overall output current	ΣI_{OHAV}	—	−50	mA	*4, *8
Power consumption	P_D	—	450	mW	
Operating temperature	T_A	−40	+105	°C	
Storage temperature	T_{STG}	−55	+150	°C	

*1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V

*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed $V_{CC} + 0.3$ V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, PA1

*5:
- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (Evaluation device : P50 to P55) , P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1
- Use within recommended operating conditions.
- Use with DC voltage (current)
- The +B signal should always be applied by using a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed the rated value, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.

(Continued)

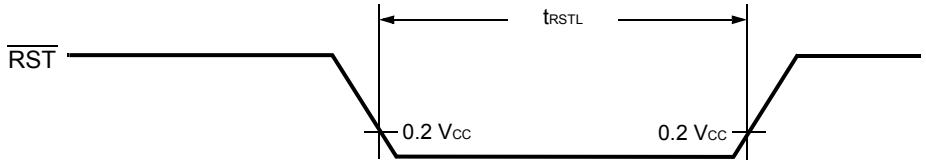
11.4.2 Reset Standby Input

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0.0 V)

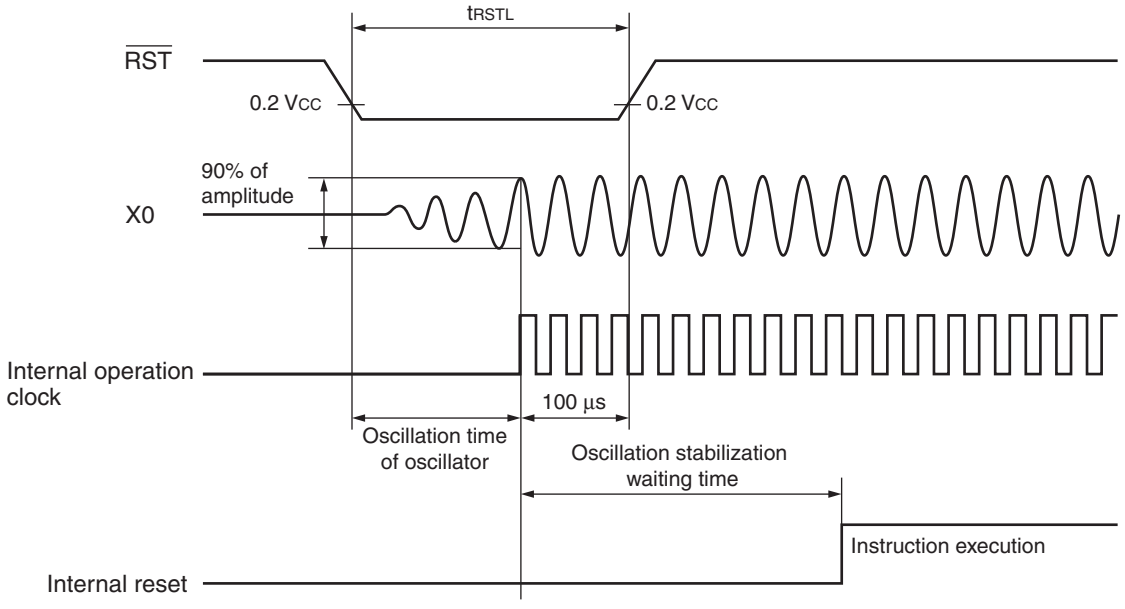
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 µs	—	µs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	µs	In Time Timer mode

* : The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

- **Under normal operation:**



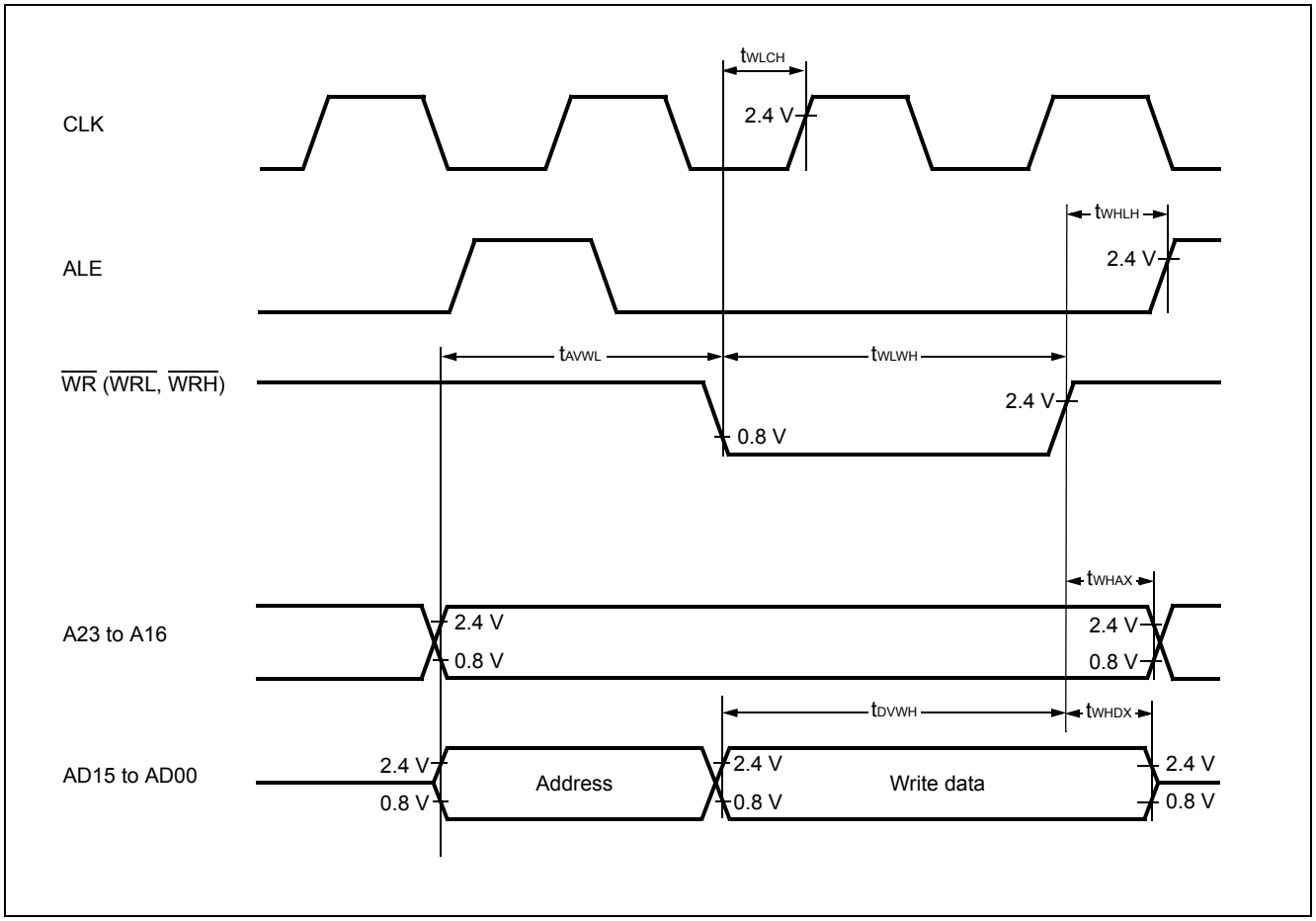
- **In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:**



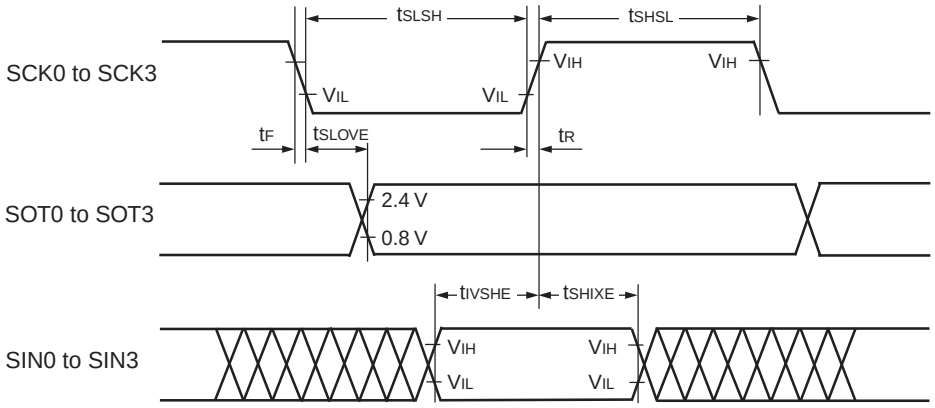
11.4.6 Bus Timing (Write)

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{WR}$	—	t_{CP}−15	—	ns
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		3 t_{CP}/2 − 20	—	ns
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	AD15 to AD00, $\overline{WR}$		3 t_{CP}/2 − 20	—	ns
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD15 to AD00, $\overline{WR}$		15	—	ns
$\overline{WR}$ ↑ → Address valid time	t_{WHAX}	A23 to A16, $\overline{WR}$		t_{CP}/2 − 10	—	ns
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		t_{CP}/2 − 15	—	ns
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		t_{CP}/2 − 15	—	ns



- External Shift Clock Mode



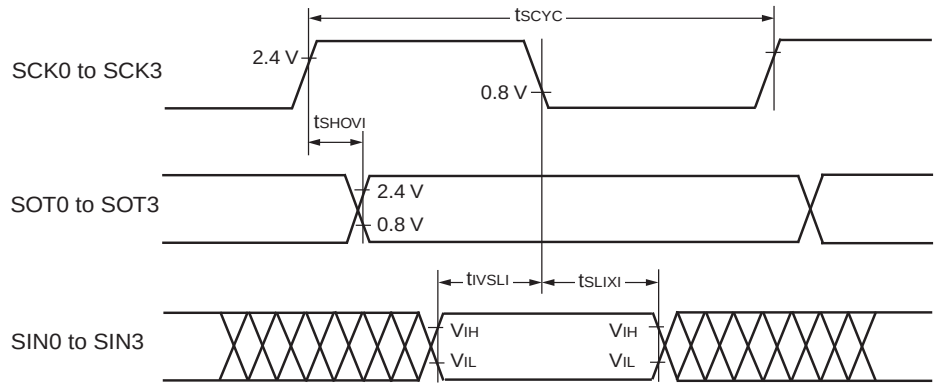
■ **Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0**

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

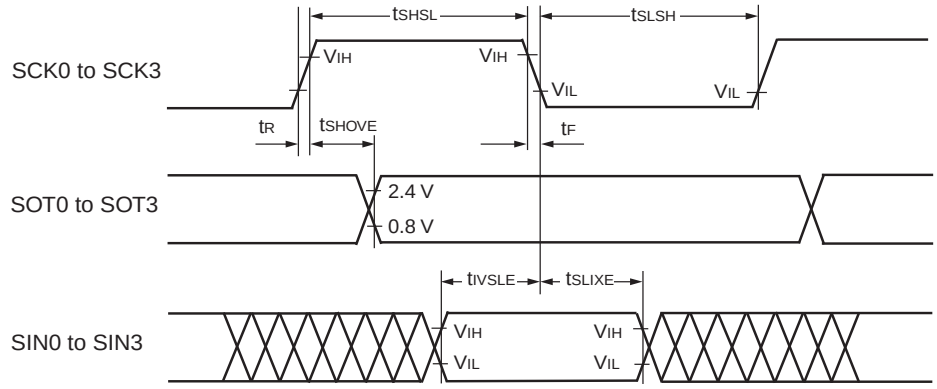
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		−50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK3		t_{CP} + 10	—	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↓	t_{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXE}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

Note:
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.

- Internal Shift Clock Mode



- External Shift Clock Mode

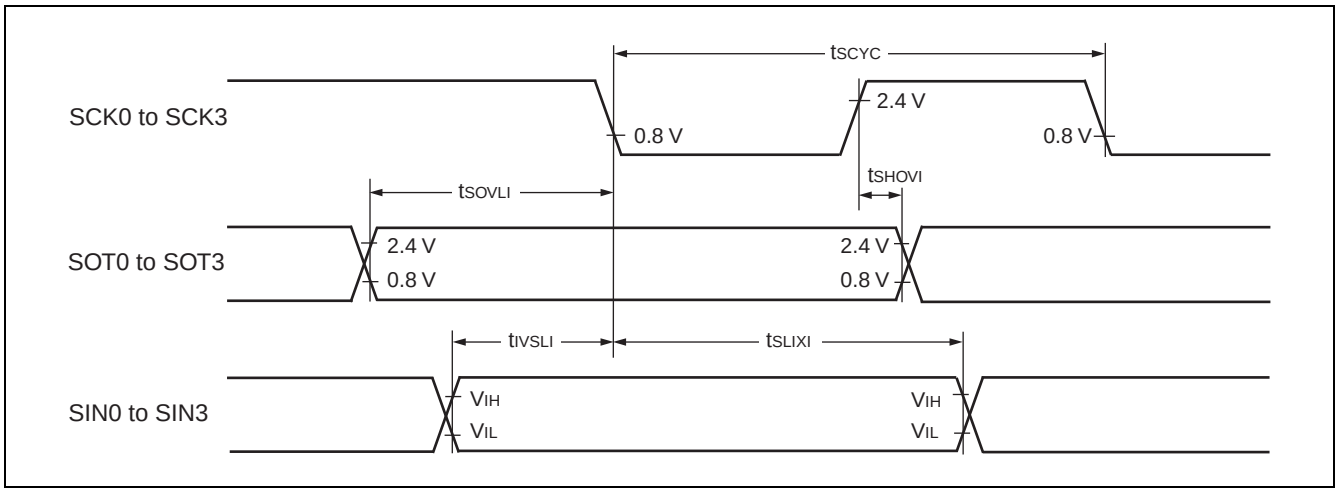


■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1**

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		−50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} − 70	—	ns

Note:
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".

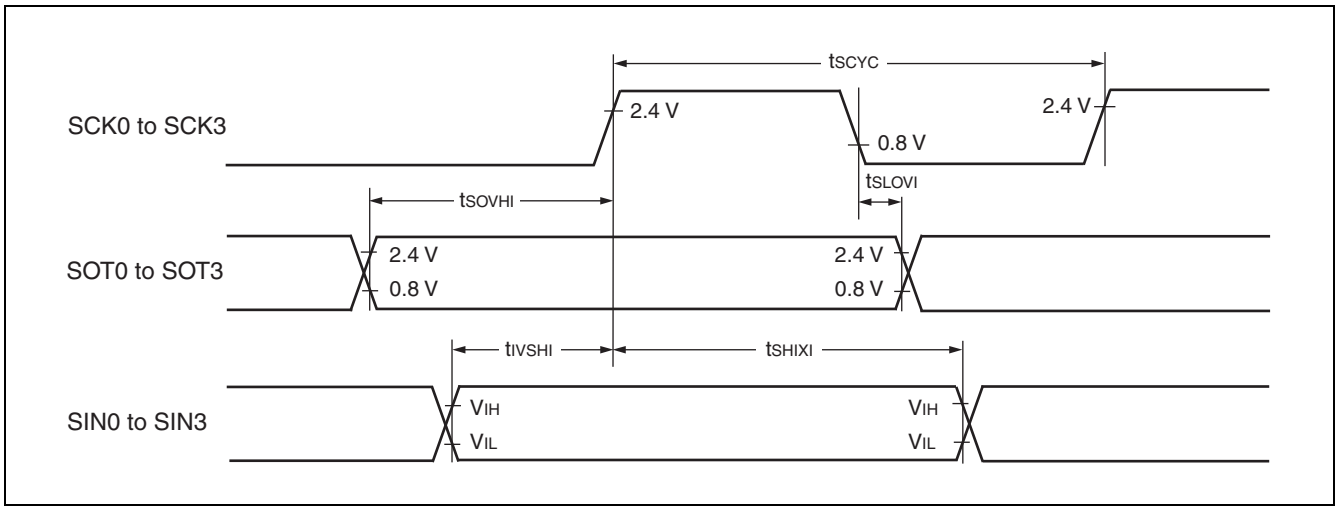


■ **Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1**

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		−50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} − 70	—	ns

Note:
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".

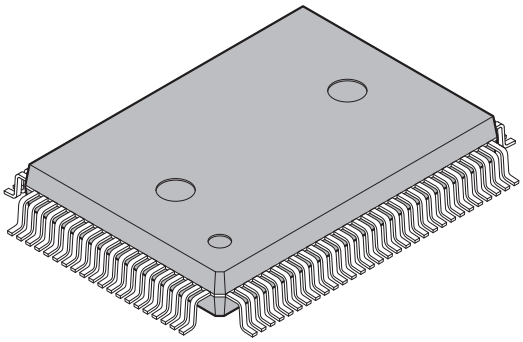


11.8 Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25°C$ $V_{CC} = 5.0$ V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	µs	Except for the over head time of the system
Program/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average $T_A = +85°C$	20	—	—	year	*

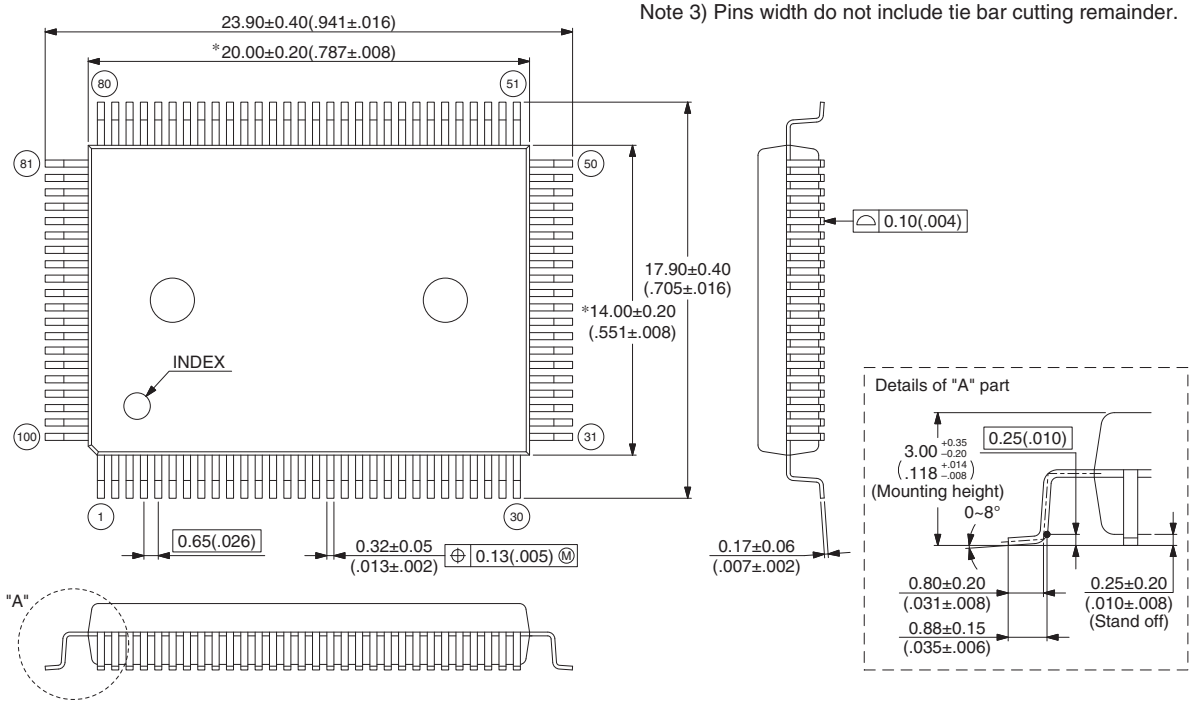
* : This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85°C) .

(Continued)

100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M06)		

100-pin plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.