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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

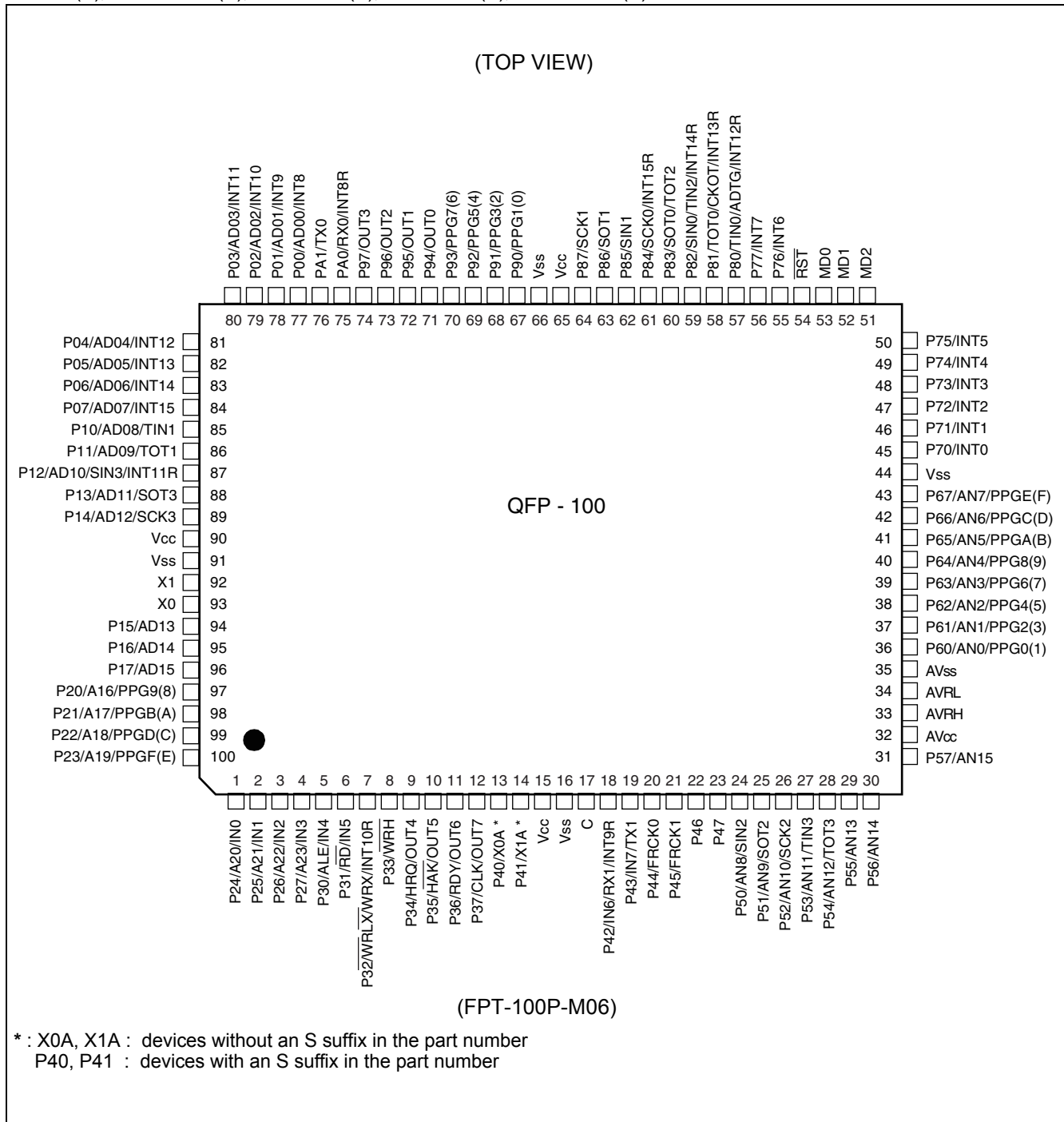
Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f342casprfr-gs-n2e1

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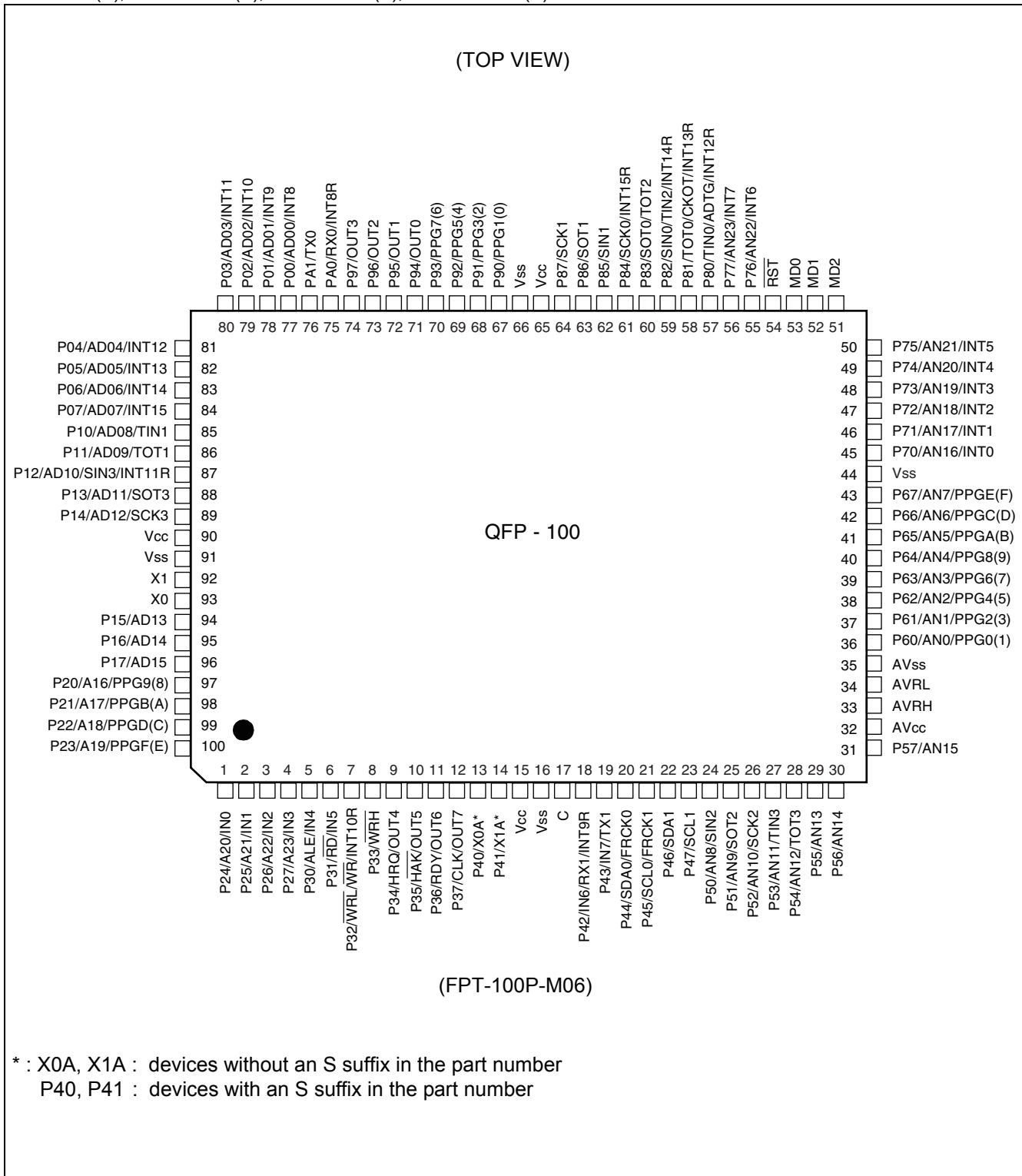
2. Pin Assignments

■ MB90341E(S), MB90342E(S), MB90F342E(S), MB90F345E(S), MB90346E(S), MB90F346E(S), MB90347E(S), MB90F347E(S), MB90348E(S), MB90349E(S), MB90F349E(S)



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■ MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)



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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
66	64	V _{SS}	—	GND pin
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pins
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pins
		OUT0 to OUT3		Waveform output pins for output compares. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin
76	74	PA1	F	General purpose I/O pin.
		TX0		TX Output pin for CAN0
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
86	84	P11	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer
87	85	P12	N	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin
88	86	P13	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
89	87	P14	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3
90	88	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
91	89	V _{SS}	—	GND pin
92	90	X1	A	Main clock output pin
93	91	X0		Main clock input pin
94	92	P15	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
95	93	P16	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.

(Continued)

5. Handling Devices

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC} , AV_{RH}) exceed the digital power-supply voltage.

2. Handling unused pins

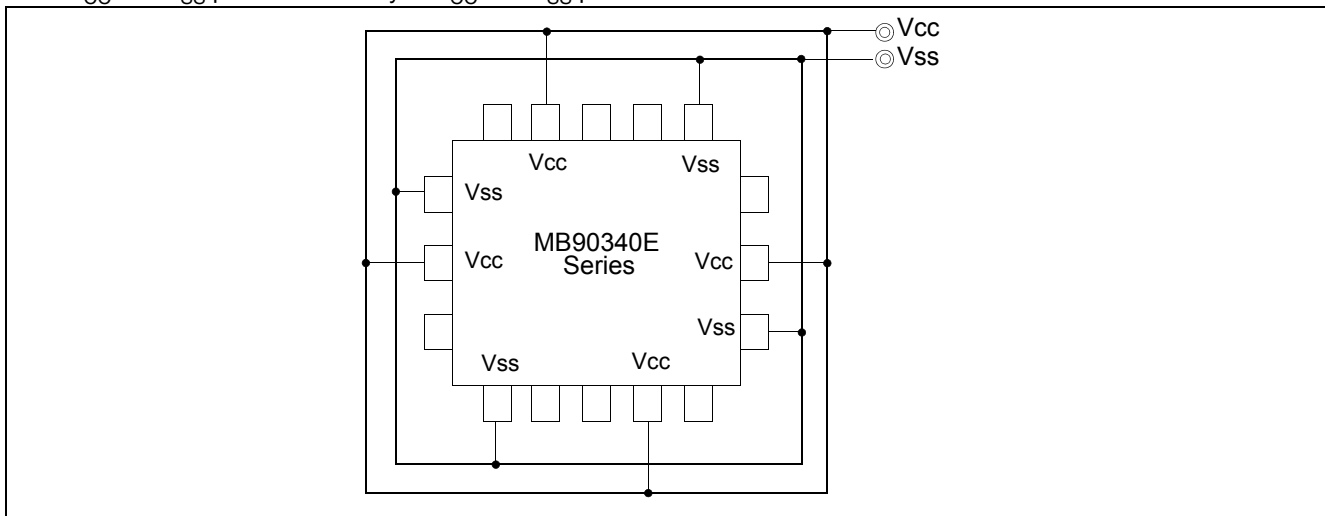
Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 k Ω or more.

3. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally. Connect V_{CC} and V_{SS} pins to the device from the current supply source at a possibly low impedance.

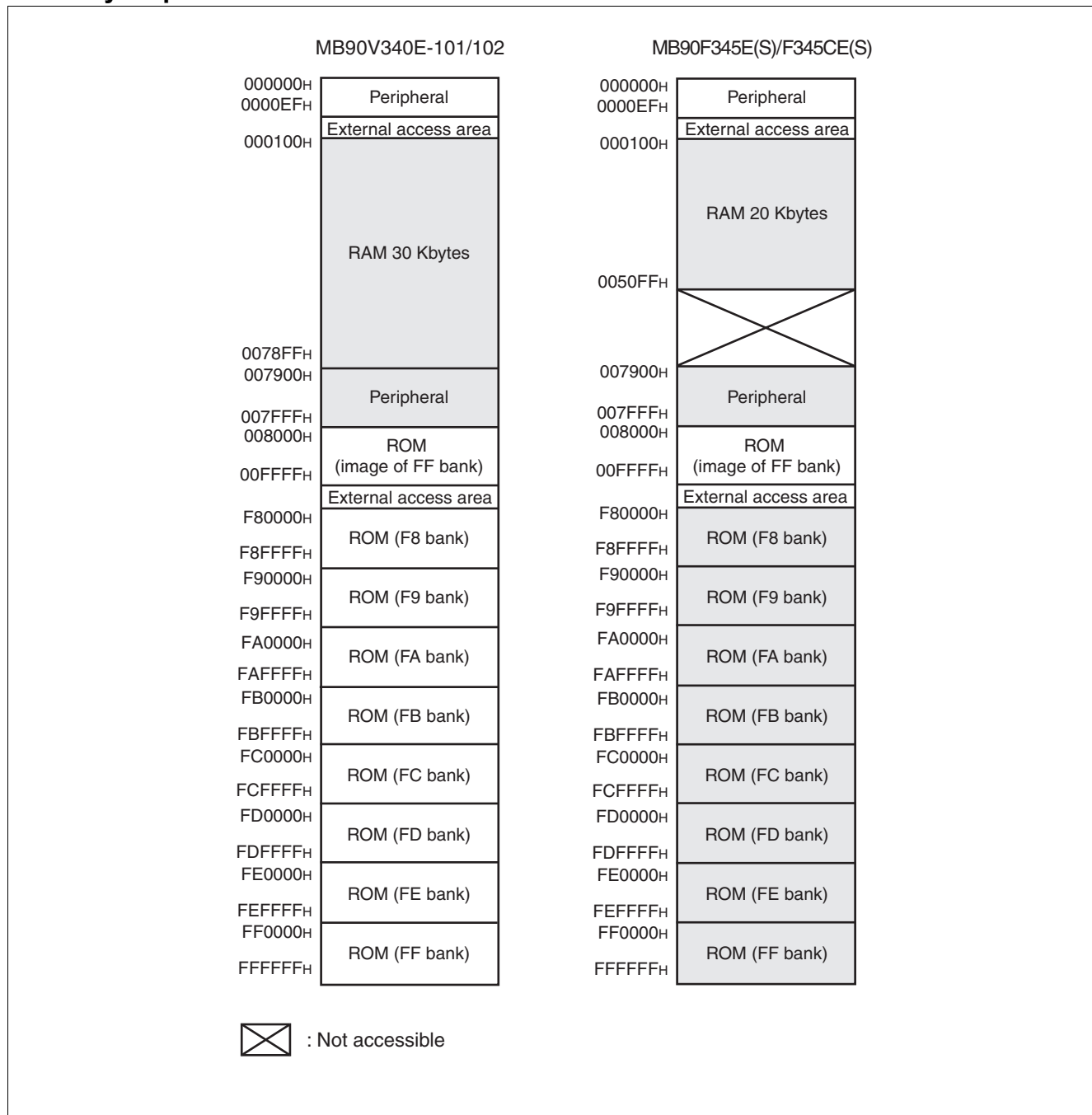
- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

7. Memory Map



MB90342E(S)/342CE(S)
MB90F342E(S)/F342CE(S)
MB90349E(S)/349CE(S)
MB90F349E(S)/F349CE(S)

MB90341E(S)/341CE(S)
MB90348E(S)/348CE(S)

MB90347E(S)/347CE(S)
MB90F347E(S)/F347CE(S)

MB90346E(S)/346CE(S)
MB90F346E(S)/F346CE(S)

000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral
	External access area		External access area		External access area		External access area
000100H		000100H		000100H	RAM 6 Kbytes	000100H	RAM 2 Kbytes
	RAM 16 Kbytes		RAM 16 Kbytes	0018FFH		0008FFH	
003FFFH		003FFFH					
007900H		007900H		007900H		007900H	
007FFFH	Peripheral	007FFFH	Peripheral	007FFFH	Peripheral	007FFFH	Peripheral
008000H		008000H		008000H		008000H	
00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)
	External access area		External access area		External access area		External access area
FC0000H							
FCFFFFH	ROM (FC bank)						
FD0000H							
FDFFFFH	ROM (FD bank)						
FE0000H		FE0000H		FE0000H		FE0000H	
FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	
FF0000H		FF0000H		FF0000H		FF0000H	
FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)

 : Not accessible

Note: :An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.

For example, when the address 00C000_H is accessed, the data at FFC000_H in ROM is actually accessed. The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00. As a result, the image between FF8000_H and FFFFFFF_H is visible in bank 00, while the image between FF0000_H and FF7FFF_H is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
000040 _H	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	0X000XX1 _B
000041 _H	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		0X000001 _B
000042 _H	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		000000X0 _B
000043 _H	Reserved				
000044 _H	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	0X000XX1 _B
000045 _H	PPG B Operation Mode Control Register	PPGCB	W,R/W		0X000001 _B
000046 _H	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		000000X0 _B
000047 _H	Reserved				
000048 _H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	0X000XX1 _B
000049 _H	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001 _B
00004A _H	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		000000X0 _B
00004B _H	Reserved				
00004C _H	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	0X000XX1 _B
00004D _H	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001 _B
00004E _H	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		000000X0 _B
00004F _H	Reserved				
000050 _H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000 _B
000051 _H	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XX _B
000052 _H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000 _B
000053 _H	Input Capture Edge 2/3	ICE23	R		XXXXXXXX _B
000054 _H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000 _B
000055 _H	Input Capture Edge 4/5	ICE45	R		XXXXXXXX _B
000056 _H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000 _B
000057 _H	Input Capture Edge 6/7	ICE67	R/W, R		XXX000XX _B
000058 _H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00 _B
000059 _H	Output Compare Control Status 1	OCS1	R/W		0XX00000 _B
00005A _H	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00 _B
00005B _H	Output Compare Control Status 3	OCS3	R/W		0XX00000 _B
00005C _H	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00 _B
00005D _H	Output Compare Control Status 5	OCS5	R/W		0XX00000 _B
00005E _H	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00 _B
00005F _H	Output Compare Control Status 7	OCS7	R/W		0XX00000 _B

(Continued)

List of Message Buffers (ID Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A00 _H to 007A1F _H	007C00 _H to 007C1F _H	General- Purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
007A20 _H	007C20 _H	ID Register 0	IDR0	R/W	XXXXXXXX _B XXXXXXXX _B
007A21 _H	007C21 _H				XXXXXXXX _B XXXXXXXX _B
007A22 _H	007C22 _H				XXXXXXXX _B XXXXXXXX _B
007A23 _H	007C23 _H				XXXXXXXX _B XXXXXXXX _B
007A24 _H	007C24 _H	ID Register 1	IDR1	R/W	XXXXXXXX _B XXXXXXXX _B
007A25 _H	007C25 _H				XXXXXXXX _B XXXXXXXX _B
007A26 _H	007C26 _H				XXXXXXXX _B XXXXXXXX _B
007A27 _H	007C27 _H				XXXXXXXX _B XXXXXXXX _B
007A28 _H	007C28 _H	ID Register 2	IDR2	R/W	XXXXXXXX _B XXXXXXXX _B
007A29 _H	007C29 _H				XXXXXXXX _B XXXXXXXX _B
007A2A _H	007C2A _H				XXXXXXXX _B XXXXXXXX _B
007A2B _H	007C2B _H				XXXXXXXX _B XXXXXXXX _B
007A2C _H	007C2C _H	ID Register 3	IDR3	R/W	XXXXXXXX _B XXXXXXXX _B
007A2D _H	007C2D _H				XXXXXXXX _B XXXXXXXX _B
007A2E _H	007C2E _H				XXXXXXXX _B XXXXXXXX _B
007A2F _H	007C2F _H				XXXXXXXX _B XXXXXXXX _B
007A30 _H	007C30 _H	ID Register 4	IDR4	R/W	XXXXXXXX _B XXXXXXXX _B
007A31 _H	007C31 _H				XXXXXXXX _B XXXXXXXX _B
007A32 _H	007C32 _H				XXXXXXXX _B XXXXXXXX _B
007A33 _H	007C33 _H				XXXXXXXX _B XXXXXXXX _B
007A34 _H	007C34 _H	ID Register 5	IDR5	R/W	XXXXXXXX _B XXXXXXXX _B
007A35 _H	007C35 _H				XXXXXXXX _B XXXXXXXX _B
007A36 _H	007C36 _H				XXXXXXXX _B XXXXXXXX _B
007A37 _H	007C37 _H				XXXXXXXX _B XXXXXXXX _B
007A38 _H	007C38 _H	ID Register 6	IDR6	R/W	XXXXXXXX _B XXXXXXXX _B
007A39 _H	007C39 _H				XXXXXXXX _B XXXXXXXX _B
007A3A _H	007C3A _H				XXXXXXXX _B XXXXXXXX _B
007A3B _H	007C3B _H				XXXXXXXX _B XXXXXXXX _B
007A3C _H	007C3C _H	ID Register 7	IDR7	R/W	XXXXXXXX _B XXXXXXXX _B
007A3D _H	007C3D _H				XXXXXXXX _B XXXXXXXX _B
007A3E _H	007C3E _H				XXXXXXXX _B XXXXXXXX _B
007A3F _H	007C3F _H				XXXXXXXX _B XXXXXXXX _B

List of Message Buffers (DLC Registers and Data Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A80 _H to 007A87 _H	007C80 _H to 007C87 _H	Data Register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B
007A88 _H to 007A8F _H	007C88 _H to 007C8F _H	Data Register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
007A90 _H to 007A97 _H	007C90 _H to 007C97 _H	Data Register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
007A98 _H to 007A9F _H	007C98 _H to 007C9F _H	Data Register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
007AA0 _H to 007AA7 _H	007CA0 _H to 007CA7 _H	Data Register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
007AA8 _H to 007AAF _H	007CA8 _H to 007CAF _H	Data Register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
007AB0 _H to 007AB7 _H	007CB0 _H to 007CB7 _H	Data Register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
007AB8 _H to 007ABF _H	007CB8 _H to 007CBF _H	Data Register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
007AC0 _H to 007AC7 _H	007CC0 _H to 007CC7 _H	Data Register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
007AC8 _H to 007ACF _H	007CC8 _H to 007CCF _H	Data Register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
007AD0 _H to 007AD7 _H	007CD0 _H to 007CD7 _H	Data Register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
007AD8 _H to 007ADF _H	007CD8 _H to 007CDF _H	Data Register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
007AE0 _H to 007AE7 _H	007CE0 _H to 007CE7 _H	Data Register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
007AE8 _H to 007AEF _H	007CE8 _H to 007CEF _H	Data Register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B

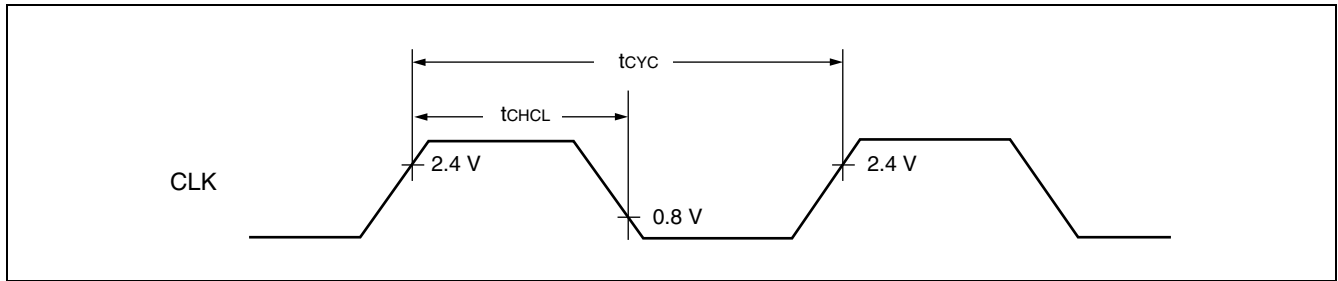
11.4 AC Characteristics

11.4.1 Clock Timing

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	When using an oscillation circuit
			4	—	16	MHz	PLL multiplied by 1 When using an oscillation circuit
			4	—	12	MHz	PLL multiplied by 2 When using an oscillation circuit
			4	—	8	MHz	PLL multiplied by 3 When using an oscillation circuit
			4	—	6	MHz	PLL multiplied by 4 When using an oscillation circuit
			—	—	4	MHz	PLL multiplied by 6 When using an oscillation circuit
			3	—	24	MHz	When using an external clock*
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	μs	When using sub clock

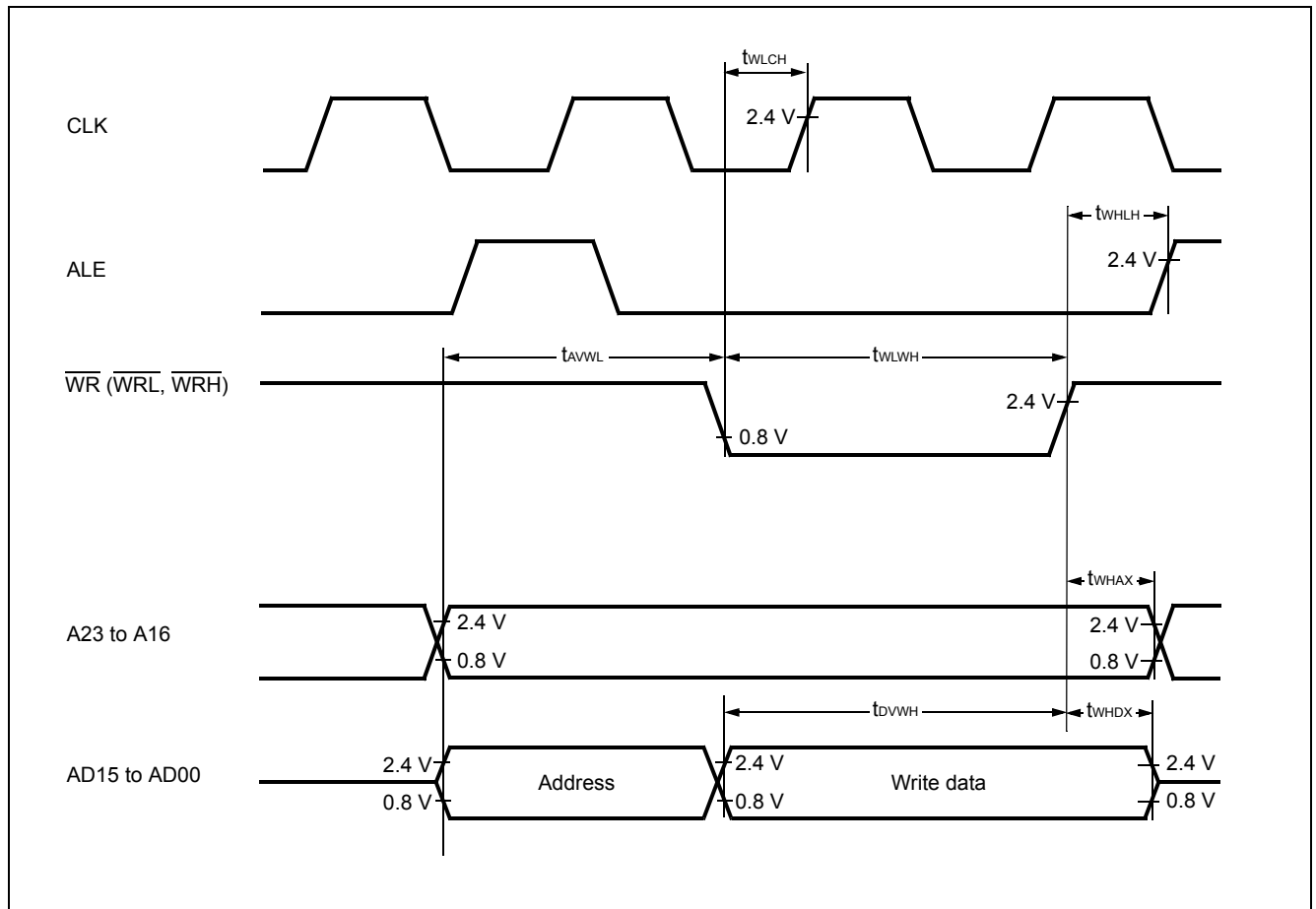
* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in "Relation between the external clock frequency and machine clock frequency".



11.4.6 Bus Timing (Write)

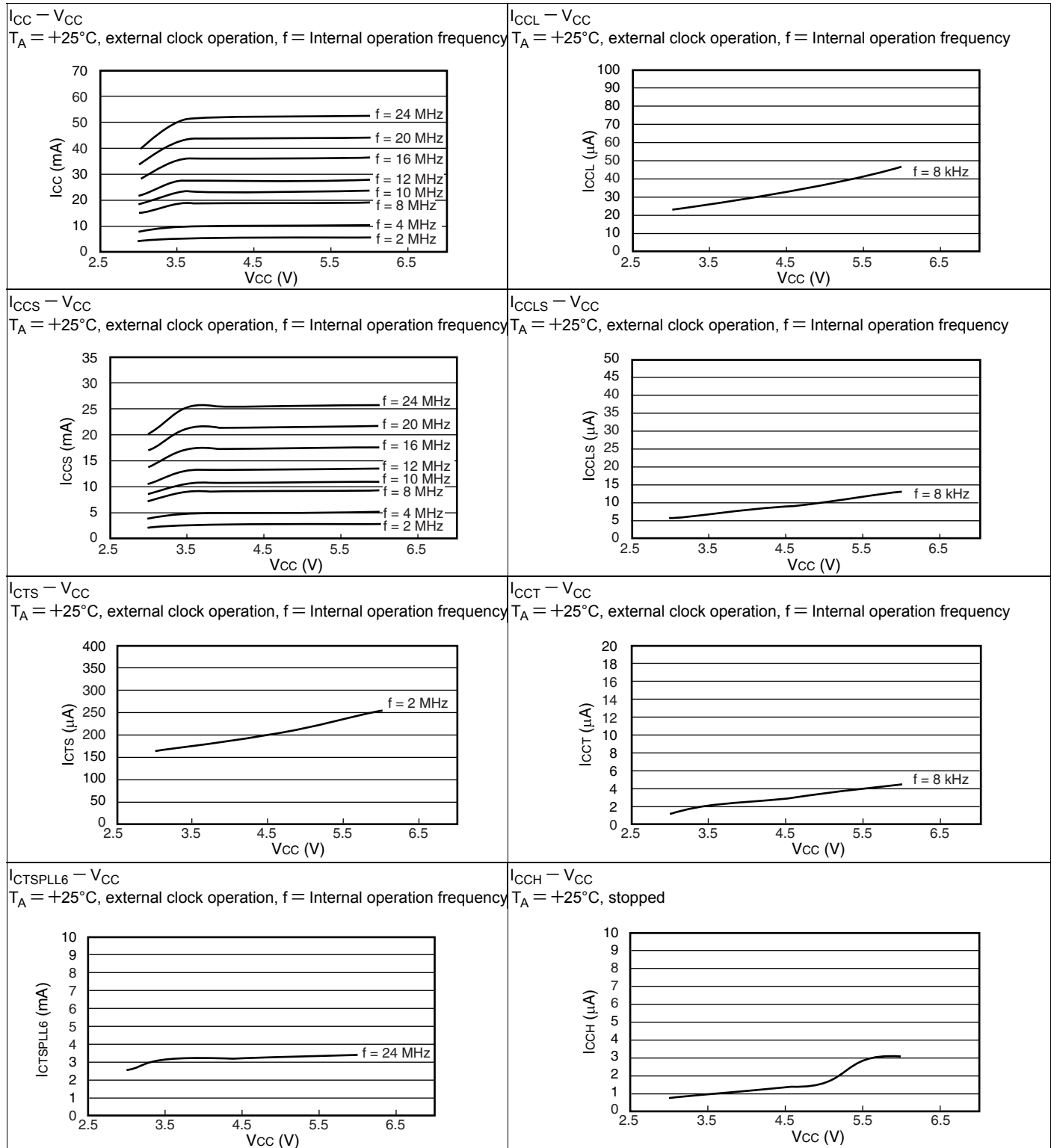
($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address $\rightarrow \overline{\text{WR}} \downarrow$ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{\text{WR}}$	—	$t_{\text{CP}} - 15$	—	ns
$\overline{\text{WR}}$ pulse width	t_{WLWH}	$\overline{\text{WR}}$		$3 t_{\text{CP}}/2 - 20$	—	ns
Valid data output $\rightarrow \overline{\text{WR}} \uparrow$ time	t_{DVWH}	AD15 to AD00, $\overline{\text{WR}}$		$3 t_{\text{CP}}/2 - 20$	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ Data hold time	t_{WHDX}	AD15 to AD00, $\overline{\text{WR}}$		15	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ Address valid time	t_{WHAX}	A23 to A16, $\overline{\text{WR}}$		$t_{\text{CP}}/2 - 10$	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ ALE $\uparrow$ time	t_{WHLH}	$\overline{\text{WR}}$, ALE		$t_{\text{CP}}/2 - 15$	—	ns
$\overline{\text{WR}} \downarrow \rightarrow$ CLK $\uparrow$ time	t_{WLCH}	$\overline{\text{WR}}$, CLK		$t_{\text{CP}}/2 - 15$	—	ns

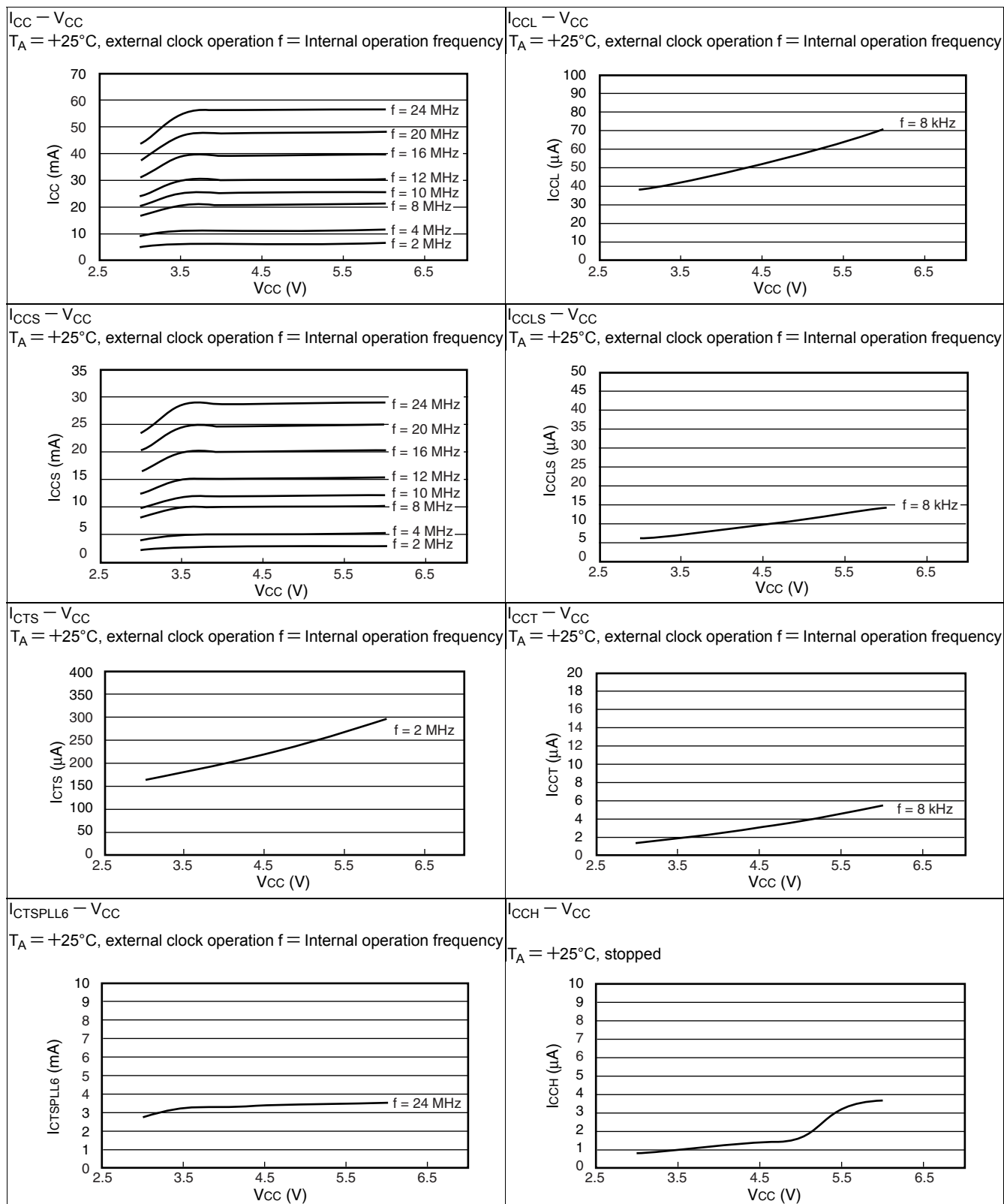


12. Example Characteristics

■ MB90F346E, MB90F346ES, MB90F346CE, MB90F346CES

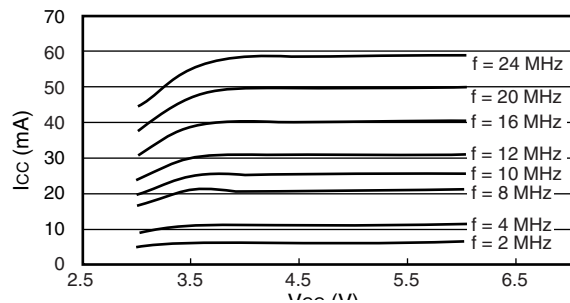


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

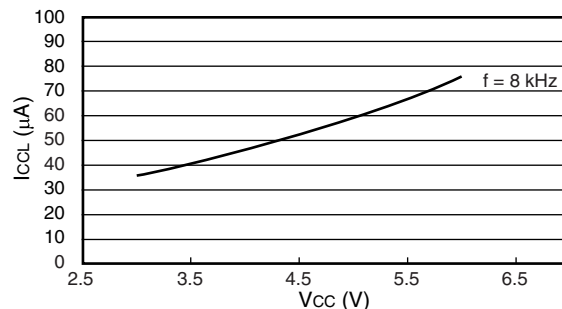


■ MB90F345E, MB90F345ES, MB90F345CE, MB90F345CES

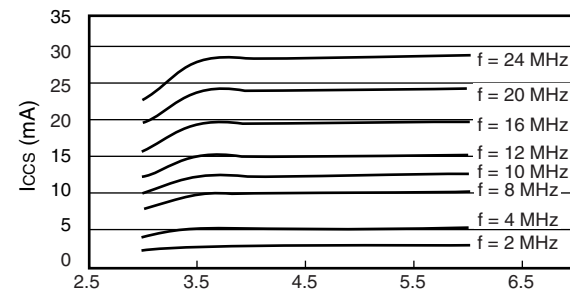
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



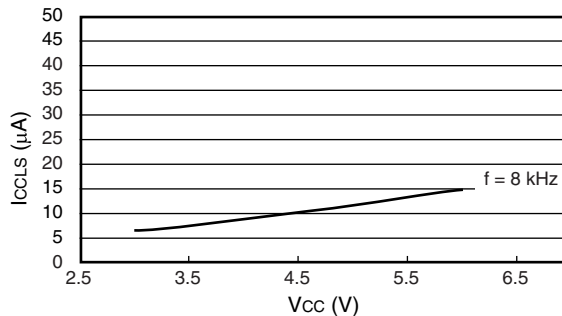
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



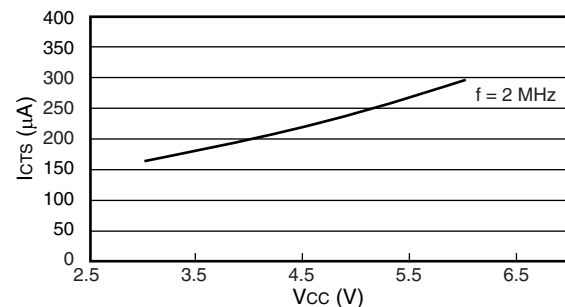
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



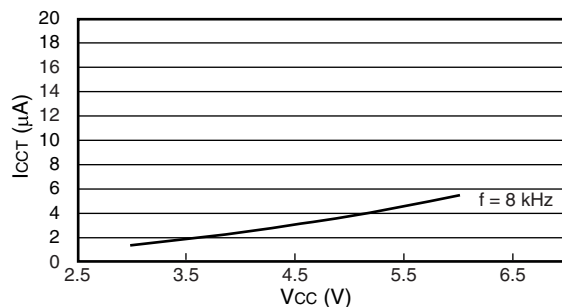
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



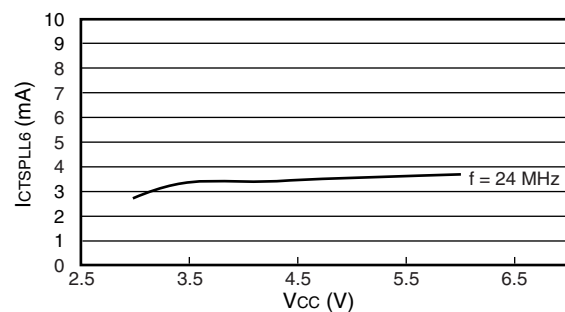
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



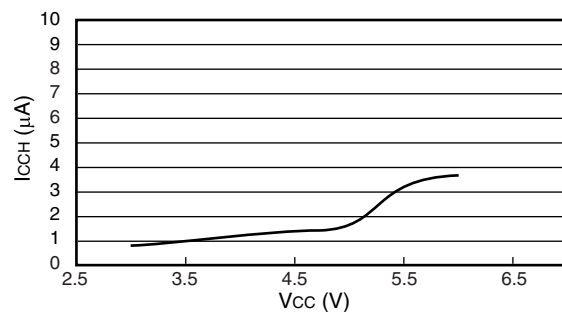
$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency

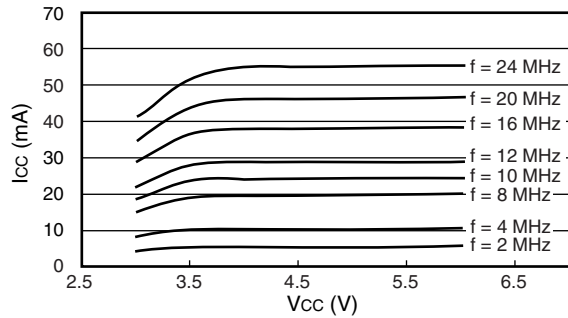


$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped

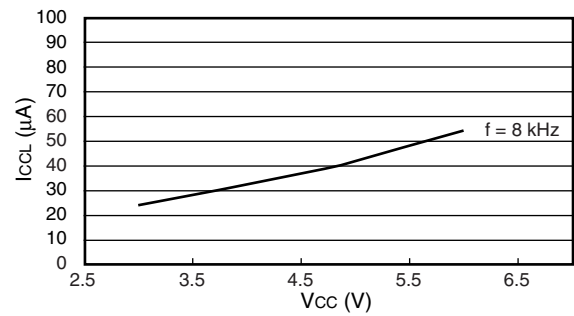


■ MB90347E, MB90347ES, MB90347CE, MB90347CES

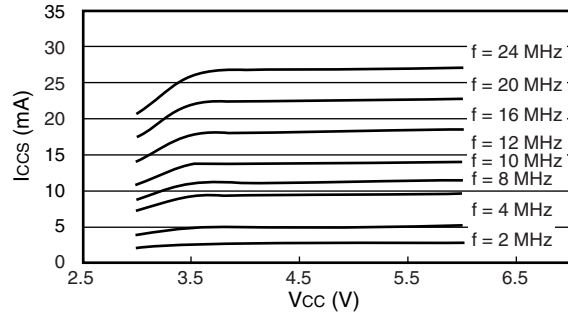
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



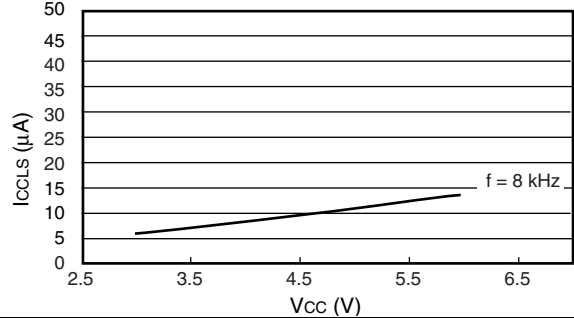
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



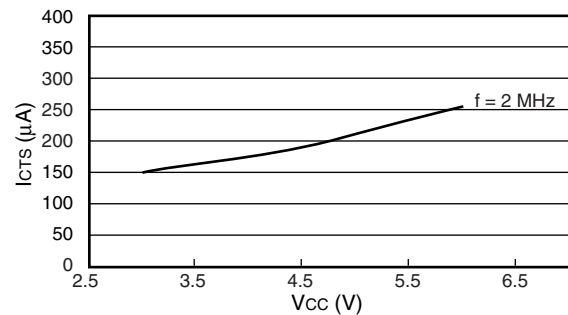
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



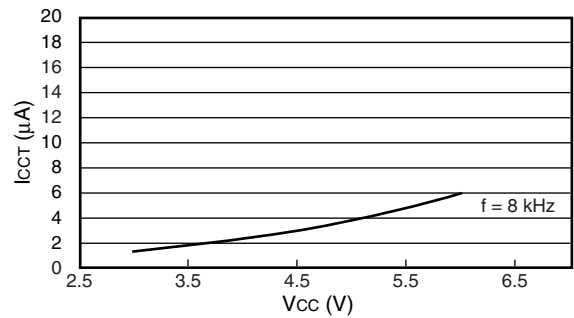
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



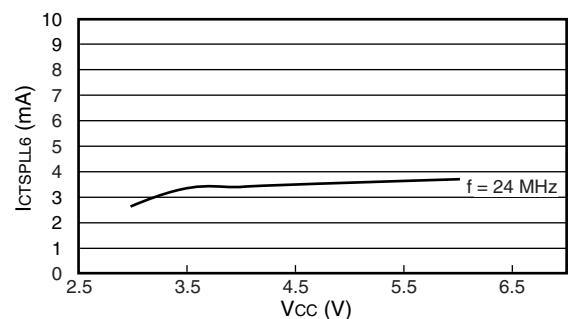
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



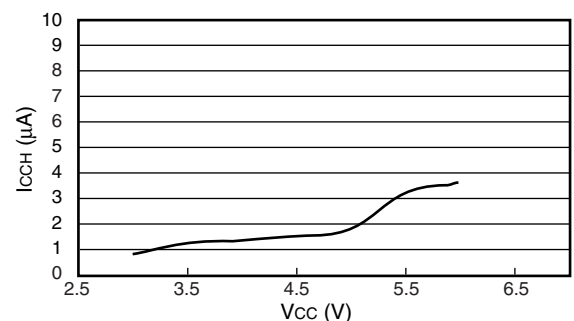
$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped



Part number	Package	Remarks
MB90F347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F347ESPF		
MB90F347CEPF		
MB90F347CESPF		
MB90F347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F347ESPMC		
MB90F347CEPMC		
MB90F347CESPMC		
MB90F349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F349ESPF		
MB90F349CEPF		
MB90F349CESPF		
MB90F349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F349ESPMC		
MB90F349CEPMC		
MB90F349CESPMC		
MB90341EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90341ESPF		
MB90341CEPF		
MB90341CESPF		
MB90341EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90341ESPMC		
MB90341CEPMC		
MB90341CESPMC		
MB90342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90342ESPF		
MB90342CEPF		
MB90342CESPF		
MB90342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90342ESPMC		
MB90342CEPMC		
MB90342CESPMC		

(Continued)

(Continued)

Part number	Package	Remarks
MB90346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90346ESPF		
MB90346CEPF		
MB90346CESPF		
MB90346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90346ESPMC		
MB90346CEPMC		
MB90346CESPMC		
MB90347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90347ESPF		
MB90347CEPF		
MB90347CESPF		
MB90347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90347ESPMC		
MB90347CEPMC		
MB90347CESPMC		
MB90348EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90348ESPF		
MB90348CEPF		
MB90348CESPF		
MB90348EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90348ESPMC		
MB90348CEPMC		
MB90348CESPMC		
MB90349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90349ESPF		
MB90349CEPF		
MB90349CESPF		
MB90349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90349ESPMC		
MB90349CEPMC		
MB90349CESPMC		
MB90V340E-101CR	299-pin ceramic PGA (PGA-299C-A01)	For evaluation
MB90V340E-102CR		