



Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

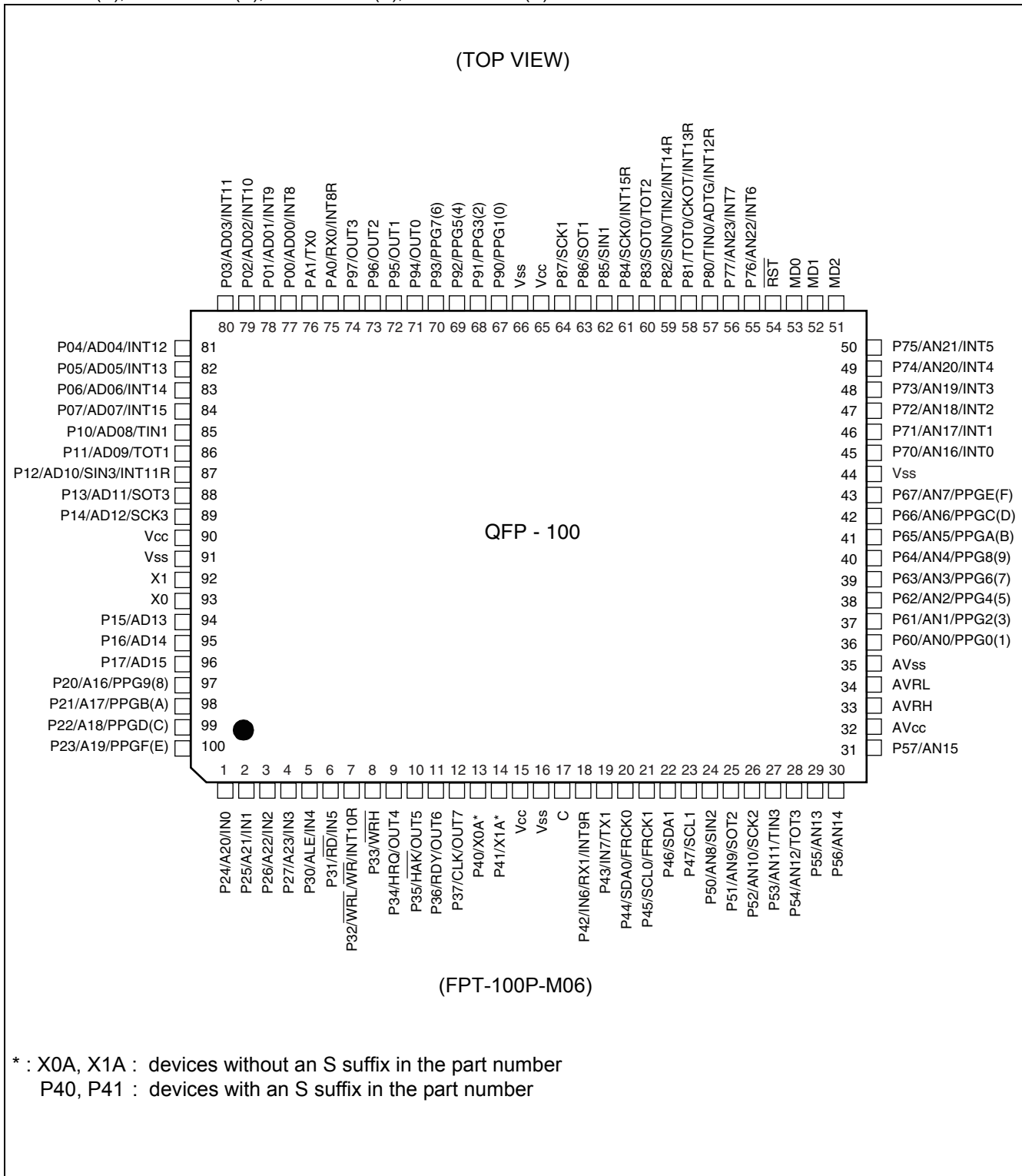
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

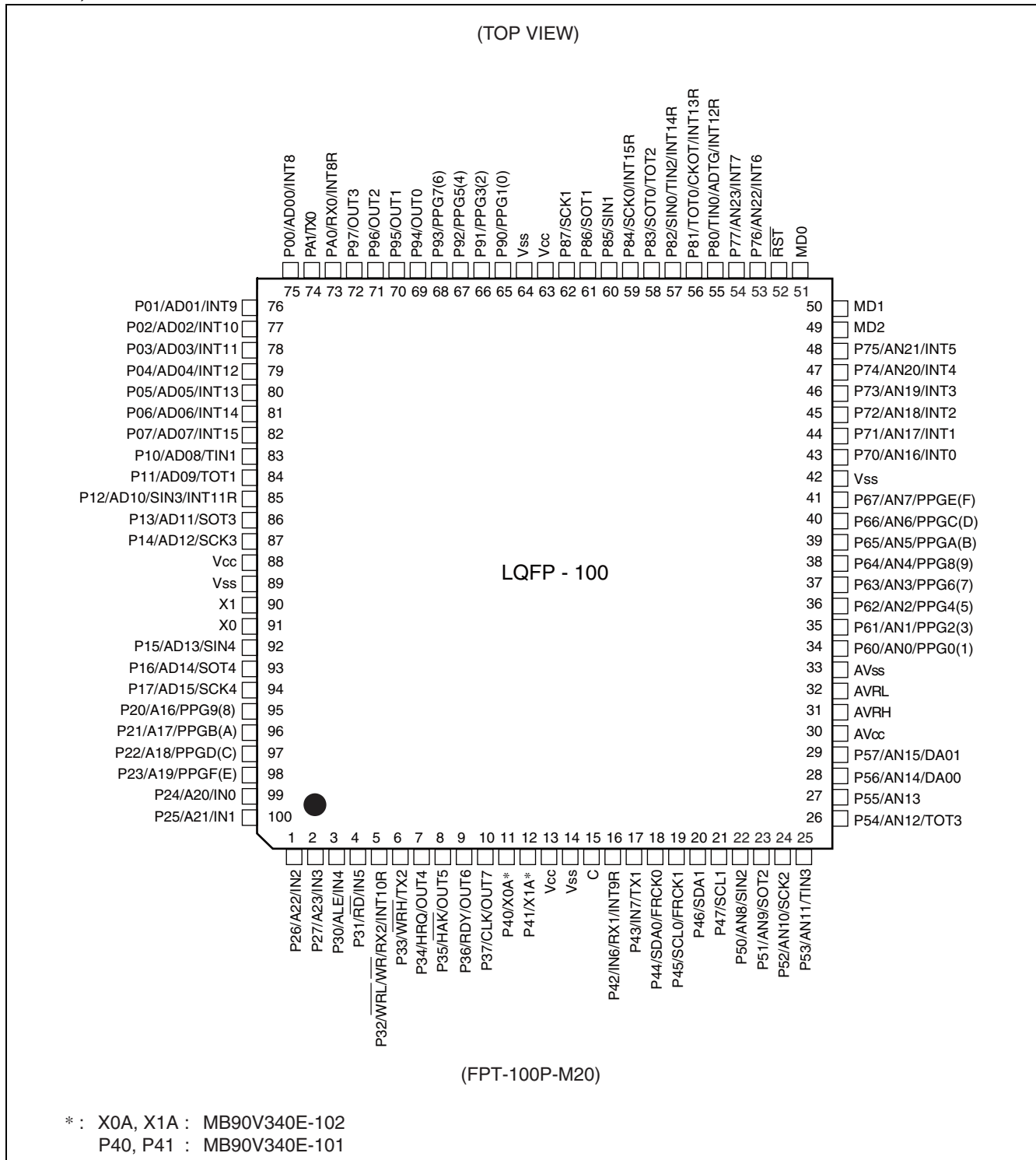
Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 24x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f342cespmc-ge1

■ MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)



(Continued)

(Continued)

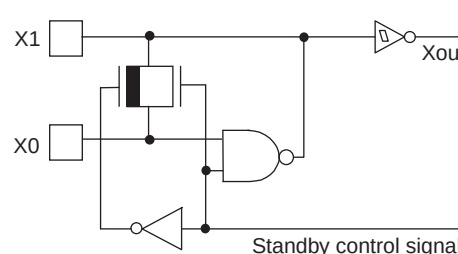
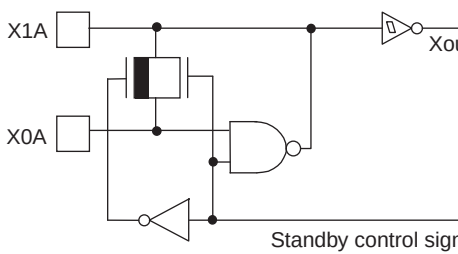
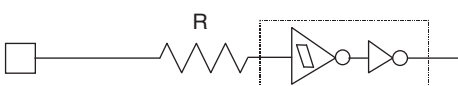
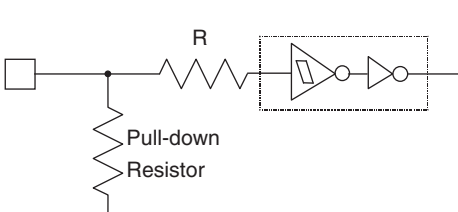
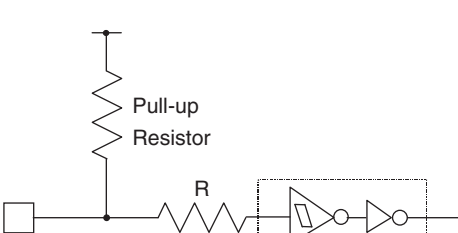


This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

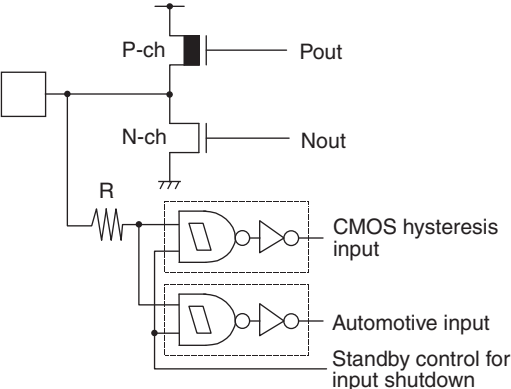
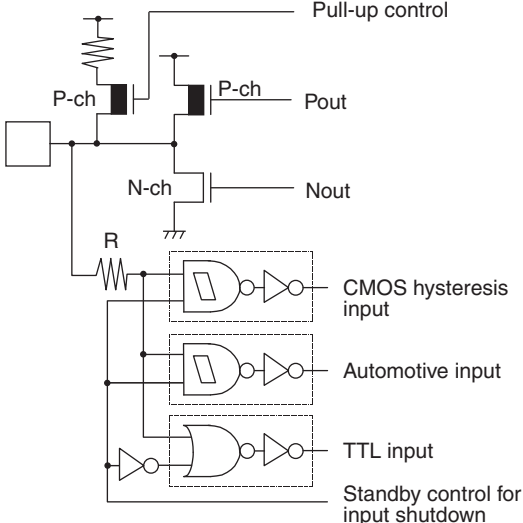
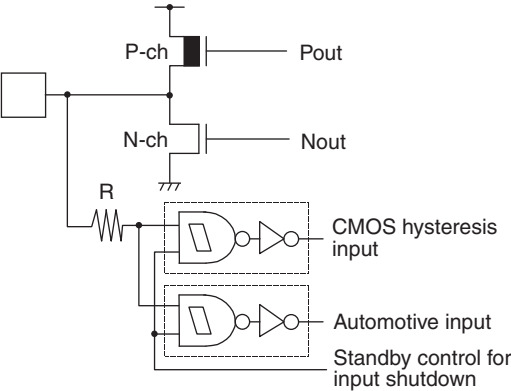
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV _{CC}	K	Analog power input pin for the A/D Converter

(Continued)

4. I/O Circuit Type

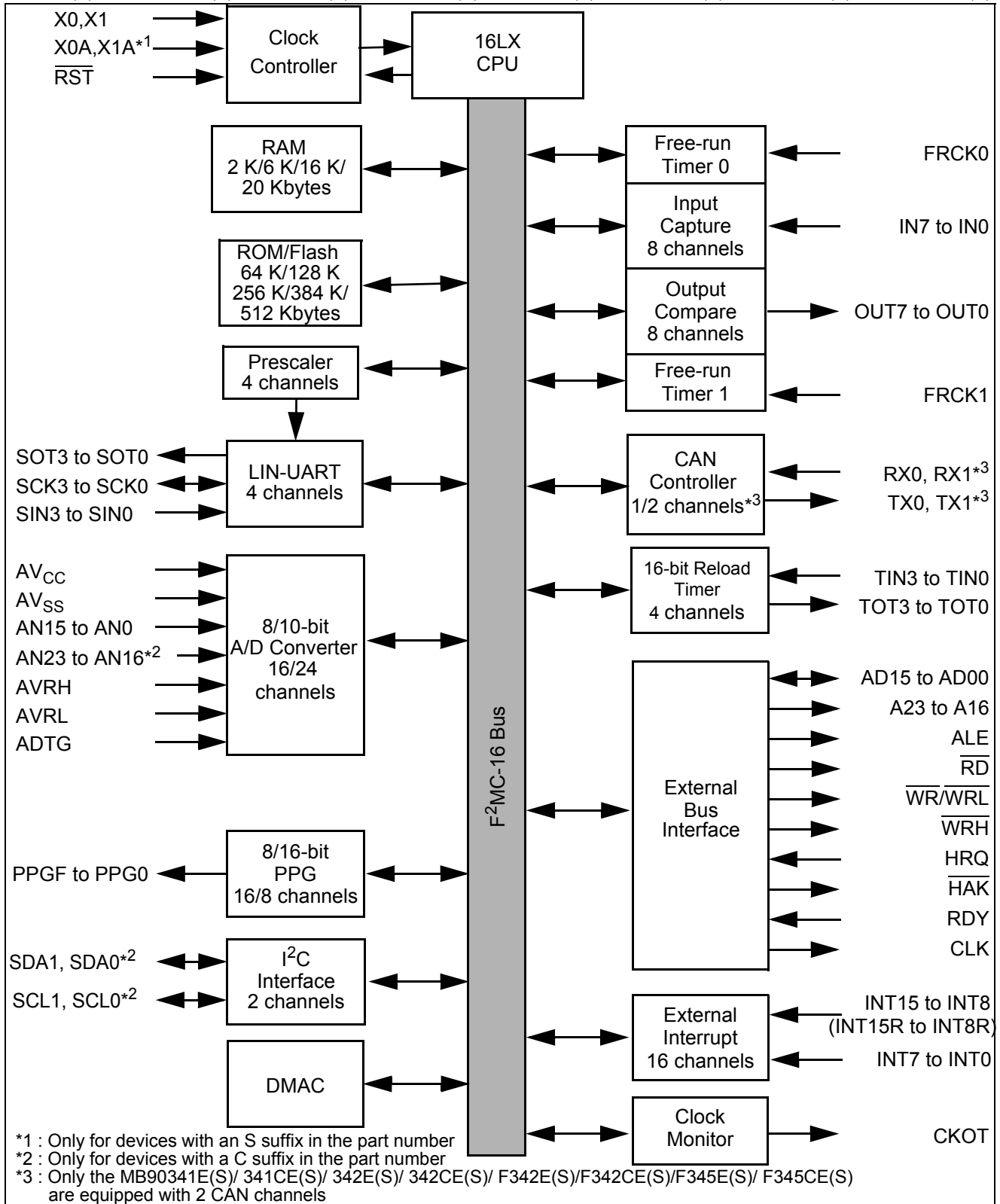
Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		■ MASK ROM and evaluation products: CMOS hysteresis input pin ■ Flash memory products: CMOS input pin
D		MASK ROM and evaluation products: ■ CMOS hysteresis input pin ■ Pull-down resistor value: approx. 50 kΩ Flash memory products: ■ CMOS input pin ■ No pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ

(Continued)

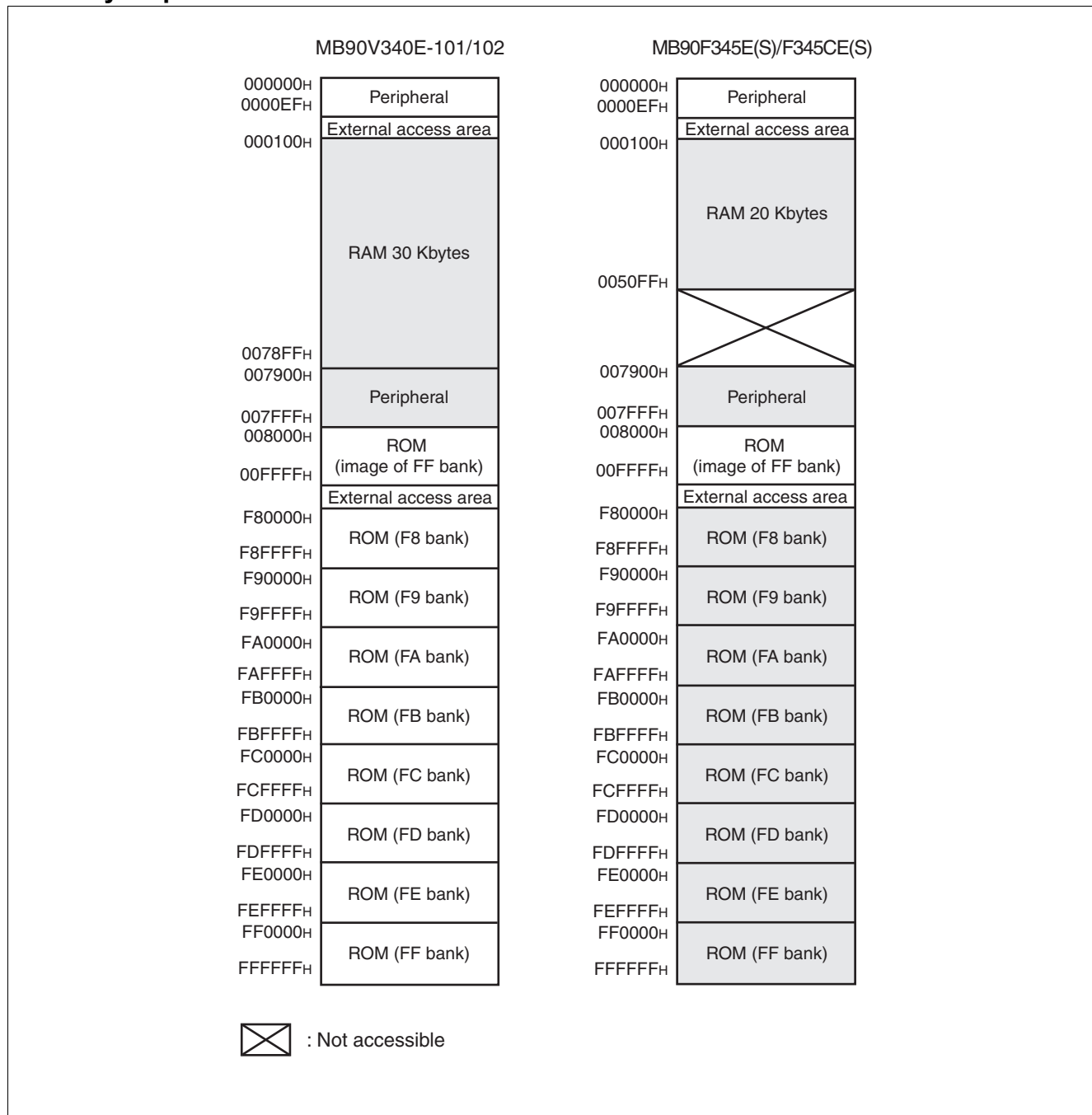
Type	Circuit	Remarks
F		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
G		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) ■ Programmable pull-up resistor: 50 kΩ approx.
H		■ CMOS level output ($I_{OL} = 3 \text{ mA}$, $I_{OH} = -3 \text{ mA}$) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)

(Continued)

■ MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)



7. Memory Map



Address	Register	Abbreviation	Access	Resource name	Initial value
000040 _H	PPG 8 Operation Mode Control Register	PPGC8	W,R/W	16-bit PPG 8/9	0X000XX1 _B
000041 _H	PPG 9 Operation Mode Control Register	PPGC9	W,R/W		0X000001 _B
000042 _H	PPG 8/PPG 9 Count Clock Control Register	PPG89	R/W		000000X0 _B
000043 _H	Reserved				
000044 _H	PPG A Operation Mode Control Register	PPGCA	W,R/W	16-bit PPG A/B	0X000XX1 _B
000045 _H	PPG B Operation Mode Control Register	PPGCB	W,R/W		0X000001 _B
000046 _H	PPG A/PPG B Count Clock Select Register	PPGAB	R/W		000000X0 _B
000047 _H	Reserved				
000048 _H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit PPG C/D	0X000XX1 _B
000049 _H	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001 _B
00004A _H	PPG C/PPG D Count Clock Select Register	PPGCD	R/W		000000X0 _B
00004B _H	Reserved				
00004C _H	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit PPG E/F	0X000XX1 _B
00004D _H	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001 _B
00004E _H	PPG E/PPG F Count Clock Select Register	PPGEF	R/W		000000X0 _B
00004F _H	Reserved				
000050 _H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000 _B
000051 _H	Input Capture Edge 0/1	ICE01	R/W, R		XXX0X0XX _B
000052 _H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000 _B
000053 _H	Input Capture Edge 2/3	ICE23	R		XXXXXXXX _B
000054 _H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000 _B
000055 _H	Input Capture Edge 4/5	ICE45	R		XXXXXXXX _B
000056 _H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000 _B
000057 _H	Input Capture Edge 6/7	ICE67	R/W, R		XXX000XX _B
000058 _H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	0000XX00 _B
000059 _H	Output Compare Control Status 1	OCS1	R/W		0XX00000 _B
00005A _H	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	0000XX00 _B
00005B _H	Output Compare Control Status 3	OCS3	R/W		0XX00000 _B
00005C _H	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	0000XX00 _B
00005D _H	Output Compare Control Status 5	OCS5	R/W		0XX00000 _B
00005E _H	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	0000XX00 _B
00005F _H	Output Compare Control Status 7	OCS7	R/W		0XX00000 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007924 _H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
007925 _H	Input Capture 2	IPCP2	R		XXXXXXXX _B
007926 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007927 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007928 _H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
007929 _H	Input Capture 4	IPCP4	R		XXXXXXXX _B
00792A _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
00792B _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
00792C _H	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
00792D _H	Input Capture 6	IPCP6	R		XXXXXXXX _B
00792E _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
00792F _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
007930 _H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
007931 _H	Output Compare 0	OCCP0	R/W		XXXXXXXX _B
007932 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007933 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007934 _H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
007935 _H	Output Compare 2	OCCP2	R/W		XXXXXXXX _B
007936 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007937 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007938 _H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX _B
007939 _H	Output Compare 4	OCCP4	R/W		XXXXXXXX _B
00793A _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793B _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793C _H	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX _B
00793D _H	Output Compare 6	OCCP6	R/W		XXXXXXXX _B
00793E _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
00793F _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
007940 _H	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000 _B
007941 _H	Timer Data 0	TCDT0	R/W		00000000 _B
007942 _H	Timer Control Status 0	TCCSL0	R/W		00000000 _B
007943 _H	Timer Control Status 0	TCCSH0	R/W		0XXXXXXXX _B
007944 _H	Timer Data 1	TCDT1	R/W	Free-run Timer 1	00000000 _B
007945 _H	Timer Data 1	TCDT1	R/W		00000000 _B
007946 _H	Timer Control Status 1	TCCSL1	R/W		00000000 _B
007947 _H	Timer Control Status 1	TCCSH1	R/W		0XXXXXXXX _B

(Continued)

List of Control Registers (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007B00 _H	007D00 _H	Control Status Register	CSR	R/W, W R/W, R	0XXXX0X1 _B 00XXX000 _B
007B01 _H	007D01 _H				
007B02 _H	007D02 _H	Last Event Indicator Register	LEIR	R/W	000X0000 _B XXXXXXXX _B
007B03 _H	007D03 _H				
007B04 _H	007D04 _H	Receive And Transmit Error Counter	RTEC	R	00000000 _B 00000000 _B
007B05 _H	007D05 _H				
007B06 _H	007D06 _H	Bit Timing Register	BTR	R/W	11111111 _B X1111111 _B
007B07 _H	007D07 _H				
007B08 _H	007D08 _H	IDE Register	IDER	R/W	XXXXXXXX _B XXXXXXXX _B
007B09 _H	007D09 _H				
007B0A _H	007D0A _H	Transmit RTR Register	TRTRR	R/W	00000000 _B 00000000 _B
007B0B _H	007D0B _H				
007B0C _H	007D0C _H	Remote Frame Receive Waiting Register	RFWTR	R/W	XXXXXXXX _B XXXXXXXX _B
007B0D _H	007D0D _H				
007B0E _H	007D0E _H	Transmit Interrupt Enable Register	TIER	R/W	00000000 _B 00000000 _B
007B0F _H	007D0F _H				
007B10 _H	007D10 _H	Acceptance Mask Select Register	AMSR	R/W	XXXXXXXX _B XXXXXXXX _B
007B11 _H	007D11 _H				
007B12 _H	007D12 _H				XXXXXXXX _B XXXXXXXX _B
007B13 _H	007D13 _H				
007B14 _H	007D14 _H	Acceptance Mask Register 0	AMR0	R/W	XXXXXXXX _B XXXXXXXX _B
007B15 _H	007D15 _H				
007B16 _H	007D16 _H				XXXXXXXX _B XXXXXXXX _B
007B17 _H	007D17 _H				
007B18 _H	007D18 _H	Acceptance Mask Register 1	AMR1	R/W	XXXXXXXX _B XXXXXXXX _B
007B19 _H	007D19 _H				
007B1A _H	007D1A _H				XXXXXXXX _B XXXXXXXX _B
007B1B _H	007D1B _H				

List of Message Buffers (ID Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A00 _H to 007A1F _H	007C00 _H to 007C1F _H	General- Purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
007A20 _H	007C20 _H	ID Register 0	IDR0	R/W	XXXXXXXX _B XXXXXXXX _B
007A21 _H	007C21 _H				XXXXXXXX _B XXXXXXXX _B
007A22 _H	007C22 _H				XXXXXXXX _B XXXXXXXX _B
007A23 _H	007C23 _H				XXXXXXXX _B XXXXXXXX _B
007A24 _H	007C24 _H	ID Register 1	IDR1	R/W	XXXXXXXX _B XXXXXXXX _B
007A25 _H	007C25 _H				XXXXXXXX _B XXXXXXXX _B
007A26 _H	007C26 _H				XXXXXXXX _B XXXXXXXX _B
007A27 _H	007C27 _H				XXXXXXXX _B XXXXXXXX _B
007A28 _H	007C28 _H	ID Register 2	IDR2	R/W	XXXXXXXX _B XXXXXXXX _B
007A29 _H	007C29 _H				XXXXXXXX _B XXXXXXXX _B
007A2A _H	007C2A _H				XXXXXXXX _B XXXXXXXX _B
007A2B _H	007C2B _H				XXXXXXXX _B XXXXXXXX _B
007A2C _H	007C2C _H	ID Register 3	IDR3	R/W	XXXXXXXX _B XXXXXXXX _B
007A2D _H	007C2D _H				XXXXXXXX _B XXXXXXXX _B
007A2E _H	007C2E _H				XXXXXXXX _B XXXXXXXX _B
007A2F _H	007C2F _H				XXXXXXXX _B XXXXXXXX _B
007A30 _H	007C30 _H	ID Register 4	IDR4	R/W	XXXXXXXX _B XXXXXXXX _B
007A31 _H	007C31 _H				XXXXXXXX _B XXXXXXXX _B
007A32 _H	007C32 _H				XXXXXXXX _B XXXXXXXX _B
007A33 _H	007C33 _H				XXXXXXXX _B XXXXXXXX _B
007A34 _H	007C34 _H	ID Register 5	IDR5	R/W	XXXXXXXX _B XXXXXXXX _B
007A35 _H	007C35 _H				XXXXXXXX _B XXXXXXXX _B
007A36 _H	007C36 _H				XXXXXXXX _B XXXXXXXX _B
007A37 _H	007C37 _H				XXXXXXXX _B XXXXXXXX _B
007A38 _H	007C38 _H	ID Register 6	IDR6	R/W	XXXXXXXX _B XXXXXXXX _B
007A39 _H	007C39 _H				XXXXXXXX _B XXXXXXXX _B
007A3A _H	007C3A _H				XXXXXXXX _B XXXXXXXX _B
007A3B _H	007C3B _H				XXXXXXXX _B XXXXXXXX _B
007A3C _H	007C3C _H	ID Register 7	IDR7	R/W	XXXXXXXX _B XXXXXXXX _B
007A3D _H	007C3D _H				XXXXXXXX _B XXXXXXXX _B
007A3E _H	007C3E _H				XXXXXXXX _B XXXXXXXX _B
007A3F _H	007C3F _H				XXXXXXXX _B XXXXXXXX _B

10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI ² OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC _H	—	—
INT9 instruction	N	—	#09	FFFFD8 _H	—	—
Exception	N	—	#10	FFFFD4 _H	—	—
CAN 0 RX	N	—	#11	FFFFD0 _H	ICR00	0000B0 _H
CAN 0 TX/NS	N	—	#12	FFFFCC _H		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4 _H		
CAN 2 RX / I ² C0	N	—	#15	FFFFC0 _H	ICR02	0000B2 _H
CAN 2 TX/NS	N	—	#16	FFFFBC _H		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8 _H	ICR03	0000B3 _H
16-bit Reload Timer 1	Y1	1	#18	FFFFB4 _H		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0 _H	ICR04	0000B4 _H
16-bit Reload Timer 3	Y1	—	#20	FFFFAC _H		
PPG 0/1/4/5	N	—	#21	FFFFA8 _H	ICR05	0000B5 _H
PPG 2/3/6/7	N	—	#22	FFFFA4 _H		
PPG 8/9/C/D	N	—	#23	FFFFA0 _H	ICR06	0000B6 _H
PPG A/B/E/F	N	—	#24	FFFF9C _H		
Time Base Timer	N	—	#25	FFFF98 _H	ICR07	0000B7 _H
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94 _H		
Watch Timer	N	—	#27	FFFF90 _H	ICR08	0000B8 _H
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C _H		
A/D Converter	Y1	5	#29	FFFF88 _H	ICR09	0000B9 _H
Free-run Timer 0 / Free-run Timer 1	N	—	#30	FFFF84 _H		
Input Capture 4/5 / I ² C1	Y1	6	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C _H		
Input Capture 0 to 3	Y1	8	#33	FFFF78 _H	ICR11	0000BB _H
Output Compare 2/3/6/7	Y1	9	#34	FFFF74 _H		
UART 0 RX	Y2	10	#35	FFFF70 _H	ICR12	0000BC _H
UART 0 TX	Y1	11	#36	FFFF6C _H		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68 _H	ICR13	0000BD _H
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64 _H		

(Continued)

(Continued)

Interrupt cause	EI ² OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX / UART 4 RX	Y2	14	#39	FFFF60 _H	ICR14	0000BE _H
UART 2 TX / UART 4 TX	Y1	15	#40	FFFF5C _H		
Flash Memory	N	—	#41	FFFF58 _H	ICR15	0000BF _H
Delayed Interrupt	N	—	#42	FFFF54 _H		

Y1 : Usable

Y2 : Usable, with EI²OS stop function

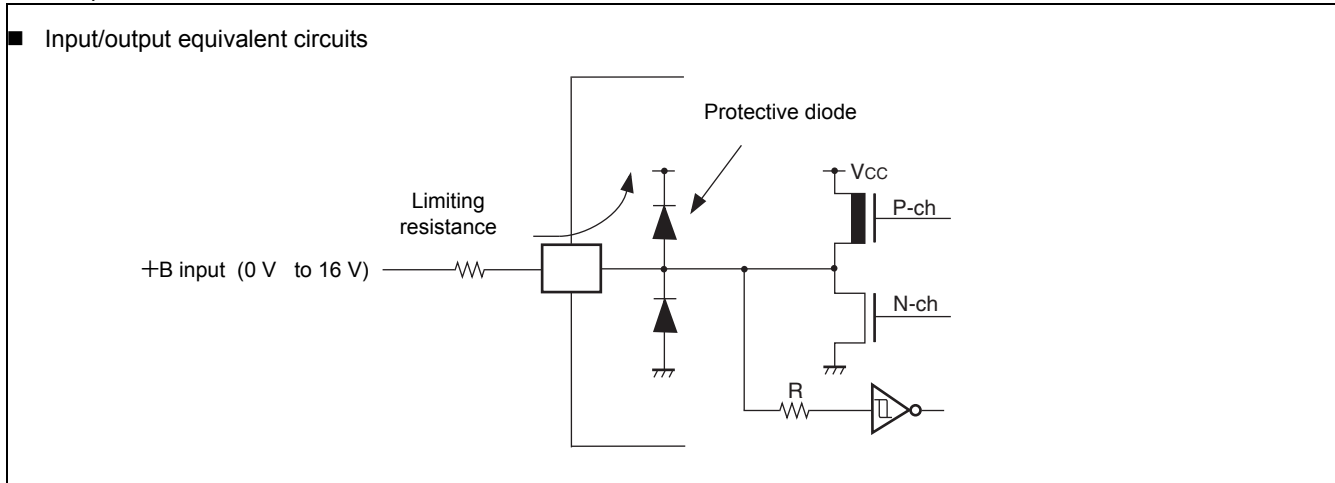
N : Unusable

Note:

- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
- When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

(Continued)

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:



*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

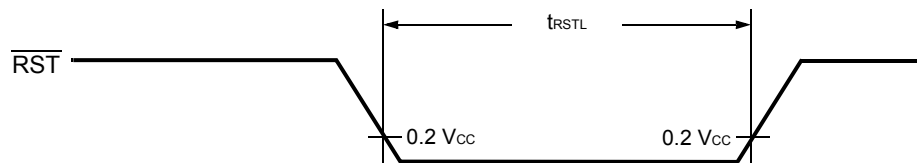
11.4.2 Reset Standby Input

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

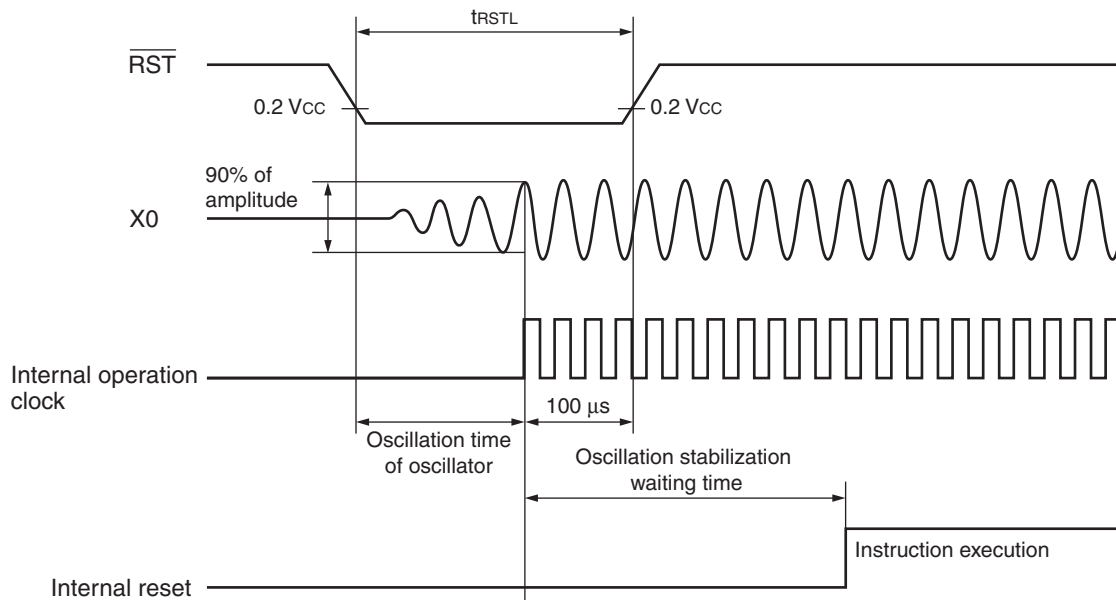
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{\text{RST}}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 μs	—	μs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	μs	In Time Timer mode

* : The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred μs and several ms, and for an external clock, the time is 0 ms.

● Under normal operation:



● In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:



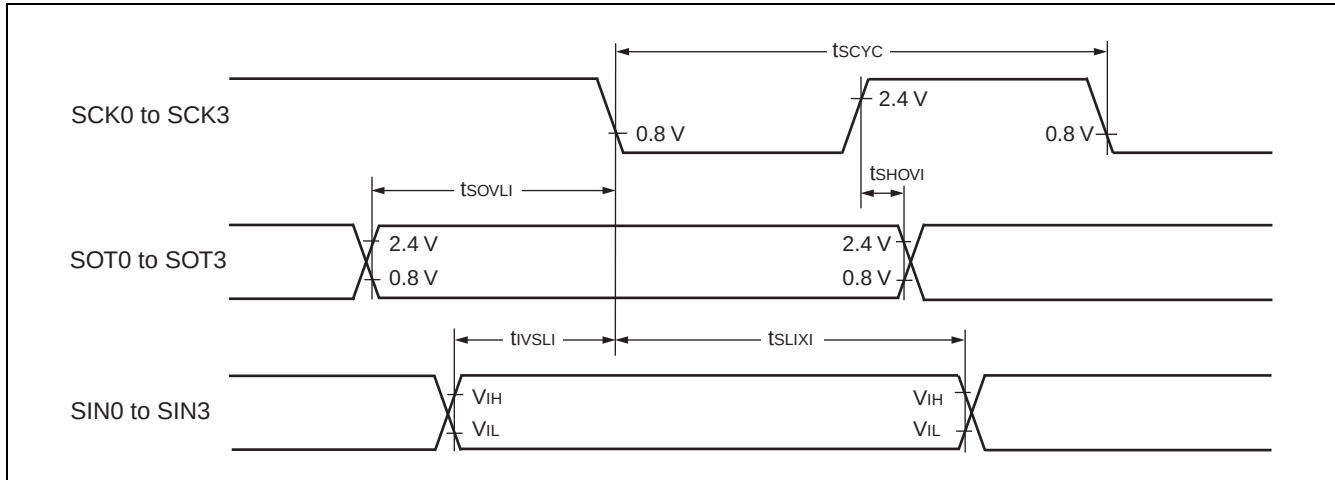
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	t_{SOVLI}	SCK0 to SCK3, SOT0 to SOT3		$3 t_{CP} - 70$	—	ns

Note:

- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.



11.5 A/D Converter

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$, $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = \text{AV}_{SS} = 0\text{ V}$)

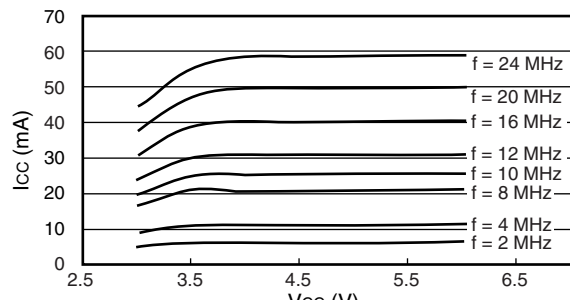
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential nonlinearity error	—	—	—	—	± 1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	$\text{AVRL} - 1.5 \times \text{LSB}$	$\text{AVRL} + 0.5 \times \text{LSB}$	$\text{AVRL} + 2.5 \times \text{LSB}$	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	$\text{AVRH} - 3.5 \times \text{LSB}$	$\text{AVRH} - 1.5 \times \text{LSB}$	$\text{AVRH} + 0.5 \times \text{LSB}$	V	
Compare time	—	—	1.0	—	16500	μs	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			2.0				$4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Sampling time	—	—	0.5	—	∞	μs	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			1.2				$4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Analog port input current	I_{AIN}	AN0 to AN23	-0.3	—	+0.3	μA	
Analog input voltage range	V_{AIN}	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$\text{AVRL} + 2.7$	—	AV_{CC}	V	
	—	AVRL	0	—	$\text{AVRH} - 2.7$	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage current	I_R	AVRH	—	600	900	μA	
	I_{RH}	AVRH	—	—	5	μA	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

*: If the A/D convertor is not operating, a current when CPU is stopped is applicable ($V_{CC} = \text{AV}_{CC} = \text{AVRH} = 5.0\text{ V}$).

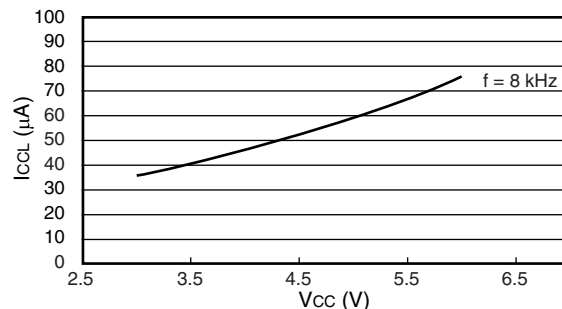
Note: : The accuracy gets worse as $|\text{AVRH} - \text{AVRL}|$ becomes smaller.

■ MB90F345E, MB90F345ES, MB90F345CE, MB90F345CES

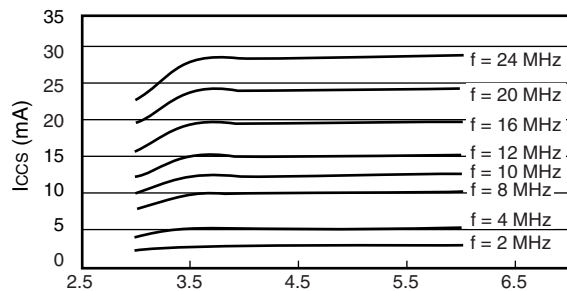
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



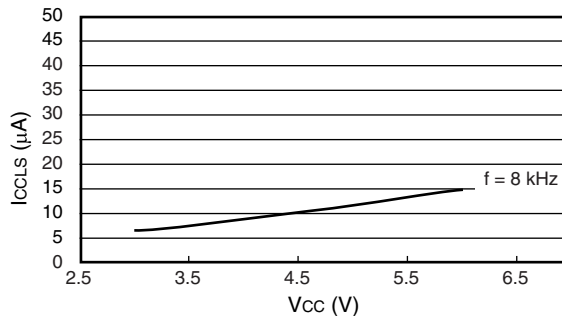
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



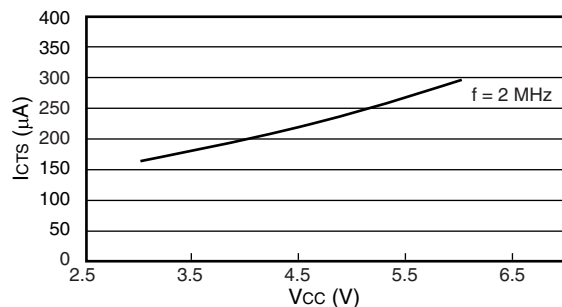
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



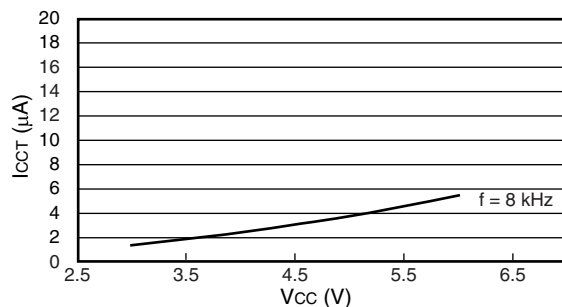
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



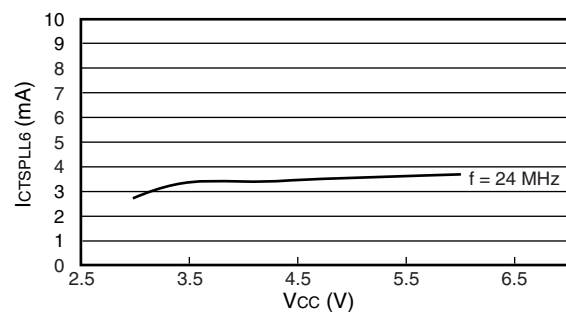
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



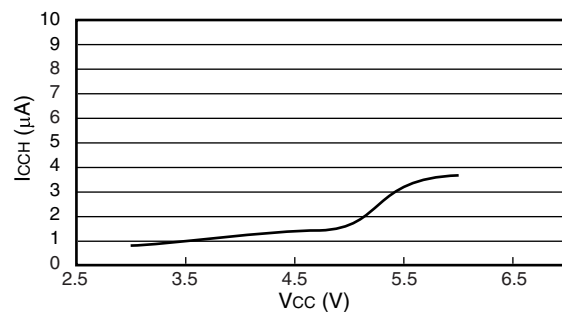
$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



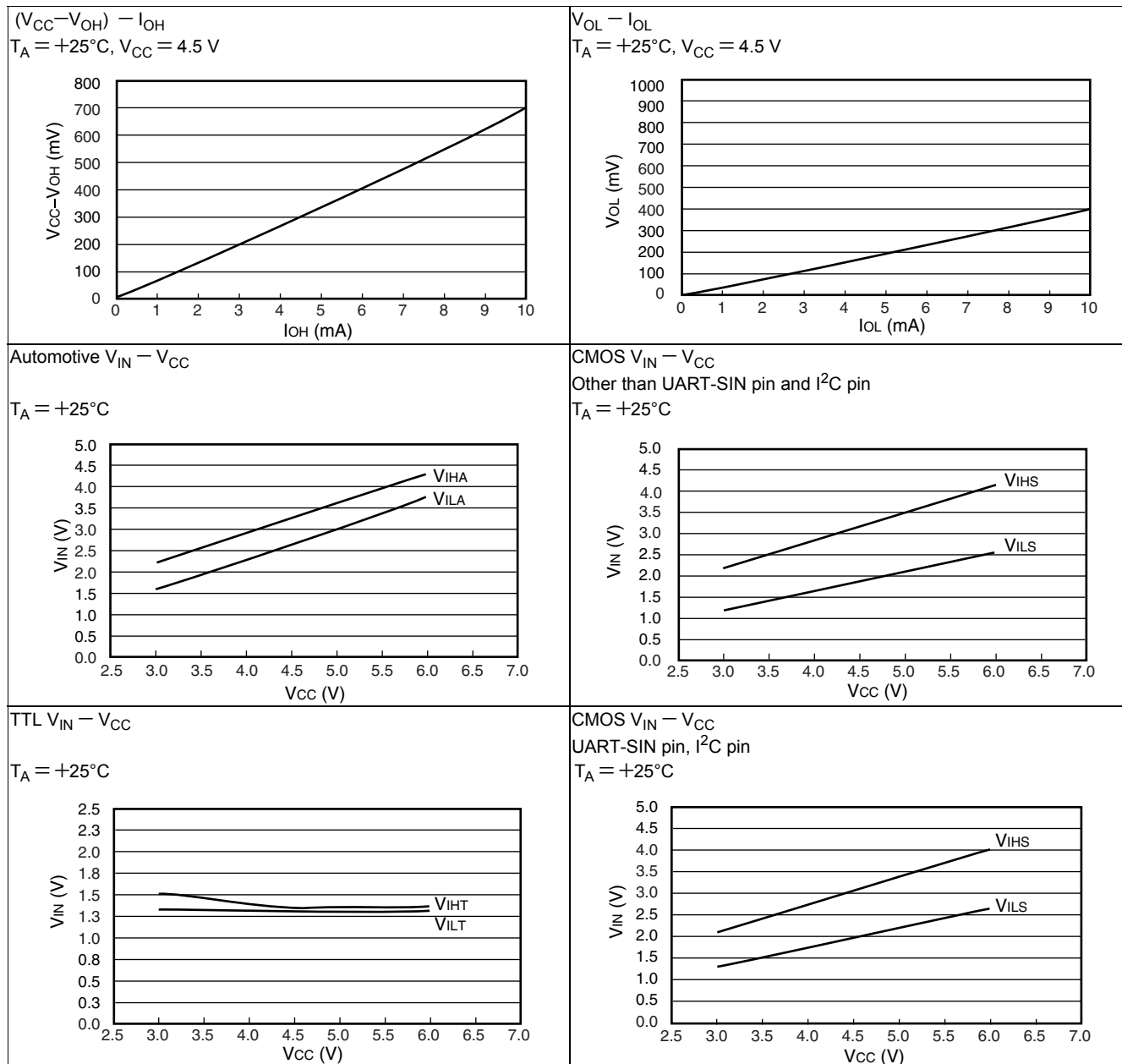
$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped



■ I/O characteristics



15. Major Changes

Spanision Publication Number: DS07-13747-4E

Page	Section	Change Results
—	—	Deleted the part numbers; MB90F343E(S), MB90F343CE(S)
51	Electrical Characteristics Absolute Maximum Ratings	Added “*6” in remark for “L” level maximum output current and “H” level maximum output current. Added “*7” in remark for “L” level average output current and “H” level average output current. Added “*8” in remark for “L” level average overall output current and “H” level average overall output current.
52		Added as follows. “*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.” “*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.” “*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.”

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90340E Series F2MC-16LX 16-bit Microcontroller Datasheet Document Number: 002-04498				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	08/23/2010	Migrated to Cypress and assigned document number 002-04498. No change to document contents or format.
*A	5221535	AKIH	05/04/2016	Updated to Cypress template