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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f342espmc-gse1

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Part Number Parameter	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
External Interrupt (16 channels)	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded intelligent I/O services (EI ² OS) and DMA		
D/A Converter	2 channels	—	
Sub clock (maximum 100 kHz)	Only for MB90V340E-102	Devices with sub clock : devices without an S suffix in the part number Devices without sub clock : devices with an S suffix in the part number	
I/O Ports	Virtually all external pins can be used as general purpose I/O port All ports are push-pull outputs Bit-wise settable as input/output or peripheral signal Can be configured 8 as CMOS schmitt trigger/ automotive inputs (in blocks of 8 pins) TTL input level settable for external bus (32-pin only for external bus)		
Flash Memory	—	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10000 cycles Data retention time : 20 years Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (except for MB90F346E(S) and MB90F346CE (S))	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01-E) is used.
Please refer to the Emulator operation manual for details.

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
9	7	P34	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare.
10	8	P35	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{\text{HAK}}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare.
11	9	P36	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		External ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare.
12	10	P37	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare
13, 14	11, 12	P40, P41	F	General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101)
		X0A, X1A	B	Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102)
15	13	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
16	14	V _{SS}	—	GND pin
17	15	C	K	This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 μF .
18	16	P42	F	General purpose I/O pin.
		IN6		Trigger input pin for input capture.
		RX1		RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only)
		INT9R		External interrupt request input pin

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV _{CC}	K	Analog power input pin for the A/D Converter

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
86	84	P11	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer
87	85	P12	N	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin
88	86	P13	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
89	87	P14	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3
90	88	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
91	89	V _{SS}	—	GND pin
92	90	X1	A	Main clock output pin
93	91	X0		Main clock input pin
94	92	P15	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
95	93	P16	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.

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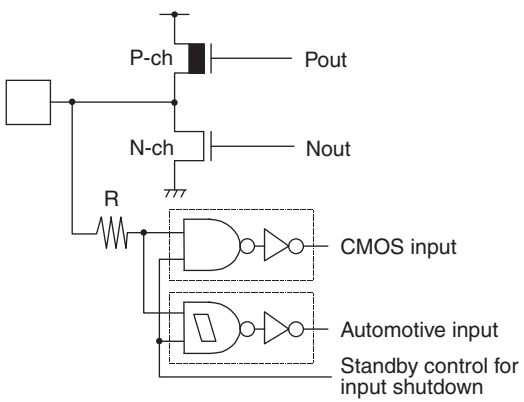
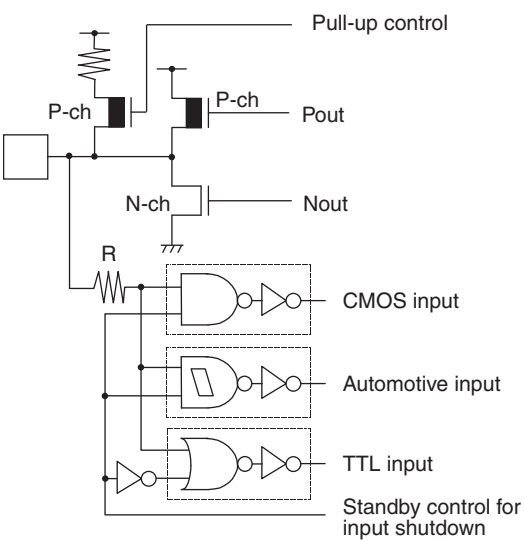
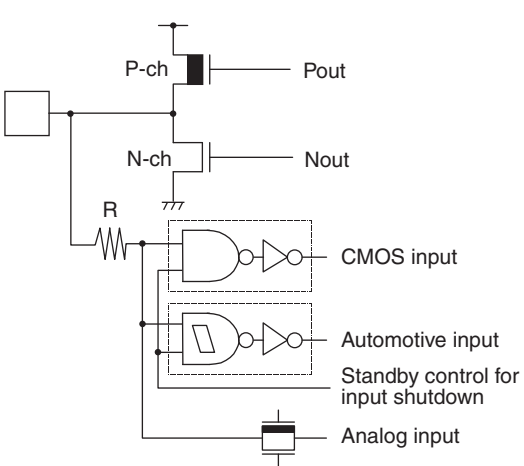
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
96	94	P17	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
97 to 100	95 to 98	P20 to P23	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		Output pins of the external address bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9, PPGB, PP GD, PPGF		Output pins for PPGs

1 : FPT-100P-M06

2 : FPT-100P-M20

3 : For I/O circuit type, refer to "I/O Circuit Type".

(Continued)

Type	Circuit	Remarks
M		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
N		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) Programmable pull-up resistor: 50 kΩ approx
O		■ CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input

MB90342E(S)/342CE(S)
 MB90F342E(S)/F342CE(S)
 MB90349E(S)/349CE(S)
 MB90F349E(S)/F349CE(S)

MB90341E(S)/341CE(S)
 MB90348E(S)/348CE(S)

MB90347E(S)/347CE(S)
 MB90F347E(S)/F347CE(S)

MB90346E(S)/346CE(S)
 MB90F346E(S)/F346CE(S)

000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral	000000H 0000EFH	Peripheral
	External access area		External access area		External access area		External access area
000100H		000100H		000100H	RAM 6 Kbytes	000100H	RAM 2 Kbytes
	RAM 16 Kbytes		RAM 16 Kbytes	0018FFH		0008FFH	
003FFFH		003FFFH					
007900H		007900H		007900H		007900H	
007FFFH	Peripheral	007FFFH	Peripheral	007FFFH	Peripheral	007FFFH	Peripheral
008000H		008000H		008000H		008000H	
00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)	00FFFFH	ROM (image of FF bank)
	External access area		External access area		External access area		External access area
FC0000H							
FCFFFFH	ROM (FC bank)						
FD0000H							
FDFFFFH	ROM (FD bank)						
FE0000H		FE0000H		FE0000H		FE0000H	
FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	ROM (FE bank)	FEFFFFH	
FF0000H		FF0000H		FF0000H		FF0000H	
FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)	FFFFFFH	ROM (FF bank)

 : Not accessible

Note: :An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.

For example, when the address 00C000_H is accessed, the data at FFC000_H in ROM is actually accessed. The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00. As a result, the image between FF8000_H and FFFFFFF_H is visible in bank 00, while the image between FF0000_H and FF7FFF_H is visible only in bank FF.

Address	Register	Abbreviation	Access	Resource name	Initial value
0000A5 _H	Automatic Ready Function Select Register	ARSR	W	External Memory Access	0011XX00 _B
0000A6 _H	External Address Output Control Register	HACR	W		00000000 _B
0000A7 _H	Bus Control Signal Selection Register	ECSR	W		0000000X _B
0000A8 _H	Watchdog Control Register	WDTN	R,W	Watchdog Timer	XXXXXX11 _B
0000A9 _H	Time Base Timer Control Register	TBTC	W,R/W	Time Base Timer	1XX00100 _B
0000AA _H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 _B
0000AB _H	Reserved				
0000AC _H	DMA Enable L Register	DERL	R/W	DMA	00000000 _B
0000AD _H	DMA Enable H Register	DERH	R/W		00000000 _B
0000AE _H	Flash Control Status Register (Flash memory devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000 _B
0000AF _H	Reserved				
0000B0 _H	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111 _B
0000B1 _H	Interrupt Control Register 01	ICR01	W,R/W		00000111 _B
0000B2 _H	Interrupt Control Register 02	ICR02	W,R/W		00000111 _B
0000B3 _H	Interrupt Control Register 03	ICR03	W,R/W		00000111 _B
0000B4 _H	Interrupt Control Register 04	ICR04	W,R/W		00000111 _B
0000B5 _H	Interrupt Control Register 05	ICR05	W,R/W		00000111 _B
0000B6 _H	Interrupt Control Register 06	ICR06	W,R/W		00000111 _B
0000B7 _H	Interrupt Control Register 07	ICR07	W,R/W		00000111 _B
0000B8 _H	Interrupt Control Register 08	ICR08	W,R/W		00000111 _B
0000B9 _H	Interrupt Control Register 09	ICR09	W,R/W		00000111 _B
0000BA _H	Interrupt Control Register 10	ICR10	W,R/W		00000111 _B
0000BB _H	Interrupt Control Register 11	ICR11	W,R/W		00000111 _B
0000BC _H	Interrupt Control Register 12	ICR12	W,R/W		00000111 _B
0000BD _H	Interrupt Control Register 13	ICR13	W,R/W		00000111 _B
0000BE _H	Interrupt Control Register 14	ICR14	W,R/W		00000111 _B
0000BF _H	Interrupt Control Register 15	ICR15	W,R/W		00000111 _B
0000C0 _H	D/A Converter Data 0	DAT0	R/W	D/A Converter	XXXXXXXX _B
0000C1 _H	D/A Converter Data 1	DAT1	R/W		XXXXXXXX _B
0000C2 _H	D/A Control 0	DACR0	R/W		XXXXXXXX0 _B
0000C3 _H	D/A Control 1	DACR1	R/W		XXXXXXXX0 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007924 _H	Input Capture 2	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
007925 _H	Input Capture 2	IPCP2	R		XXXXXXXX _B
007926 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007927 _H	Input Capture 3	IPCP3	R		XXXXXXXX _B
007928 _H	Input Capture 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
007929 _H	Input Capture 4	IPCP4	R		XXXXXXXX _B
00792A _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
00792B _H	Input Capture 5	IPCP5	R		XXXXXXXX _B
00792C _H	Input Capture 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
00792D _H	Input Capture 6	IPCP6	R		XXXXXXXX _B
00792E _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
00792F _H	Input Capture 7	IPCP7	R		XXXXXXXX _B
007930 _H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
007931 _H	Output Compare 0	OCCP0	R/W		XXXXXXXX _B
007932 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007933 _H	Output Compare 1	OCCP1	R/W		XXXXXXXX _B
007934 _H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	XXXXXXXX _B
007935 _H	Output Compare 2	OCCP2	R/W		XXXXXXXX _B
007936 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007937 _H	Output Compare 3	OCCP3	R/W		XXXXXXXX _B
007938 _H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX _B
007939 _H	Output Compare 4	OCCP4	R/W		XXXXXXXX _B
00793A _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793B _H	Output Compare 5	OCCP5	R/W		XXXXXXXX _B
00793C _H	Output Compare 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX _B
00793D _H	Output Compare 6	OCCP6	R/W		XXXXXXXX _B
00793E _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
00793F _H	Output Compare 7	OCCP7	R/W		XXXXXXXX _B
007940 _H	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000 _B
007941 _H	Timer Data 0	TCDT0	R/W		00000000 _B
007942 _H	Timer Control Status 0	TCCSL0	R/W		00000000 _B
007943 _H	Timer Control Status 0	TCCSH0	R/W		0XXXXXXXX _B
007944 _H	Timer Data 1	TCDT1	R/W	Free-run Timer 1	00000000 _B
007945 _H	Timer Data 1	TCDT1	R/W		00000000 _B
007946 _H	Timer Control Status 1	TCCSL1	R/W		00000000 _B
007947 _H	Timer Control Status 1	TCCSH1	R/W		0XXXXXXXX _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007948 _H	Timer 0/Reload 0	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX _B
007949 _H			R/W		XXXXXXXX _B
00794A _H	Timer 1/Reload 1	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX _B
00794B _H			R/W		XXXXXXXX _B
00794C _H	Timer 2/Reload 2	TMR2/TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX _B
00794D _H			R/W		XXXXXXXX _B
00794E _H	Timer 3/Reload 3	TMR3/TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX _B
00794F _H			R/W		XXXXXXXX _B
007950 _H	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000 _B
007951 _H	Serial Control Register 3	SCR3	W,R/W		00000000 _B
007952 _H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000 _B
007953 _H	Serial Status Register 3	SSR3	R,R/W		00001000 _B
007954 _H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XX _B
007955 _H	Extended Status Control Register	ESCR3	R/W		00000100 _B
007956 _H	Baud Rate Generator Register 30	BGR30	R/W		00000000 _B
007957 _H	Baud Rate Generator Register 31	BGR31	R/W		00000000 _B
007958 _H	Serial Mode Register 4	SMR4	W,R/W	UART4	00000000 _B
007959 _H	Serial Control Register 4	SCR4	W,R/W		00000000 _B
00795A _H	Reception/Transmission Data Register 4	RDR4/TDR4	R/W		00000000 _B
00795B _H	Serial Status Register 4	SSR4	R,R/W		00001000 _B
00795C _H	Extended Communication Control Register 4	ECCR4	R,W, R/W		000000XX _B
00795D _H	Extended Status Control Register	ESCR4	R/W		00000100 _B
00795E _H	Baud Rate Generator Register 40	BGR40	R/W		00000000 _B
00795F _H	Baud Rate Generator Register 41	BGR41	R/W		00000000 _B
007960 _H to 00796B _H	Reserved				
00796C _H	Clock Output Enable Register	CLKR	R/W	Clock Monitor	XXXX0000 _B
00796D _H	Reserved				
00796E _H	CAN Direct Mode Register	CDMR	R/W	CAN Clock sync	XXXXXXX0 _B
00796F _H	CAN Switch Register	CANSWR	R/W	CAN 0/1	XXXXXXX0 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007970 _H	I ² C Bus Status Register 0	IBSR0	R	I ² C Interface 0	00000000 _B
007971 _H	I ² C Bus Control Register 0	IBCR0	W,R/W		00000000 _B
007972 _H	I ² C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000 _B
007973 _H		ITBAH0	R/W		00000000 _B
007974 _H	I ² C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111 _B
007975 _H		ITMKH0	R/W		00111111 _B
007976 _H	I ² C 7-bit Slave Address Register 0	ISBA0	R/W		00000000 _B
007977 _H	I ² C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111 _B
007978 _H	I ² C Data Register 0	IDAR0	R/W		00000000 _B
007979 _H , 00797A _H	Reserved				
00797B _H	I ² C Clock Control Register 0	ICCR0	R/W	I ² C Interface 0	00011111 _B
00797C _H to 00797F _H	Reserved				
007980 _H	I ² C Bus Status Register 1	IBSR1	R	I ² C Interface 1	00000000 _B
007981 _H	I ² C Bus Control Register 1	IBCR1	W,R/W		00000000 _B
007982 _H	I ² C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000 _B
007983 _H		ITBAH1	R/W		00000000 _B
007984 _H	I ² C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111 _B
007985 _H		ITMKH1	R/W		00111111 _B
007986 _H	I ² C 7-bit Slave Address Register 1	ISBA1	R/W		00000000 _B
007987 _H	I ² C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111 _B
007988 _H	I ² C Data Register 1	IDAR1	R/W		00000000 _B
007989 _H , 00798A _H	Reserved				
00798B _H	I ² C Clock Control Register 1	ICCR1	R/W	I ² C Interface 1	00011111 _B
00798C _H to 0079C1 _H	Reserved				
0079C2 _H	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	0001X000 _B
0079C3 _H to 0079DF _H	Reserved				

(Continued)

9. CAN Controllers

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
- Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
- 29-bit ID and 8-byte data
- Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
- Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070 _H	000080 _H	Message Buffer Valid Register	BVALR	R/W	00000000 _B 00000000 _B
000071 _H	000081 _H				
000072 _H	000082 _H	Transmit Request Register	TREQR	R/W	00000000 _B 00000000 _B
000073 _H	000083 _H				
000074 _H	000084 _H	Transmit Cancel Register	TCANR	W	00000000 _B 00000000 _B
000075 _H	000085 _H				
000076 _H	000086 _H	Transmission Complete Register	TCR	R/W	00000000 _B 00000000 _B
000077 _H	000087 _H				
000078 _H	000088 _H	Receive Complete Register	RCR	R/W	00000000 _B 00000000 _B
000079 _H	000089 _H				
00007A _H	00008A _H	Remote Request Receiving Register	RRTRR	R/W	00000000 _B 00000000 _B
00007B _H	00008B _H				
00007C _H	00008C _H	Receive Overrun Register	ROVRR	R/W	00000000 _B 00000000 _B
00007D _H	00008D _H				
00007E _H	00008E _H	Reception Interrupt Enable Register	RIER	R/W	00000000 _B 00000000 _B
00007F _H	00008F _H				

10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI ² OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC _H	—	—
INT9 instruction	N	—	#09	FFFFD8 _H	—	—
Exception	N	—	#10	FFFFD4 _H	—	—
CAN 0 RX	N	—	#11	FFFFD0 _H	ICR00	0000B0 _H
CAN 0 TX/NS	N	—	#12	FFFFCC _H		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4 _H		
CAN 2 RX / I ² C0	N	—	#15	FFFFC0 _H	ICR02	0000B2 _H
CAN 2 TX/NS	N	—	#16	FFFFBC _H		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8 _H	ICR03	0000B3 _H
16-bit Reload Timer 1	Y1	1	#18	FFFFB4 _H		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0 _H	ICR04	0000B4 _H
16-bit Reload Timer 3	Y1	—	#20	FFFFAC _H		
PPG 0/1/4/5	N	—	#21	FFFFA8 _H	ICR05	0000B5 _H
PPG 2/3/6/7	N	—	#22	FFFFA4 _H		
PPG 8/9/C/D	N	—	#23	FFFFA0 _H	ICR06	0000B6 _H
PPG A/B/E/F	N	—	#24	FFFF9C _H		
Time Base Timer	N	—	#25	FFFF98 _H	ICR07	0000B7 _H
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94 _H		
Watch Timer	N	—	#27	FFFF90 _H	ICR08	0000B8 _H
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C _H		
A/D Converter	Y1	5	#29	FFFF88 _H	ICR09	0000B9 _H
Free-run Timer 0 / Free-run Timer 1	N	—	#30	FFFF84 _H		
Input Capture 4/5 / I ² C1	Y1	6	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C _H		
Input Capture 0 to 3	Y1	8	#33	FFFF78 _H	ICR11	0000BB _H
Output Compare 2/3/6/7	Y1	9	#34	FFFF74 _H		
UART 0 RX	Y2	10	#35	FFFF70 _H	ICR12	0000BC _H
UART 0 TX	Y1	11	#36	FFFF6C _H		
UART 1 RX / UART 3 RX	Y2	12	#37	FFFF68 _H	ICR13	0000BD _H
UART 1 TX / UART 3 TX	Y1	13	#38	FFFF64 _H		

(Continued)

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *2
	$AVRH, AVRL$	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH, AV_{CC} \geq AVRL, AVRH \geq AVRL$
Input voltage*1	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\sum I_{CLAMP} $	—	40	mA	*5
"L" level maximum output current	I_{OL}	—	15	mA	*4, *6
"L" level average output current	I_{OLAV}	—	4	mA	*4, *7
"L" level maximum overall output current	$\sum I_{OL}$	—	100	mA	*4
"L" level average overall output current	$\sum I_{OLAV}$	—	50	mA	*4, *8
"H" level maximum output current	I_{OH}	—	-15	mA	*4, *6
"H" level average output current	I_{OHAV}	—	-4	mA	*4, *7
"H" level maximum overall output current	$\sum I_{OH}$	—	-100	mA	*4
"H" level average overall output current	$\sum I_{OHAV}$	—	-50	mA	*4, *8
Power consumption	P_D	—	450	mW	
Operating temperature	T_A	-40	+105	°C	
Storage temperature	T_{STG}	-55	+150	°C	

*1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V

*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed $V_{CC} + 0.3$ V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, PA1

*5: • Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57 (Evaluation device : P50 to P55), P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1

• Use within recommended operating conditions.

• Use with DC voltage (current)

• The +B signal should always be applied by using a limiting resistance placed between the +B signal and the microcontroller.

• The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed the rated value, either instantaneously or for prolonged periods.

• Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.

(Continued)

11.3 DC Characteristics
 $(T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, f_{CP} \leq 24\text{ MHz}, V_{SS} = AV_{SS} = 0\text{ V})$

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{IHS}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{IHA}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected
	V_{IHS}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHI}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{ILA}	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if Automotive input levels are selected
	V_{ILT}	—	—	$V_{SS} - 0.3$	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILI}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	$V_{CC} = 4.5\text{ V}, I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	V_{OHI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}, I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	V_{OL}	Normal outputs	$V_{CC} = 4.5\text{ V}, I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Output L voltage	V_{OLI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}, I_{OL} = 3.0\text{ mA}$	—	—	0.4	V	

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11.4 AC Characteristics

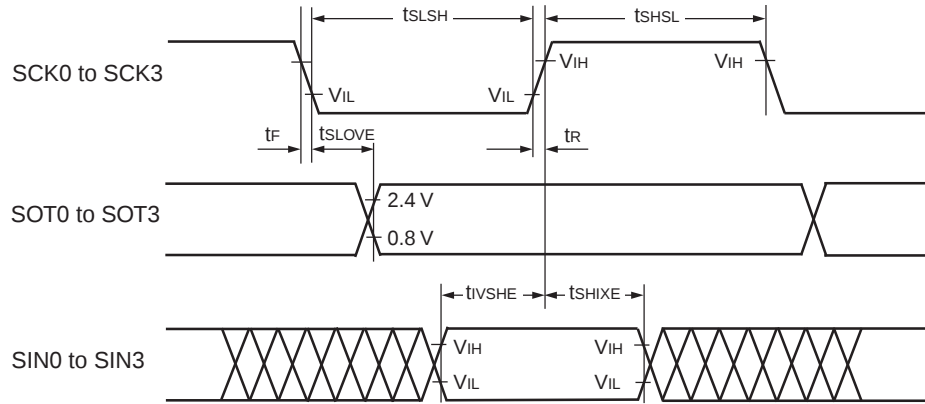
11.4.1 Clock Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	When using an oscillation circuit
			4	—	16	MHz	PLL multiplied by 1 When using an oscillation circuit
			4	—	12	MHz	PLL multiplied by 2 When using an oscillation circuit
			4	—	8	MHz	PLL multiplied by 3 When using an oscillation circuit
			4	—	6	MHz	PLL multiplied by 4 When using an oscillation circuit
			—	—	4	MHz	PLL multiplied by 6 When using an oscillation circuit
			3	—	24	MHz	When using an external clock*
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	μs	When using sub clock

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in "Relation between the external clock frequency and machine clock frequency".

• External Shift Clock Mode



■ Bit setting: ESCR:SCES = 1, ECCR:SCDE = 0

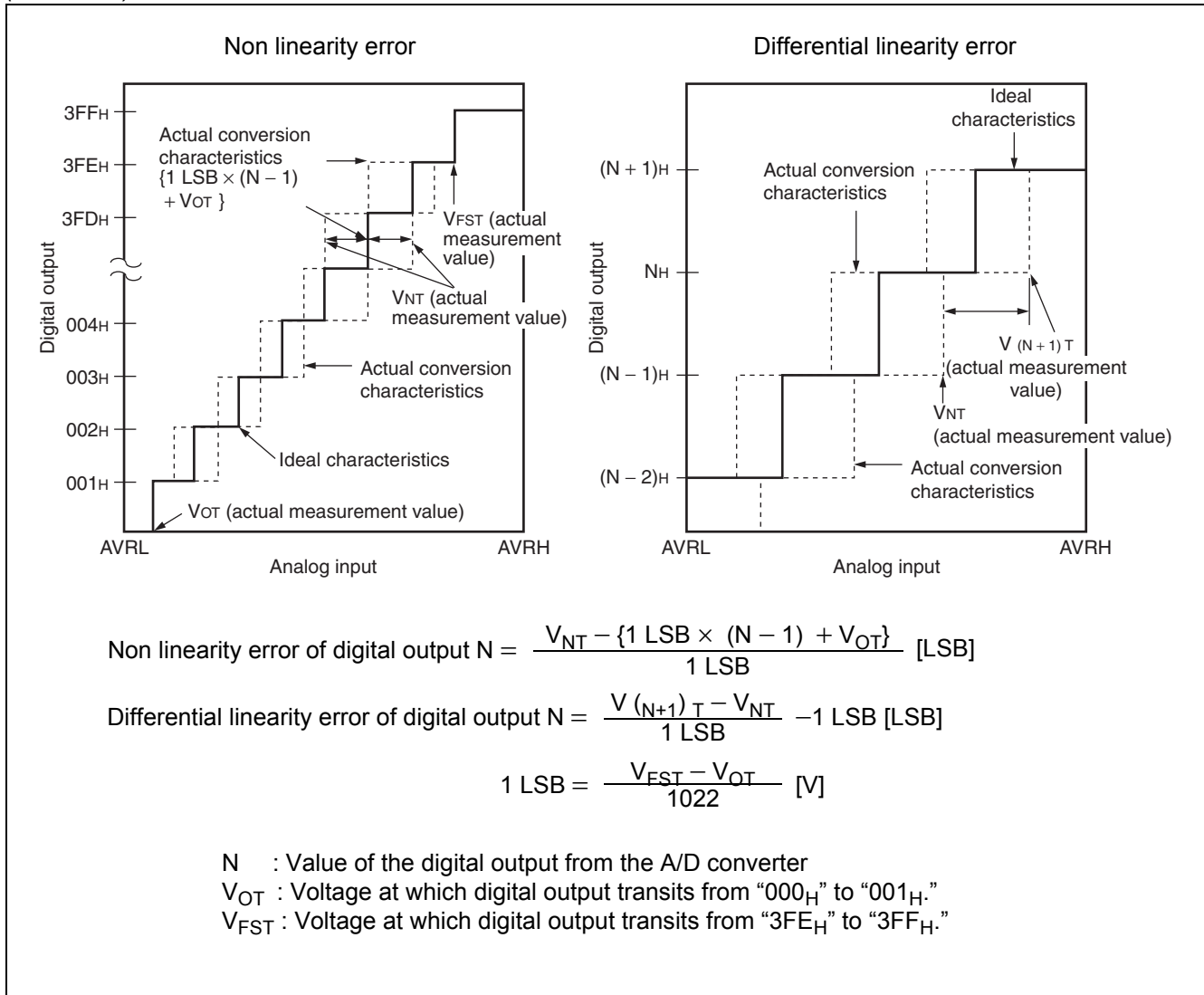
($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK $\uparrow$ → SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN → SCK $\downarrow$	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\downarrow$ → Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$3 t_{CP} - t_R$	—	ns
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK3		$t_{CP} + 10$	—	ns
SCK $\uparrow$ → SOT delay time	t_{SHOVE}	SCK0 to SCK3, SOT0 to SOT3		—	$2 t_{CP} + 60$	ns
Valid SIN → SCK $\downarrow$	t_{IVSLE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK $\downarrow$ → Valid SIN hold time	t_{SLIXE}	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 30$	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

Note:

- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".

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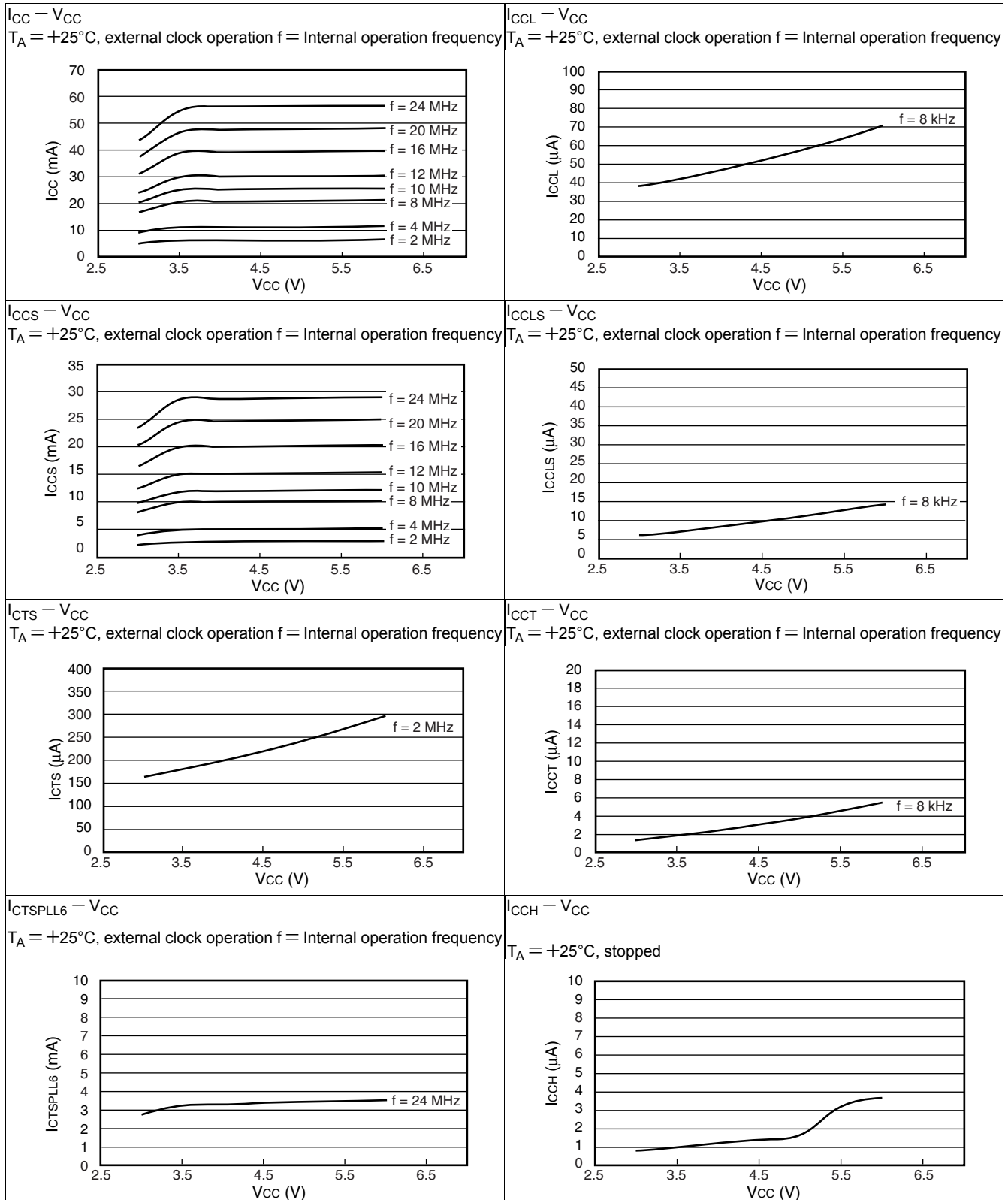
11.7 Notes on A/D Converter Section

Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower ($4.0 \text{ V} \leq AV_{CC} \leq 5.5 \text{ V}$,
sampling period = 0.5 μs)

If an external capacitor is used, in consideration of the capacitive voltage dividing effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor be several thousand times greater than the capacitance of the internal capacitor.

■ MB90F349E, MB90F349ES, MB90F349CE, MB90F349CES



Part number	Package	Remarks
MB90F347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F347ESPF		
MB90F347CEPF		
MB90F347CESPF		
MB90F347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F347ESPMC		
MB90F347CEPMC		
MB90F347CESPMC		
MB90F349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F349ESPF		
MB90F349CEPF		
MB90F349CESPF		
MB90F349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F349ESPMC		
MB90F349CEPMC		
MB90F349CESPMC		
MB90341EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90341ESPF		
MB90341CEPF		
MB90341CESPF		
MB90341EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90341ESPMC		
MB90341CEPMC		
MB90341CESPMC		
MB90342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90342ESPF		
MB90342CEPF		
MB90342CESPF		
MB90342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90342ESPMC		
MB90342CEPMC		
MB90342CESPMC		

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