# Infineon Technologies - MB90F345CESPMC-G-JNE1 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

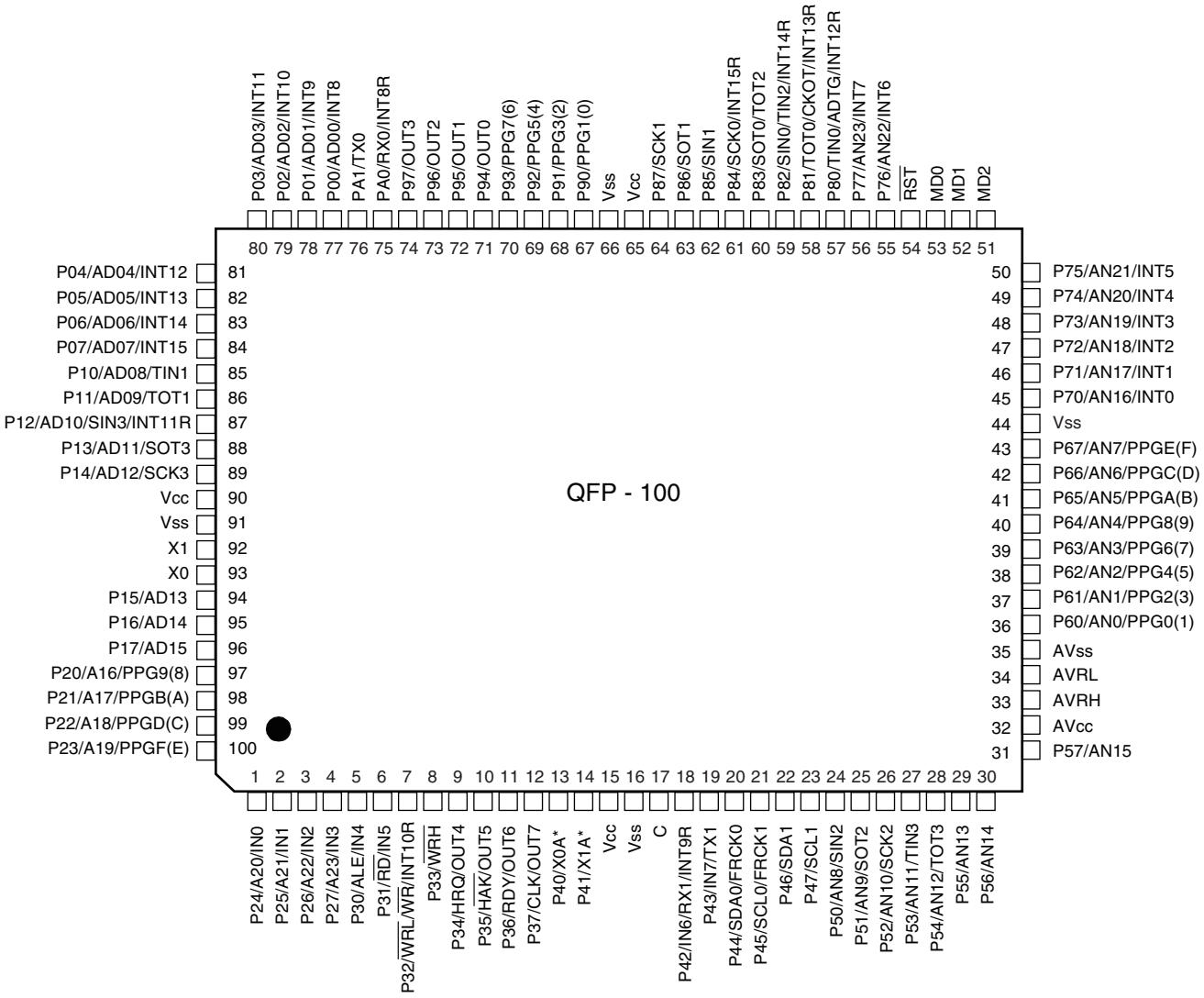
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART |
| Peripherals | DMA, POR, WDT |
| Number of I/O | 82 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 20K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 5.5V |
| Data Converters | A/D 24x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90f345cespmc-g-jne1 |

## Contents

■ MB90341CE(S), MB90342CE(S), MB90F342CE(S), MB90F345CE(S), MB90346CE(S), MB90F346CE(S), MB90347CE(S), MB90F347CE(S), MB90348CE(S), MB90349CE(S), MB90F349CE(S)

(TOP VIEW)




(FPT-100P-M06)

* : X0A, X1A : devices without an S suffix in the part number
P40, P41 : devices with an S suffix in the part number

*(Continued)*

| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 9 | 7 | P34 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled. |
| | | HRQ | | Hold request input pin. This function is enabled when both the external bus and the hold function are enabled. |
| | | OUT4 | | Waveform output pin for output compare. |
| 10 | 8 | P35 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled. |
| | | $\overline{\text{HAK}}$ | | Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled. |
| | | OUT5 | | Waveform output pin for output compare. |
| 11 | 9 | P36 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled. |
| | | RDY | | External ready input pin. This function is enabled when both the external bus and the external ready function are enabled. |
| | | OUT6 | | Waveform output pin for output compare. |
| 12 | 10 | P37 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled. |
| | | CLK | | Clock output pin. This function is enabled when both the external bus and clock output are enabled. |
| | | OUT7 | | Waveform output pin for output compare |
| 13, 14 | 11, 12 | P40, P41 | F | General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101) |
| | | X0A, X1A | B | Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102) |
| 15 | 13 | $V_{CC}$ | — | Power (3.5 V to 5.5 V) input pin |
| 16 | 14 | $V_{SS}$ | — | GND pin |
| 17 | 15 | C | K | This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 µF. |
| 18 | 16 | P42 | F | General purpose I/O pin. |
| | | IN6 | | Trigger input pin for input capture. |
| | | RX1 | | RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only) |
| | | INT9R | | External interrupt request input pin |

*(Continued)*

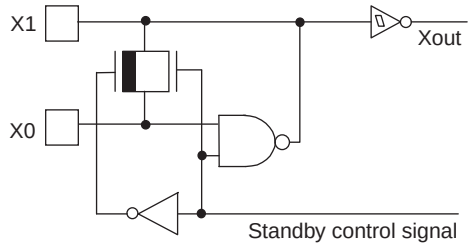
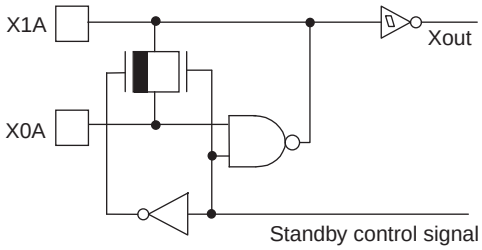
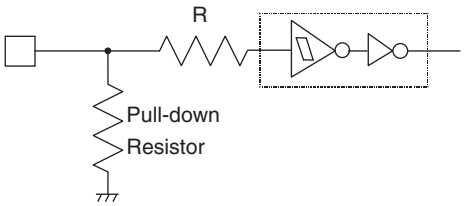
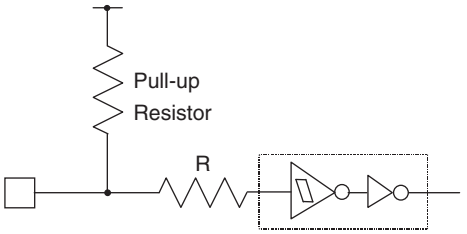
| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 19 | 17 | P43 | F | General purpose I/O pin. |
| | | IN7 | | Trigger input pin for input capture. |
| | | TX1 | | TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only) |
| 20 | 18 | P44 | H | General purpose I/O pin. |
| | | SDA0 | | Serial data I/O pin for $I^2C$ (devices with a C suffix in the part number) |
| | | FRCK0 | | Input pin for the 16-bit Free-run Timer 0 |
| 21 | 19 | P45 | H | General purpose I/O pin. |
| | | SCL0 | | Serial clock I/O pin for $I^2C$ (devices with a C suffix in the part number) |
| | | FRCK1 | | Input pin for the 16-bit Free-run Timer |
| 22 | 20 | P46 | H | General purpose I/O pin. |
| | | SDA1 | | Serial data I/O pin for $I^2C$ (devices with a C suffix in the part number) |
| 23 | 21 | P47 | H | General purpose I/O pin. |
| | | SCL1 | | Serial clock I/O pin for $I^2C$ (devices with a C suffix in the part number) |
| 24 | 22 | P50 | O | General purpose I/O pin. |
| | | AN8 | | Analog input pin for the A/D converter |
| | | SIN2 | | Serial data input pin for UART2 |
| 25 | 23 | P51 | I | General purpose I/O pin. |
| | | AN9 | | Analog input pin for the A/D converter |
| | | SOT2 | | Serial data output pin for UART2 |
| 26 | 24 | P52 | I | General purpose I/O pin. |
| | | AN10 | | Analog input pin for the A/D converter |
| | | SCK2 | | Clock I/O pin for UART2 |
| 27 | 25 | P53 | I | General purpose I/O pin. |
| | | AN11 | | Analog input pin for the A/D converter |
| | | TIN3 | | Event input pin for the reload timer |
| 28 | 26 | P54 | I | General purpose I/O pin. |
| | | AN12 | | Analog input pin for the A/D converter |
| | | TOT3 | | Output pin for the reload timer |
| 29 | 27 | P55 | I | General purpose I/O pin. |
| | | AN13 | | Analog input pin for the A/D converter |
| 30, 31 | 28, 29 | P56, P57 | J | General purpose I/O pins. |
| | | AN14, AN15 | | Analog input pins for the A/D converter |
| 32 | 30 | $AV_{CC}$ | K | Analog power input pin for the A/D Converter |

*(Continued)*

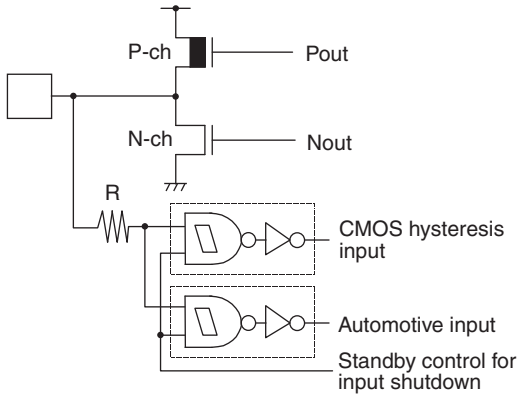
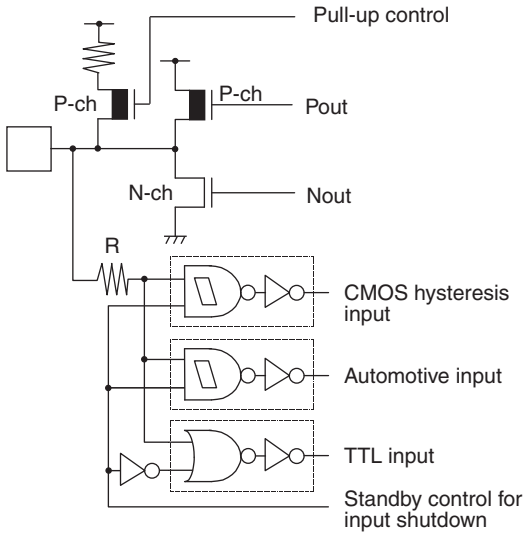
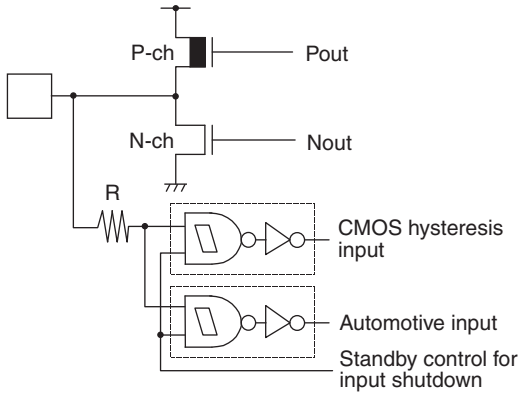
| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 33 | 31 | AVRH | L | Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to $AV_{CC}$. |
| 34 | 32 | AVRL | K | Lower reference voltage input pin for the A/D Converter |
| 35 | 33 | $AV_{SS}$ | K | Analog GND pin for the A/D Converter |
| 36 to 43 | 34 to 41 | P60 to P67 | I | General purpose I/O pins. |
| | | AN0 to AN7 | | Analog input pins for the A/D converter |
| | | PPG0, 2, 4, 6, 8, A, C, E | | Output pins for PPGs |
| 44 | 42 | $V_{SS}$ | — | GND pin |
| 45 to 50 | 43 to 48 | P70 to P75 | I | General purpose I/O pins. |
| | | AN16 to AN21 | | Analog input pins for the A/D converter (devices with a C suffix in the part number) |
| | | INT0 to INT5 | | External interrupt request input pins |
| 51 | 49 | MD2 | D | Input pin for specifying the operating mode. |
| 52, 53 | 50, 51 | MD1, MD0 | C | Input pins for specifying the operating mode. |
| 54 | 52 | $\overline{RST}$ | E | Reset input pin |
| 55, 56 | 53, 54 | P76, P77 | I | General purpose I/O pins. |
| | | AN22, AN23 | | Analog input pins for the A/D converter (devices with a C suffix in the part number) |
| | | INT6, INT7 | | External interrupt request input pins |
| 57 | 55 | P80 | F | General purpose I/O pin. |
| | | TIN0 | | Event input pin for the reload timer |
| | | ADTG | | Trigger input pin for the A/D converter |
| | | INT12R | | External interrupt request input pin |
| 58 | 56 | P81 | F | General purpose I/O pin. |
| | | TOT0 | | Output pin for the reload timer |
| | | CKOT | | Output pin for the clock monitor |
| | | INT13R | | External interrupt request input pin |
| 59 | 57 | P82 | M | General purpose I/O pin. |
| | | SIN0 | | Serial data input pin for UART0 |
| | | TIN2 | | Event input pin for the reload timer |
| | | INT14R | | External interrupt request input pin |
| 60 | 58 | P83 | F | General purpose I/O pin. |
| | | SOT0 | | Serial data output pin for UART0 |
| | | TOT2 | | Output pin for the reload timer |

*(Continued)*

## 4. I/O Circuit Type

| Type | Circuit | Remarks |
|---|---|---|
| A |  | Oscillation circuit<br>High-speed oscillation feedback resistor = approx. 1 MΩ |
| B |  | Oscillation circuit<br>Low-speed oscillation feedback resistor = approx. 10 MΩ |
| C |  | ■ MASK ROM and evaluation products: CMOS hysteresis input pin<br>■ Flash memory products: CMOS input pin |
| D |  | MASK ROM and evaluation products:<br>■ CMOS hysteresis input pin<br>■ Pull-down resistor value: approx. 50 kΩ<br>Flash memory products:<br>■ CMOS input pin<br>■ No pull-down |
| E |  | CMOS hysteresis input pin<br>Pull-up resistor value: approx. 50 kΩ |

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| F |  | ■ CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>■ CMOS hysteresis input (with function to disconnect input during standby)<br>■ Automotive input (with function to disconnect input during standby) |
| G |  | ■ CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>■ CMOS hysteresis input (with function to disconnect input during standby)<br>■ Automotive input (with function to disconnect input during standby)<br>■ TTL input (with function to disconnect input during standby)<br>■ Programmable pull-up resistor: 50 kΩ approx. |
| H |  | ■ CMOS level output ($I_{OL}$ = 3 mA, $I_{OH}$ = –3 mA)<br>■ CMOS hysteresis input (with function to disconnect input during standby)<br>■ Automotive input (with function to disconnect input during standby) |

*(Continued)*

## 5. Handling Devices

### 1. Preventing latch-up

**CMOS IC may suffer latch-up under the following conditions:**

- A voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between $V_{CC}$ and $V_{SS}$ pins.
- The $AV_{CC}$ power supply is applied before the $V_{CC}$ voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage ($AV_{CC}$, AVRH) exceed the digital power-supply voltage.

### 2. Handling unused pins

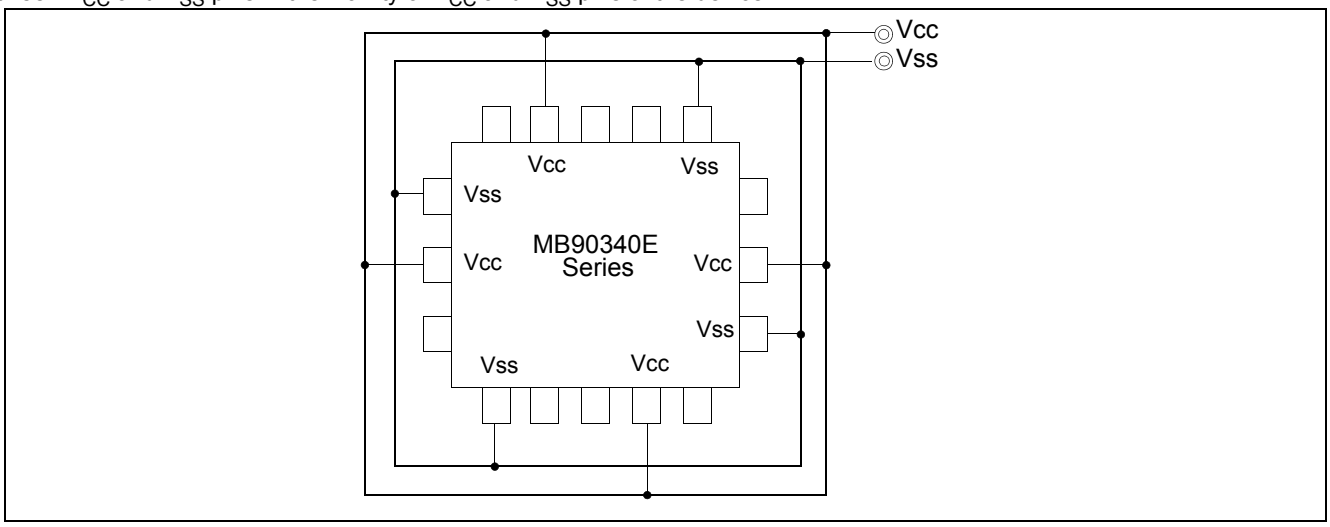
Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 kΩ or more.

### 3. Power supply pins ($V_{CC}$/$V_{SS}$)

- If there are multiple $V_{CC}$ and $V_{SS}$ pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the $V_{CC}$ and $V_{SS}$ pins to the power supply and ground externally.
Connect $V_{CC}$ and $V_{SS}$ pins to the device from the current supply source at a possibly low impedance.

- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 µF as a bypass capacitor between $V_{CC}$ and $V_{SS}$ pins in the vicinity of $V_{CC}$ and $V_{SS}$ pins of the device.




### 4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to $V_{CC}$ or $V_{SS}$ pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to $V_{CC}$ or $V_{SS}$ pins and to provide a low-impedance connection.

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $007900_H$ | Reload Register L0 | PRLL0 | R/W | 16-bit PPG 0/1 | $XXXXXXXX_B$ |
| $007901_H$ | Reload Register H0 | PRLH0 | R/W | | $XXXXXXXX_B$ |
| $007902_H$ | Reload Register L1 | PRLL1 | R/W | | $XXXXXXXX_B$ |
| $007903_H$ | Reload Register H1 | PRLH1 | R/W | | $XXXXXXXX_B$ |
| $007904_H$ | Reload Register L2 | PRLL2 | R/W | 16-bit PPG 2/3 | $XXXXXXXX_B$ |
| $007905_H$ | Reload Register H2 | PRLH2 | R/W | | $XXXXXXXX_B$ |
| $007906_H$ | Reload Register L3 | PRLL3 | R/W | | $XXXXXXXX_B$ |
| $007907_H$ | Reload Register H3 | PRLH3 | R/W | | $XXXXXXXX_B$ |
| $007908_H$ | Reload Register L4 | PRLL4 | R/W | 16-bit PPG 4/5 | $XXXXXXXX_B$ |
| $007909_H$ | Reload Register H4 | PRLH4 | R/W | | $XXXXXXXX_B$ |
| $00790A_H$ | Reload Register L5 | PRLL5 | R/W | | $XXXXXXXX_B$ |
| $00790B_H$ | Reload Register H5 | PRLH5 | R/W | | $XXXXXXXX_B$ |
| $00790C_H$ | Reload Register L6 | PRLL6 | R/W | 16-bit PPG 6/7 | $XXXXXXXX_B$ |
| $00790D_H$ | Reload Register H6 | PRLH6 | R/W | | $XXXXXXXX_B$ |
| $00790E_H$ | Reload Register L7 | PRLL7 | R/W | | $XXXXXXXX_B$ |
| $00790F_H$ | Reload Register H7 | PRLH7 | R/W | | $XXXXXXXX_B$ |
| $007910_H$ | Reload Register L8 | PRLL8 | R/W | 16-bit PPG 8/9 | $XXXXXXXX_B$ |
| $007911_H$ | Reload Register H8 | PRLH8 | R/W | | $XXXXXXXX_B$ |
| $007912_H$ | Reload Register L9 | PRLL9 | R/W | | $XXXXXXXX_B$ |
| $007913_H$ | Reload Register H9 | PRLH9 | R/W | | $XXXXXXXX_B$ |
| $007914_H$ | Reload Register LA | PRLLA | R/W | 16-bit PPG A/B | $XXXXXXXX_B$ |
| $007915_H$ | Reload Register HA | PRLHA | R/W | | $XXXXXXXX_B$ |
| $007916_H$ | Reload Register LB | PRLLB | R/W | | $XXXXXXXX_B$ |
| $007917_H$ | Reload Register HB | PRLHB | R/W | | $XXXXXXXX_B$ |
| $007918_H$ | Reload Register LC | PRLLC | R/W | 16-bit PPG C/D | $XXXXXXXX_B$ |
| $007919_H$ | Reload Register HC | PRLHC | R/W | | $XXXXXXXX_B$ |
| $00791A_H$ | Reload Register LD | PRLLD | R/W | | $XXXXXXXX_B$ |
| $00791B_H$ | Reload Register HD | PRLHD | R/W | | $XXXXXXXX_B$ |
| $00791C_H$ | Reload Register LE | PRLLE | R/W | 16-bit PPG E/F | $XXXXXXXX_B$ |
| $00791D_H$ | Reload Register HE | PRLHE | R/W | | $XXXXXXXX_B$ |
| $00791E_H$ | Reload Register LF | PRLLF | R/W | | $XXXXXXXX_B$ |
| $00791F_H$ | Reload Register HF | PRLHF | R/W | | $XXXXXXXX_B$ |
| $007920_H$ | Input Capture 0 | IPCP0 | R | Input Capture 0/1 | $XXXXXXXX_B$ |
| $007921_H$ | Input Capture 0 | IPCP0 | R | | $XXXXXXXX_B$ |
| $007922_H$ | Input Capture 1 | IPCP1 | R | | $XXXXXXXX_B$ |
| $007923_H$ | Input Capture 1 | IPCP1 | R | | $XXXXXXXX_B$ |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $007924_H$ | Input Capture 2 | IPCP2 | R | Input Capture 2/3 | $XXXXXXXX_B$ |
| $007925_H$ | Input Capture 2 | IPCP2 | R | | $XXXXXXXX_B$ |
| $007926_H$ | Input Capture 3 | IPCP3 | R | | $XXXXXXXX_B$ |
| $007927_H$ | Input Capture 3 | IPCP3 | R | | $XXXXXXXX_B$ |
| $007928_H$ | Input Capture 4 | IPCP4 | R | Input Capture 4/5 | $XXXXXXXX_B$ |
| $007929_H$ | Input Capture 4 | IPCP4 | R | | $XXXXXXXX_B$ |
| $00792A_H$ | Input Capture 5 | IPCP5 | R | | $XXXXXXXX_B$ |
| $00792B_H$ | Input Capture 5 | IPCP5 | R | | $XXXXXXXX_B$ |
| $00792C_H$ | Input Capture 6 | IPCP6 | R | Input Capture 6/7 | $XXXXXXXX_B$ |
| $00792D_H$ | Input Capture 6 | IPCP6 | R | | $XXXXXXXX_B$ |
| $00792E_H$ | Input Capture 7 | IPCP7 | R | | $XXXXXXXX_B$ |
| $00792F_H$ | Input Capture 7 | IPCP7 | R | | $XXXXXXXX_B$ |
| $007930_H$ | Output Compare 0 | OCCP0 | R/W | Output Compare 0/1 | $XXXXXXXX_B$ |
| $007931_H$ | Output Compare 0 | OCCP0 | R/W | | $XXXXXXXX_B$ |
| $007932_H$ | Output Compare 1 | OCCP1 | R/W | | $XXXXXXXX_B$ |
| $007933_H$ | Output Compare 1 | OCCP1 | R/W | | $XXXXXXXX_B$ |
| $007934_H$ | Output Compare 2 | OCCP2 | R/W | Output Compare 2/3 | $XXXXXXXX_B$ |
| $007935_H$ | Output Compare 2 | OCCP2 | R/W | | $XXXXXXXX_B$ |
| $007936_H$ | Output Compare 3 | OCCP3 | R/W | | $XXXXXXXX_B$ |
| $007937_H$ | Output Compare 3 | OCCP3 | R/W | | $XXXXXXXX_B$ |
| $007938_H$ | Output Compare 4 | OCCP4 | R/W | Output Compare 4/5 | $XXXXXXXX_B$ |
| $007939_H$ | Output Compare 4 | OCCP4 | R/W | | $XXXXXXXX_B$ |
| $00793A_H$ | Output Compare 5 | OCCP5 | R/W | | $XXXXXXXX_B$ |
| $00793B_H$ | Output Compare 5 | OCCP5 | R/W | | $XXXXXXXX_B$ |
| $00793C_H$ | Output Compare 6 | OCCP6 | R/W | Output Compare 6/7 | $XXXXXXXX_B$ |
| $00793D_H$ | Output Compare 6 | OCCP6 | R/W | | $XXXXXXXX_B$ |
| $00793E_H$ | Output Compare 7 | OCCP7 | R/W | | $XXXXXXXX_B$ |
| $00793F_H$ | Output Compare 7 | OCCP7 | R/W | | $XXXXXXXX_B$ |
| $007940_H$ | Timer Data 0 | TCDT0 | R/W | Free-run Timer 0 | $00000000_B$ |
| $007941_H$ | Timer Data 0 | TCDT0 | R/W | | $00000000_B$ |
| $007942_H$ | Timer Control Status 0 | TCCSL0 | R/W | | $00000000_B$ |
| $007943_H$ | Timer Control Status 0 | TCCSH0 | R/W | | $0XXXXXXX_B$ |
| $007944_H$ | Timer Data 1 | TCDT1 | R/W | Free-run Timer 1 | $00000000_B$ |
| $007945_H$ | Timer Data 1 | TCDT1 | R/W | | $00000000_B$ |
| $007946_H$ | Timer Control Status 1 | TCCSL1 | R/W | | $00000000_B$ |
| $007947_H$ | Timer Control Status 1 | TCCSH1 | R/W | | $0XXXXXXX_B$ |

*(Continued)*

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $007948_H$ | Timer 0/Reload 0 | TMR0/TMRLR0 | R/W | 16-bit Reload Timer 0 | $XXXXXXXX_B$ |
| $007949_H$ | | | R/W | | $XXXXXXXX_B$ |
| $00794A_H$ | Timer 1/Reload 1 | TMR1/TMRLR1 | R/W | 16-bit Reload Timer 1 | $XXXXXXXX_B$ |
| $00794B_H$ | | | R/W | | $XXXXXXXX_B$ |
| $00794C_H$ | Timer 2/Reload 2 | TMR2/TMRLR2 | R/W | 16-bit Reload Timer 2 | $XXXXXXXX_B$ |
| $00794D_H$ | | | R/W | | $XXXXXXXX_B$ |
| $00794E_H$ | Timer 3/Reload 3 | TMR3/TMRLR3 | R/W | 16-bit Reload Timer 3 | $XXXXXXXX_B$ |
| $00794F_H$ | | | R/W | | $XXXXXXXX_B$ |
| $007950_H$ | Serial Mode Register 3 | SMR3 | W,R/W | UART3 | $00000000_B$ |
| $007951_H$ | Serial Control Register 3 | SCR3 | W,R/W | | $00000000_B$ |
| $007952_H$ | Reception/Transmission Data Register 3 | RDR3/TDR3 | R/W | | $00000000_B$ |
| $007953_H$ | Serial Status Register 3 | SSR3 | R,R/W | | $00001000_B$ |
| $007954_H$ | Extended Communication Control Register 3 | ECCR3 | R,W, R/W | | $000000XX_B$ |
| $007955_H$ | Extended Status Control Register | ESCR3 | R/W | | $00000100_B$ |
| $007956_H$ | Baud Rate Generator Register 30 | BGR30 | R/W | | $00000000_B$ |
| $007957_H$ | Baud Rate Generator Register 31 | BGR31 | R/W | | $00000000_B$ |
| $007958_H$ | Serial Mode Register 4 | SMR4 | W,R/W | UART4 | $00000000_B$ |
| $007959_H$ | Serial Control Register 4 | SCR4 | W,R/W | | $00000000_B$ |
| $00795A_H$ | Reception/Transmission Data Register 4 | RDR4/TDR4 | R/W | | $00000000_B$ |
| $00795B_H$ | Serial Status Register 4 | SSR4 | R,R/W | | $00001000_B$ |
| $00795C_H$ | Extended Communication Control Register 4 | ECCR4 | R,W, R/W | | $000000XX_B$ |
| $00795D_H$ | Extended Status Control Register | ESCR4 | R/W | | $00000100_B$ |
| $00795E_H$ | Baud Rate Generator Register 40 | BGR40 | R/W | | $00000000_B$ |
| $00795F_H$ | Baud Rate Generator Register 41 | BGR41 | R/W | | $00000000_B$ |
| $007960_H$ to $00796B_H$ | Reserved | | | | |
| $00796C_H$ | Clock Output Enable Register | CLKR | R/W | Clock Monitor | $XXXX0000_B$ |
| $00796D_H$ | Reserved | | | | |
| $00796E_H$ | CAN Direct Mode Register | CDMR | R/W | CAN Clock sync | $XXXXXXX0_B$ |
| $00796F_H$ | CAN Switch Register | CANSWR | R/W | CAN 0/1 | $XXXXXX00_B$ |

*(Continued)*

**List of Message Buffers (ID Registers) (2)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| $007A40_H$ | $007C40_H$ | ID Register 8 | IDR8 | R/W | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A41_H$ | $007C41_H$ | | | | |
| $007A42_H$ | $007C42_H$ | | | | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A43_H$ | $007C43_H$ | | | | |
| $007A44_H$ | $007C44_H$ | ID Register 9 | IDR9 | R/W | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A45_H$ | $007C45_H$ | | | | |
| $007A46_H$ | $007C46_H$ | | | | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A47_H$ | $007C47_H$ | | | | |
| $007A48_H$ | $007C48_H$ | ID Register 10 | IDR10 | R/W | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A49_H$ | $007C49_H$ | | | | |
| $007A4A_H$ | $007C4A_H$ | | | | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A4B_H$ | $007C4B_H$ | | | | |
| $007A4C_H$ | $007C4C_H$ | ID Register 11 | IDR11 | R/W | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A4D_H$ | $007C4D_H$ | | | | |
| $007A4E_H$ | $007C4E_H$ | | | | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A4F_H$ | $007C4F_H$ | | | | |
| $007A50_H$ | $007C50_H$ | ID Register 12 | IDR12 | R/W | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A51_H$ | $007C51_H$ | | | | |
| $007A52_H$ | $007C52_H$ | | | | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A53_H$ | $007C53_H$ | | | | |
| $007A54_H$ | $007C54_H$ | ID Register 13 | IDR13 | R/W | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A55_H$ | $007C55_H$ | | | | |
| $007A56_H$ | $007C56_H$ | | | | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A57_H$ | $007C57_H$ | | | | |
| $007A58_H$ | $007C58_H$ | ID Register 14 | IDR14 | R/W | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A59_H$ | $007C59_H$ | | | | |
| $007A5A_H$ | $007C5A_H$ | | | | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A5B_H$ | $007C5B_H$ | | | | |
| $007A5C_H$ | $007C5C_H$ | ID Register 15 | IDR15 | R/W | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A5D_H$ | $007C5D_H$ | | | | |
| $007A5E_H$ | $007C5E_H$ | | | | $XXXXXXXX_B$ $XXXXXXXX_B$ |
| $007A5F_H$ | $007C5F_H$ | | | | |

**List of Message Buffers (DLC Registers and Data Registers) (1)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| $007A60_H$ | $007C60_H$ | DLC Register 0 | DLCR0 | R/W | $XXXXXXXX_B$ |
| $007A61_H$ | $007C61_H$ | | | | |
| $007A62_H$ | $007C62_H$ | DLC Register 1 | DLCR1 | R/W | $XXXXXXXX_B$ |
| $007A63_H$ | $007C63_H$ | | | | |
| $007A64_H$ | $007C64_H$ | DLC Register 2 | DLCR2 | R/W | $XXXXXXXX_B$ |
| $007A65_H$ | $007C65_H$ | | | | |
| $007A66_H$ | $007C66_H$ | DLC Register 3 | DLCR3 | R/W | $XXXXXXXX_B$ |
| $007A67_H$ | $007C67_H$ | | | | |
| $007A68_H$ | $007C68_H$ | DLC Register 4 | DLCR4 | R/W | $XXXXXXXX_B$ |
| $007A69_H$ | $007C69_H$ | | | | |
| $007A6A_H$ | $007C6A_H$ | DLC Register 5 | DLCR5 | R/W | $XXXXXXXX_B$ |
| $007A6B_H$ | $007C6B_H$ | | | | |
| $007A6C_H$ | $007C6C_H$ | DLC Register 6 | DLCR6 | R/W | $XXXXXXXX_B$ |
| $007A6D_H$ | $007C6D_H$ | | | | |
| $007A6E_H$ | $007C6E_H$ | DLC Register 7 | DLCR7 | R/W | $XXXXXXXX_B$ |
| $007A6F_H$ | $007C6F_H$ | | | | |
| $007A70_H$ | $007C70_H$ | DLC Register 8 | DLCR8 | R/W | $XXXXXXXX_B$ |
| $007A71_H$ | $007C71_H$ | | | | |
| $007A72_H$ | $007C72_H$ | DLC Register 9 | DLCR9 | R/W | $XXXXXXXX_B$ |
| $007A73_H$ | $007C73_H$ | | | | |
| $007A74_H$ | $007C74_H$ | DLC Register 10 | DLCR10 | R/W | $XXXXXXXX_B$ |
| $007A75_H$ | $007C75_H$ | | | | |
| $007A76_H$ | $007C76_H$ | DLC Register 11 | DLCR11 | R/W | $XXXXXXXX_B$ |
| $007A77_H$ | $007C77_H$ | | | | |
| $007A78_H$ | $007C78_H$ | DLC Register 12 | DLCR12 | R/W | $XXXXXXXX_B$ |
| $007A79_H$ | $007C79_H$ | | | | |
| $007A7A_H$ | $007C7A_H$ | DLC Register 13 | DLCR13 | R/W | $XXXXXXXX_B$ |
| $007A7B_H$ | $007C7B_H$ | | | | |
| $007A7C_H$ | $007C7C_H$ | DLC Register 14 | DLCR14 | R/W | $XXXXXXXX_B$ |
| $007A7D_H$ | $007C7D_H$ | | | | |
| $007A7E_H$ | $007C7E_H$ | DLC Register 15 | DLCR15 | R/W | $XXXXXXXX_B$ |
| $007A7F_H$ | $007C7F_H$ | | | | |

**List of Message Buffers (DLC Registers and Data Registers) (3)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| $007AF0_H$ to $007AF7_H$ | $007CF0_H$ to $007CF7_H$ | Data Register 14 (8 bytes) | DTR14 | R/W | $XXXXXXXX_B$ to $XXXXXXXX_B$ |
| $007AF8_H$ to $007AFF_H$ | $007CF8_H$ to $007CFF_H$ | Data Register 15 (8 bytes) | DTR15 | R/W | $XXXXXXXX_B$ to $XXXXXXXX_B$ |

## 10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

| Interrupt cause | EI$^2$OS Support | DMA channel number | Interrupt vector | | Interrupt control register | |
|---|---|---|---|---|---|---|
| | | | Number | Address | Number | Address |
| Reset | N | — | #08 | FFFFDC$_H$ | — | — |
| INT9 instruction | N | — | #09 | FFFFD8$_H$ | — | — |
| Exception | N | — | #10 | FFFFD4$_H$ | — | — |
| CAN 0 RX | N | — | #11 | FFFFD0$_H$ | ICR00 | 0000B0$_H$ |
| CAN 0 TX/NS | N | — | #12 | FFFFCC$_H$ | | |
| CAN 1 RX / Input Capture 6 | Y1 | — | #13 | FFFFC8$_H$ | ICR01 | 0000B1$_H$ |
| CAN 1 TX/NS / Input Capture 7 | Y1 | — | #14 | FFFFC4$_H$ | | |
| CAN 2 RX / I$^2$C0 | N | — | #15 | FFFFC0$_H$ | ICR02 | 0000B2$_H$ |
| CAN 2 TX/NS | N | — | #16 | FFFFBC$_H$ | | |
| 16-bit Reload Timer 0 | Y1 | 0 | #17 | FFFFB8$_H$ | ICR03 | 0000B3$_H$ |
| 16-bit Reload Timer 1 | Y1 | 1 | #18 | FFFFB4$_H$ | | |
| 16-bit Reload Timer 2 | Y1 | 2 | #19 | FFFFB0$_H$ | ICR04 | 0000B4$_H$ |
| 16-bit Reload Timer 3 | Y1 | — | #20 | FFFFAC$_H$ | | |
| PPG 0/1/4/5 | N | — | #21 | FFFFA8$_H$ | ICR05 | 0000B5$_H$ |
| PPG 2/3/6/7 | N | — | #22 | FFFFA4$_H$ | | |
| PPG 8/9/C/D | N | — | #23 | FFFFA0$_H$ | ICR06 | 0000B6$_H$ |
| PPG A/B/E/F | N | — | #24 | FFFF9C$_H$ | | |
| Time Base Timer | N | — | #25 | FFFF98$_H$ | ICR07 | 0000B7$_H$ |
| External Interrupt 0 to 3, 8 to 11 | Y1 | 3 | #26 | FFFF94$_H$ | | |
| Watch Timer | N | — | #27 | FFFF90$_H$ | ICR08 | 0000B8$_H$ |
| External Interrupt 4 to 7, 12 to 15 | Y1 | 4 | #28 | FFFF8C$_H$ | | |
| A/D Converter | Y1 | 5 | #29 | FFFF88$_H$ | ICR09 | 0000B9$_H$ |
| Free-run Timer 0 / Free-run Timer 1 | N | — | #30 | FFFF84$_H$ | | |
| Input Capture 4/5 / I$^2$C1 | Y1 | 6 | #31 | FFFF80$_H$ | ICR10 | 0000BA$_H$ |
| Output Compare 0/1/4/5 | Y1 | 7 | #32 | FFFF7C$_H$ | | |
| Input Capture 0 to 3 | Y1 | 8 | #33 | FFFF78$_H$ | ICR11 | 0000BB$_H$ |
| Output Compare 2/3/6/7 | Y1 | 9 | #34 | FFFF74$_H$ | | |
| UART 0 RX | Y2 | 10 | #35 | FFFF70$_H$ | ICR12 | 0000BC$_H$ |
| UART 0 TX | Y1 | 11 | #36 | FFFF6C$_H$ | | |
| UART 1 RX / UART 3 RX | Y2 | 12 | #37 | FFFF68$_H$ | ICR13 | 0000BD$_H$ |
| UART 1 TX / UART 3 TX | Y1 | 13 | #38 | FFFF64$_H$ | | |

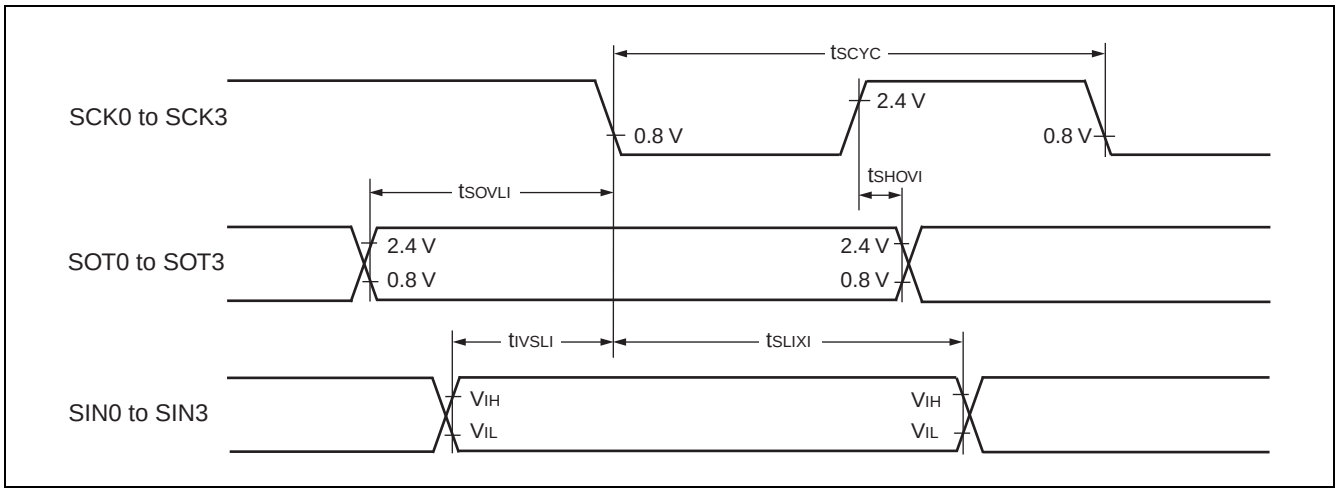
*(Continued)*

■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1**

($T_A$ = −40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal clock operation output pins are $C_L$ = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↑ → SOT delay time | $t_{SHOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | −50 | +50 | ns |
| Valid SIN → SCK ↓ | $t_{IVSLI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↓ → Valid SIN hold time | $t_{SLIXI}$ | SCK0 to SCK3, SIN0 to SIN3 | | 0 | — | ns |
| SOT → SCK ↓ delay time | $t_{SOVLI}$ | SCK0 to SCK3, SOT0 to SOT3 | | 3 $t_{CP}$ − 70 | — | ns |

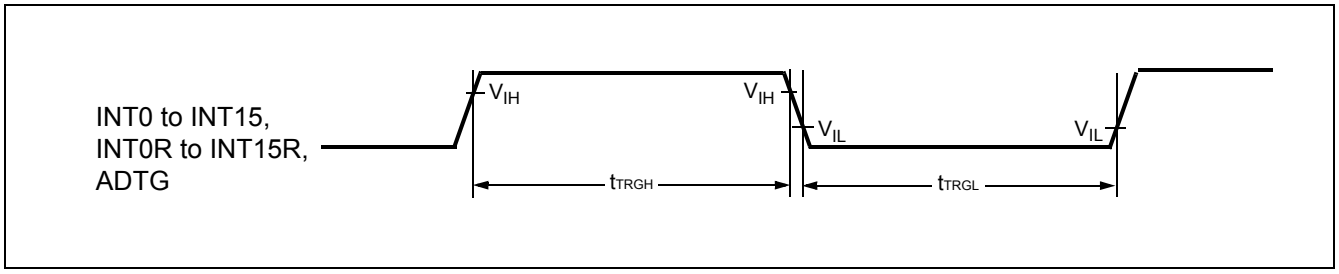
**Note:**
- $C_L$ is load capacity value of pins when testing.
- $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".



### 11.4.10 Trigger Input Timing

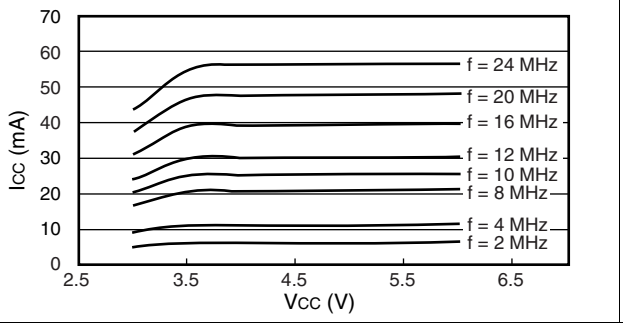
($T_A$ = −40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | INT0 to INT15,<br>INT0R to INT15R,<br>ADTG | — | 5 $t_{CP}$ | — | ns |

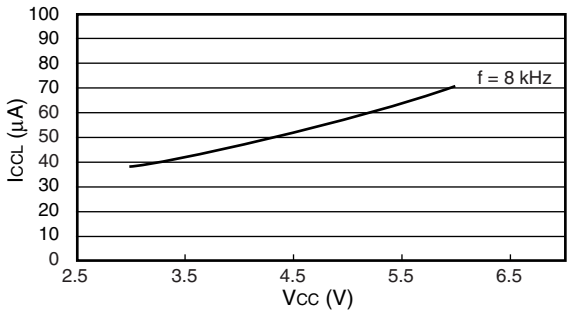


■ MB90F349E, MB90F349ES, MB90F349CE, MB90F349CES

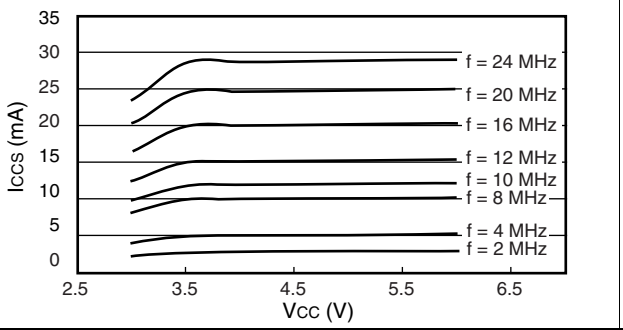
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



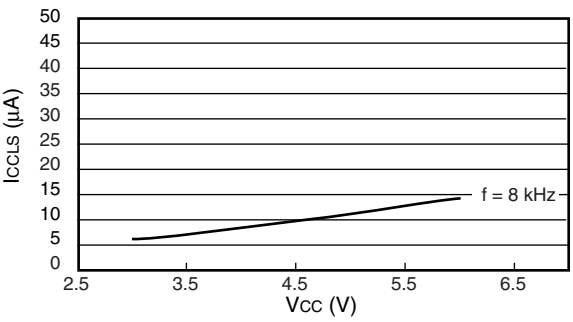

$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



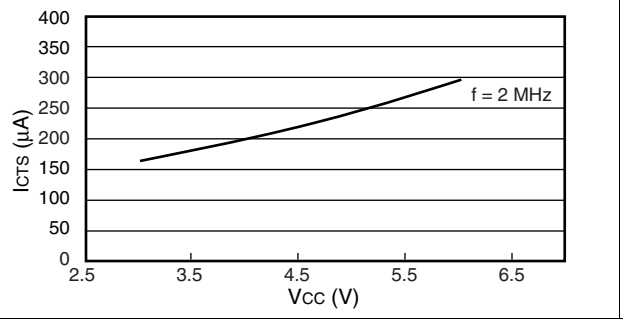

$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



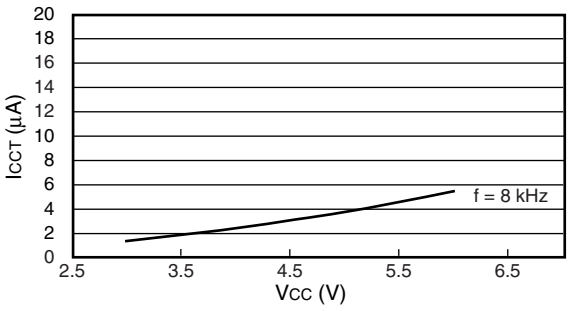

$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



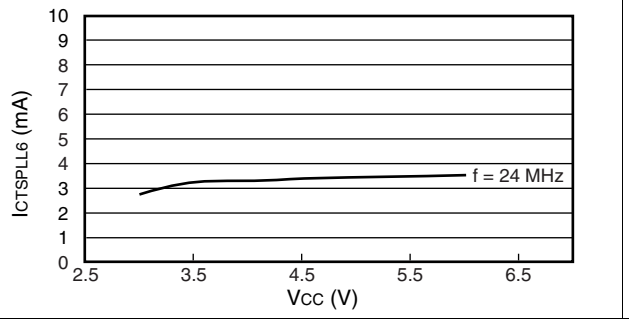

$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



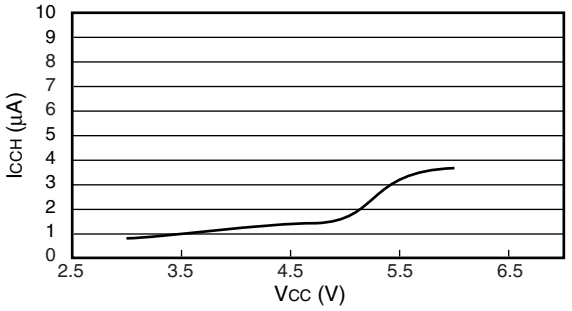

$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency




$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency

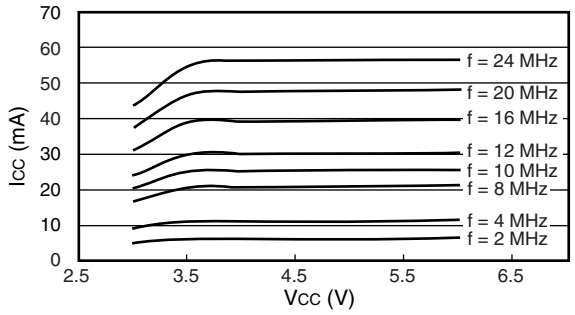



$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

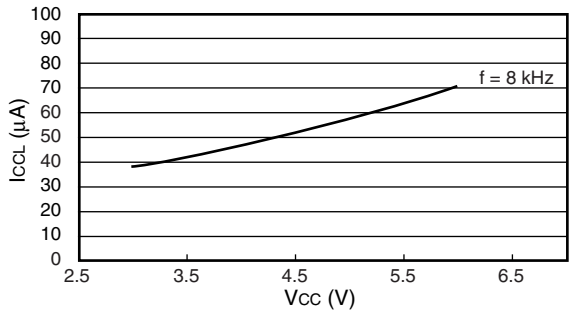


■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

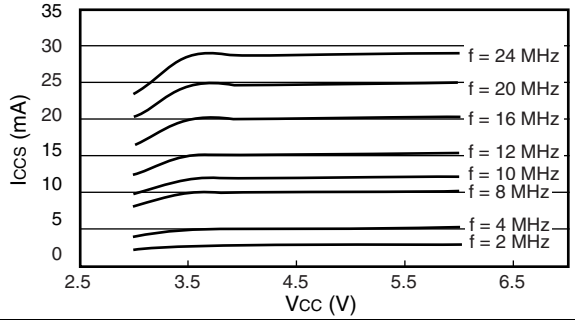
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



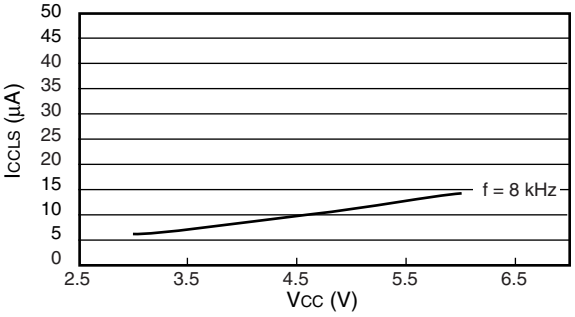

$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



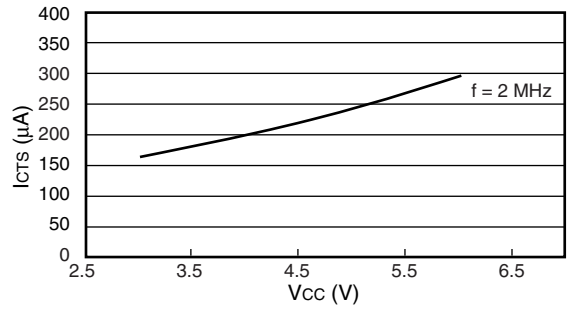

$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



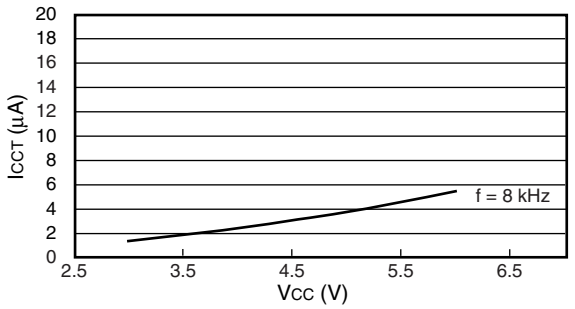

$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



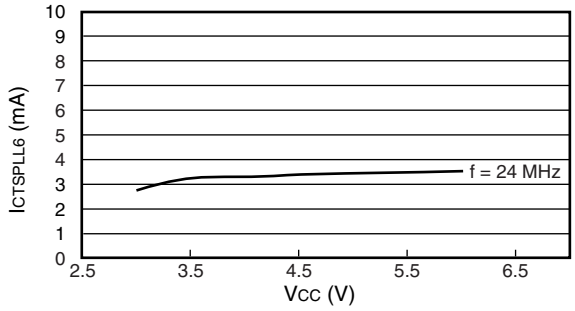

$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



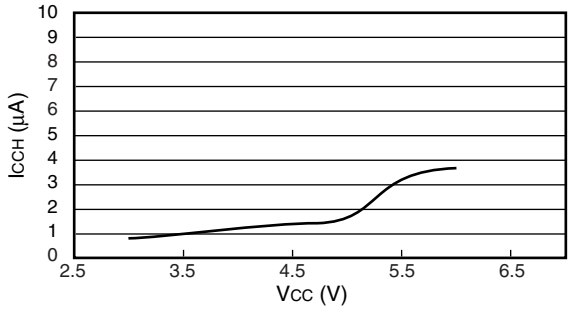

$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency




$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency

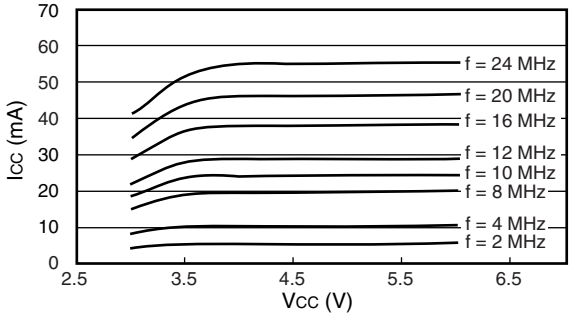



$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

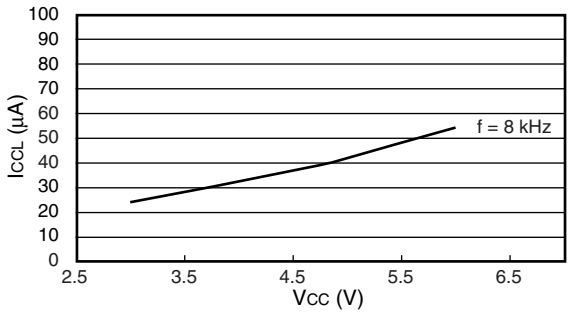


■ MB90346E, MB90346ES, MB90346CE, MB90346CES

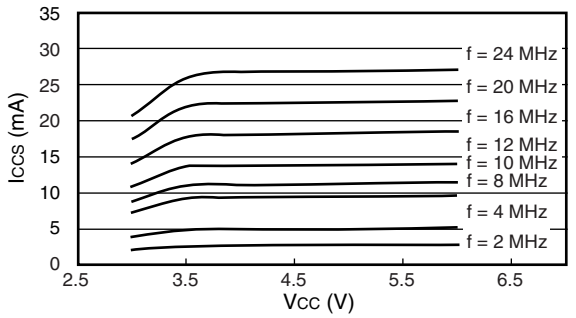
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



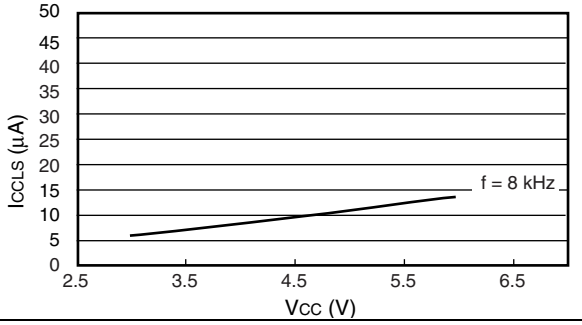

$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



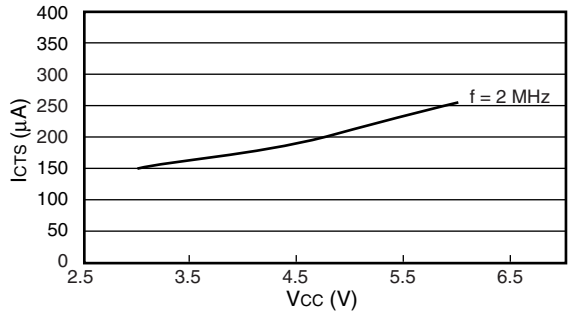

$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



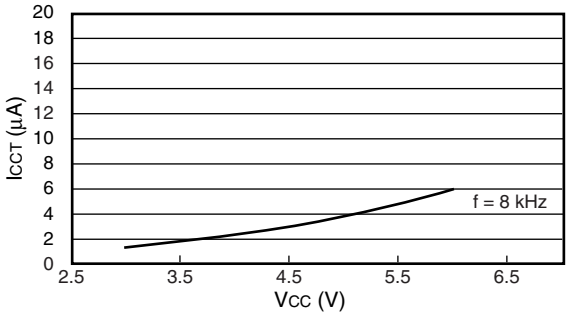

$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



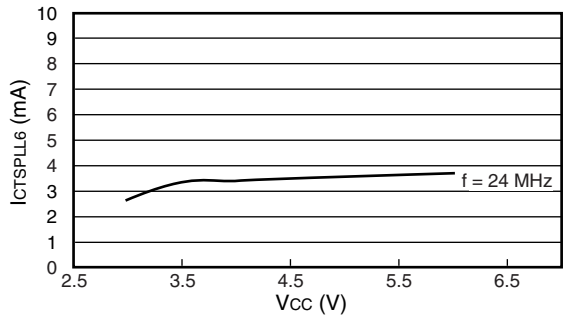

$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency




$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency




$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency




$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped