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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

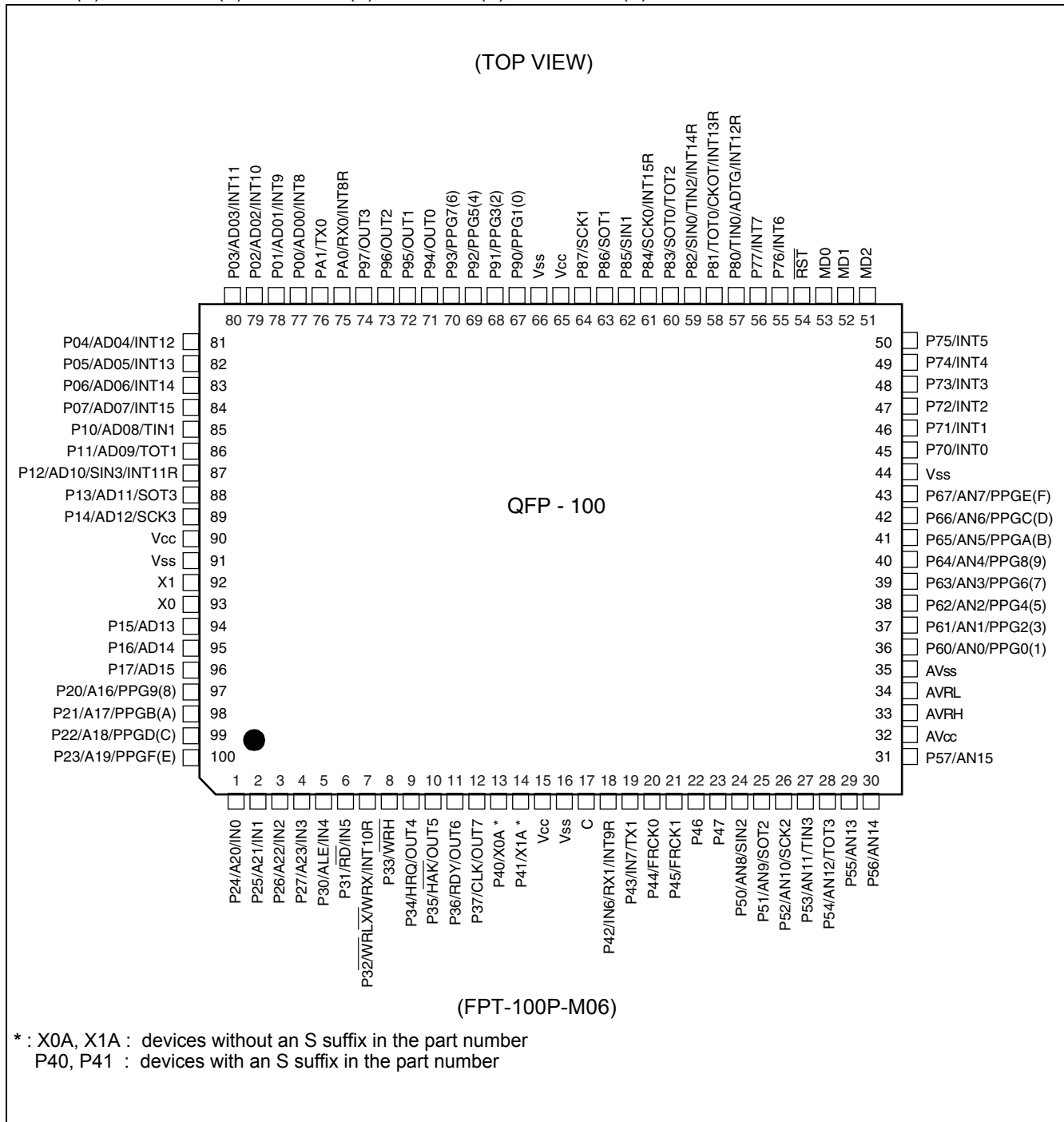
Details

Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 24x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f347cespmc-g-jne1

Part Number	Parameter		
	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
A/D Converter	24 input channels	Devices with a C suffix in the part number : 24 channels Devices without a C suffix in the part number : 16 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs include sample time (per one channel)		
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2 ¹ , fsys/2 ³ , fsys/2 ⁵ (fsys = Machine clock frequency) Supports External Event Count function		
16-bit Free-run Timer (2 channels)	Generates an interrupt signal on overflow Supports Timer Clear when the output compare finds a match Operation clock freq. : fsys, fsys/2 ¹ , fsys/2 ² , fsys/2 ³ , fsys/2 ⁴ , fsys/2 ⁵ , fsys/2 ⁶ , fsys/2 ⁷ (fsys = Machine clock freq.) Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3 Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7		
16-bit Output Compare (8 channels)	Generates an interrupt signal when one of the 16-bit free-run timer matches the output compare register A pair of compare registers can be used to generate an output signal.		
16-bit Input Capture (8 channels)	Captures the value of the 16-bit free-run timer and generates an interrupt when triggered by a pin input (rising edge, falling edge, or both rising and falling edges).		
8/16-bit Programmable Pulse Generator	8 channels (16-bit) /16 channels (8-bit) Sixteen 8-bit reload counters Sixteen 8-bit reload registers for L pulse width Sixteen 8-bit reload registers for H pulse width		
	Supports 8-bit and 16-bit operation modes A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operating clock freq. : fsys, fsys/2 ¹ , fsys/2 ² , fsys/2 ³ , fsys/2 ⁴ or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)		
CAN Interface	3 channels	2 channels : MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S) 1 channel : MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	2 channels : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S) 1 channel : MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission in response to Remote Frames Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		

2. Pin Assignments

■ MB90341E(S), MB90342E(S), MB90F342E(S), MB90F345E(S), MB90346E(S), MB90F346E(S), MB90347E(S), MB90F347E(S), MB90348E(S), MB90349E(S), MB90F349E(S)



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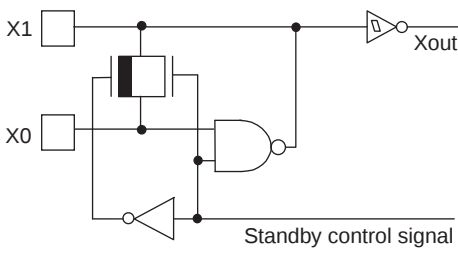
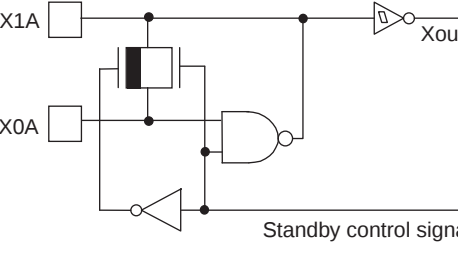
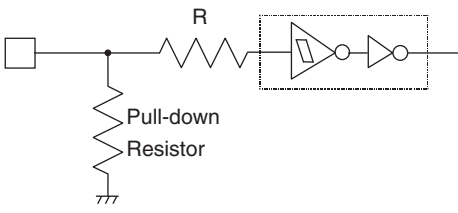
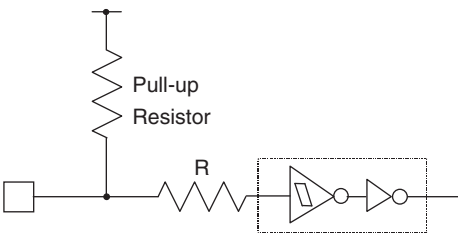
Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I ² C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I ² C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV _{CC}	K	Analog power input pin for the A/D Converter

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
66	64	V _{SS}	—	GND pin
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pins
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pins
		OUT0 to OUT3		Waveform output pins for output compares. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin
76	74	PA1	F	General purpose I/O pin.
		TX0		TX Output pin for CAN0
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer

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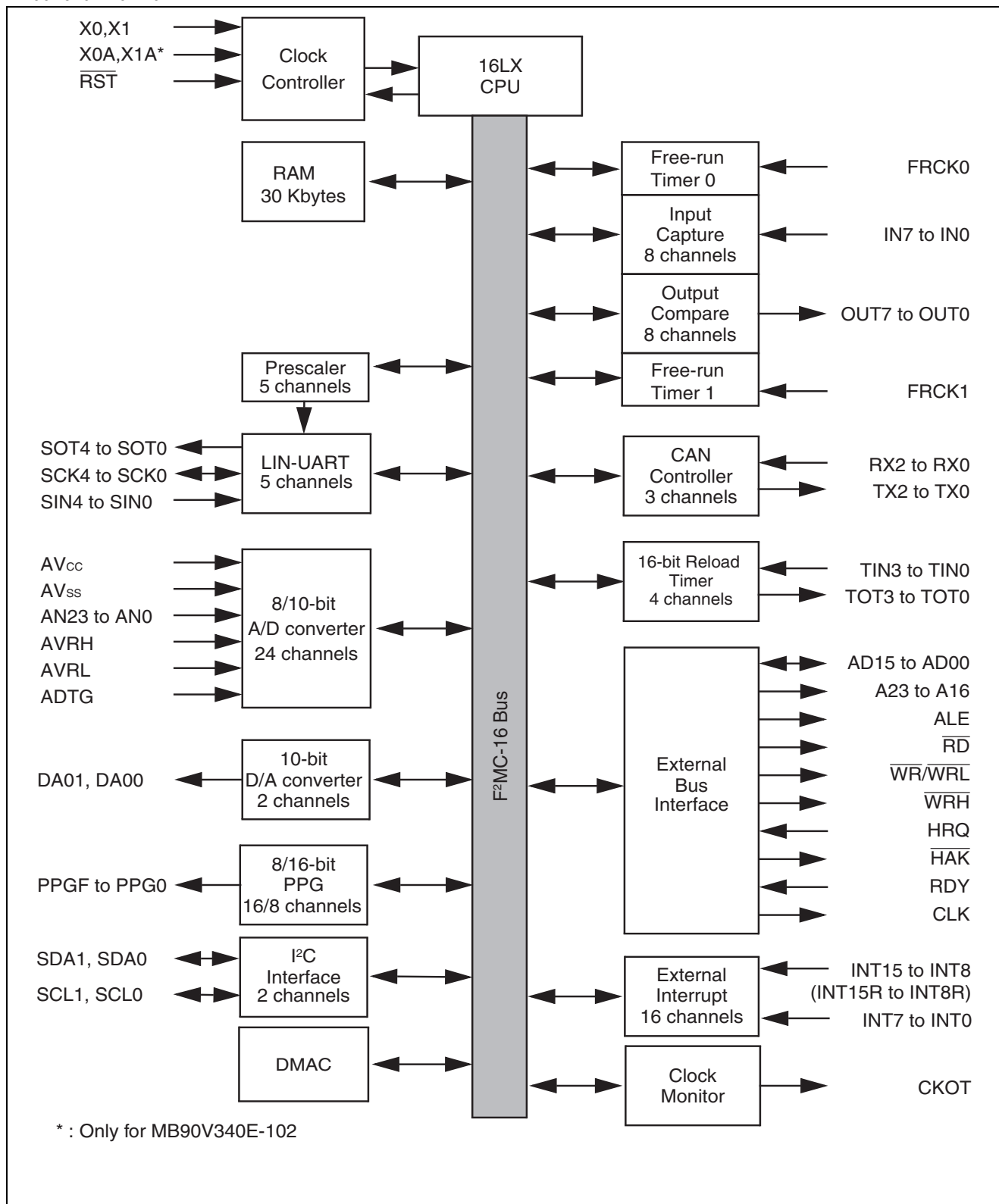
4. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		■ MASK ROM and evaluation products: CMOS hysteresis input pin ■ Flash memory products: CMOS input pin
D		MASK ROM and evaluation products: ■ CMOS hysteresis input pin ■ Pull-down resistor value: approx. 50 kΩ Flash memory products: ■ CMOS input pin ■ No pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ

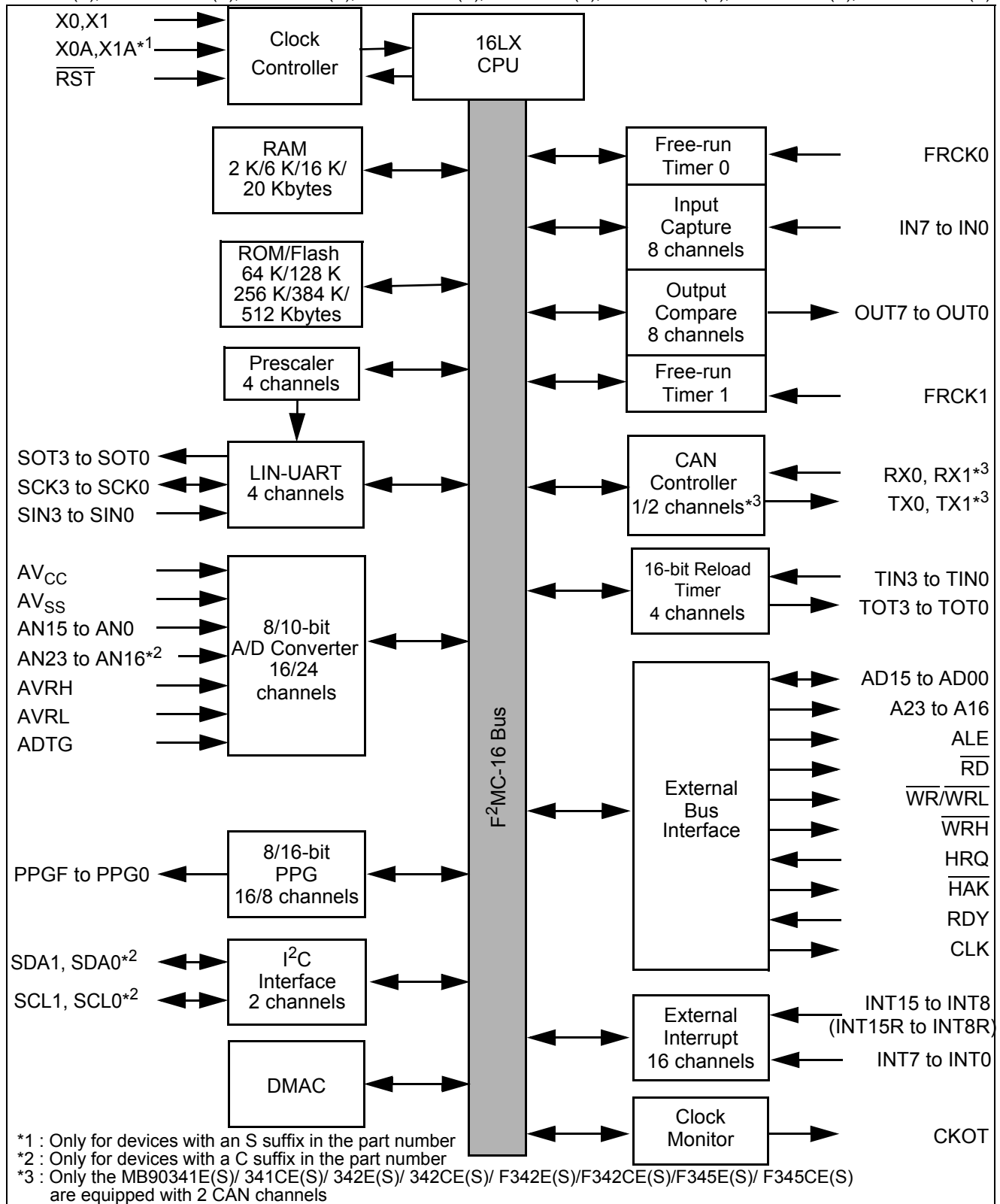
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6. Block Diagrams

■ MB90V340E-101/102



■ MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)



8. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
000000 _H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX _B
000001 _H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX _B
000002 _H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX _B
000003 _H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX _B
000004 _H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX _B
000005 _H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX _B
000006 _H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX _B
000007 _H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX _B
000008 _H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX _B
000009 _H	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXXX _B
00000A _H	Port A Data Register	PDRA	R/W	Port A	XXXXXXXX _B
00000B _H	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	1111111 _B
00000C _H	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	1111111 _B
00000D _H	Port 7 Analog Input Enable Register	ADER7	R/W	Port 7, A/D	1111111 _B
00000E _H	Input Level Select Register 0	ILSR0	R/W	Ports	XXXXXXXX _B
00000F _H	Input Level Select Register 1	ILSR1	R/W	Ports	XXXX0XXX _B
000010 _H	Port 0 Direction Register	DDR0	R/W	Port 0	0000000 _B
000011 _H	Port 1 Direction Register	DDR1	R/W	Port 1	0000000 _B
000012 _H	Port 2 Direction Register	DDR2	R/W	Port 2	0000000 _B
000013 _H	Port 3 Direction Register	DDR3	R/W	Port 3	0000000 _B
000014 _H	Port 4 Direction Register	DDR4	R/W	Port 4	0000000 _B
000015 _H	Port 5 Direction Register	DDR5	R/W	Port 5	0000000 _B
000016 _H	Port 6 Direction Register	DDR6	R/W	Port 6	0000000 _B
000017 _H	Port 7 Direction Register	DDR7	R/W	Port 7	0000000 _B
000018 _H	Port 8 Direction Register	DDR8	R/W	Port 8	0000000 _B
000019 _H	Port 9 Direction Register	DDR9	R/W	Port 9	0000000 _B
00001A _H	Port A Direction Register	DDRA	R/W	Port A	00000100 _B
00001B _H	Reserved				
00001C _H	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	0000000 _B
00001D _H	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	0000000 _B
00001E _H	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	0000000 _B
00001F _H	Port 3 Pull-up Control Register	PUCR3	W, R/W	Port 3	0000000 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
000020 _H	Serial Mode Register 0	SMR0	W,R/W	UART0	00000000 _B
000021 _H	Serial Control Register 0	SCR0	W,R/W		00000000 _B
000022 _H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000 _B
000023 _H	Serial Status Register 0	SSR0	R,R/W		00001000 _B
000024 _H	Extended Communication Control Register 0	ECCR0	R,W, R/W		000000XX _B
000025 _H	Extended Status/Control Register 0	ESCR0	R/W		00000100 _B
000026 _H	Baud Rate Generator Register 00	BGR00	R/W		00000000 _B
000027 _H	Baud Rate Generator Register 01	BGR01	R/W		00000000 _B
000028 _H	Serial Mode Register 1	SMR1	W,R/W	UART1	00000000 _B
000029 _H	Serial Control Register 1	SCR1	W,R/W		00000000 _B
00002A _H	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000 _B
00002B _H	Serial Status Register 1	SSR1	R,R/W		00001000 _B
00002C _H	Extended Communication Control Register 1	ECCR1	R,W, R/W		000000XX _B
00002D _H	Extended Status/Control Register 1	ESCR1	R/W		00000100 _B
00002E _H	Baud Rate Generator Register 10	BGR10	R/W		00000000 _B
00002F _H	Baud Rate Generator Register 11	BGR11	R/W		00000000 _B
000030 _H	PPG 0 Operation Mode Control Register	PPGC0	W,R/W	16-bit PPG 0/1	0X000XX1 _B
000031 _H	PPG 1 Operation Mode Control Register	PPGC1	W,R/W		0X000001 _B
000032 _H	PPG 0/PPG 1 Count Clock Select Register	PPG01	R/W		000000X0 _B
000033 _H	Reserved				
000034 _H	PPG 2 Operation Mode Control Register	PPGC2	W,R/W	16-bit PPG 2/3	0X000XX1 _B
000035 _H	PPG 3 Operation Mode Control Register	PPGC3	W,R/W		0X000001 _B
000036 _H	PPG 2/PPG 3 Count Clock Select Register	PPG23	R/W		000000X0 _B
000037 _H	Reserved				
000038 _H	PPG 4 Operation Mode Control Register	PPGC4	W,R/W	16-bit PPG 4/5	0X000XX1 _B
000039 _H	PPG 5 Operation Mode Control Register	PPGC5	W,R/W		0X000001 _B
00003A _H	PPG 4/PPG 5 Clock Select Register	PPG45	R/W		000000X0 _B
00003B _H	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000 _B
00003C _H	PPG 6 Operation Mode Control Register	PPGC6	W,R/W	16-bit PPG 6/7	0X000XX1 _B
00003D _H	PPG 7 Operation Mode Control Register	PPGC7	W,R/W		0X000001 _B
00003E _H	PPG 6/PPG 7 Count Clock Control Register	PPG67	R/W		000000X0 _B
00003F _H	Reserved				

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Address	Register	Abbreviation	Access	Resource name	Initial value
007948 _H	Timer 0/Reload 0	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	XXXXXXXX _B
007949 _H			R/W		XXXXXXXX _B
00794A _H	Timer 1/Reload 1	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	XXXXXXXX _B
00794B _H			R/W		XXXXXXXX _B
00794C _H	Timer 2/Reload 2	TMR2/TMRLR2	R/W	16-bit Reload Timer 2	XXXXXXXX _B
00794D _H			R/W		XXXXXXXX _B
00794E _H	Timer 3/Reload 3	TMR3/TMRLR3	R/W	16-bit Reload Timer 3	XXXXXXXX _B
00794F _H			R/W		XXXXXXXX _B
007950 _H	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000 _B
007951 _H	Serial Control Register 3	SCR3	W,R/W		00000000 _B
007952 _H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000 _B
007953 _H	Serial Status Register 3	SSR3	R,R/W		00001000 _B
007954 _H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XX _B
007955 _H	Extended Status Control Register	ESCR3	R/W		00000100 _B
007956 _H	Baud Rate Generator Register 30	BGR30	R/W		00000000 _B
007957 _H	Baud Rate Generator Register 31	BGR31	R/W		00000000 _B
007958 _H	Serial Mode Register 4	SMR4	W,R/W	UART4	00000000 _B
007959 _H	Serial Control Register 4	SCR4	W,R/W		00000000 _B
00795A _H	Reception/Transmission Data Register 4	RDR4/TDR4	R/W		00000000 _B
00795B _H	Serial Status Register 4	SSR4	R,R/W		00001000 _B
00795C _H	Extended Communication Control Register 4	ECCR4	R,W, R/W		000000XX _B
00795D _H	Extended Status Control Register	ESCR4	R/W		00000100 _B
00795E _H	Baud Rate Generator Register 40	BGR40	R/W		00000000 _B
00795F _H	Baud Rate Generator Register 41	BGR41	R/W		00000000 _B
007960 _H to 00796B _H	Reserved				
00796C _H	Clock Output Enable Register	CLKR	R/W	Clock Monitor	XXXX0000 _B
00796D _H	Reserved				
00796E _H	CAN Direct Mode Register	CDMR	R/W	CAN Clock sync	XXXXXXX0 _B
00796F _H	CAN Switch Register	CANSWR	R/W	CAN 0/1	XXXXXXX0 _B

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Address	Register	Abbreviation	Access	Resource name	Initial value
007970 _H	I ² C Bus Status Register 0	IBSR0	R	I ² C Interface 0	00000000 _B
007971 _H	I ² C Bus Control Register 0	IBCR0	W,R/W		00000000 _B
007972 _H	I ² C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000 _B
007973 _H		ITBAH0	R/W		00000000 _B
007974 _H	I ² C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111 _B
007975 _H		ITMKH0	R/W		00111111 _B
007976 _H	I ² C 7-bit Slave Address Register 0	ISBA0	R/W		00000000 _B
007977 _H	I ² C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111 _B
007978 _H	I ² C Data Register 0	IDAR0	R/W		00000000 _B
007979 _H , 00797A _H	Reserved				
00797B _H	I ² C Clock Control Register 0	ICCR0	R/W	I ² C Interface 0	00011111 _B
00797C _H to 00797F _H	Reserved				
007980 _H	I ² C Bus Status Register 1	IBSR1	R	I ² C Interface 1	00000000 _B
007981 _H	I ² C Bus Control Register 1	IBCR1	W,R/W		00000000 _B
007982 _H	I ² C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000 _B
007983 _H		ITBAH1	R/W		00000000 _B
007984 _H	I ² C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111 _B
007985 _H		ITMKH1	R/W		00111111 _B
007986 _H	I ² C 7-bit Slave Address Register 1	ISBA1	R/W		00000000 _B
007987 _H	I ² C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111 _B
007988 _H	I ² C Data Register 1	IDAR1	R/W		00000000 _B
007989 _H , 00798A _H	Reserved				
00798B _H	I ² C Clock Control Register 1	ICCR1	R/W	I ² C Interface 1	00011111 _B
00798C _H to 0079C1 _H	Reserved				
0079C2 _H	Clock Modulator Control Register	CMCR	R, R/W	Clock Modulator	0001X000 _B
0079C3 _H to 0079DF _H	Reserved				

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9. CAN Controllers

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
- Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
- 29-bit ID and 8-byte data
- Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
- Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
000070 _H	000080 _H	Message Buffer Valid Register	BVALR	R/W	00000000 _B 00000000 _B
000071 _H	000081 _H				
000072 _H	000082 _H	Transmit Request Register	TREQR	R/W	00000000 _B 00000000 _B
000073 _H	000083 _H				
000074 _H	000084 _H	Transmit Cancel Register	TCANR	W	00000000 _B 00000000 _B
000075 _H	000085 _H				
000076 _H	000086 _H	Transmission Complete Register	TCR	R/W	00000000 _B 00000000 _B
000077 _H	000087 _H				
000078 _H	000088 _H	Receive Complete Register	RCR	R/W	00000000 _B 00000000 _B
000079 _H	000089 _H				
00007A _H	00008A _H	Remote Request Receiving Register	RRTRR	R/W	00000000 _B 00000000 _B
00007B _H	00008B _H				
00007C _H	00008C _H	Receive Overrun Register	ROVRR	R/W	00000000 _B 00000000 _B
00007D _H	00008D _H				
00007E _H	00008E _H	Reception Interrupt Enable Register	RIER	R/W	00000000 _B 00000000 _B
00007F _H	00008F _H				

List of Message Buffers (ID Registers) (1)

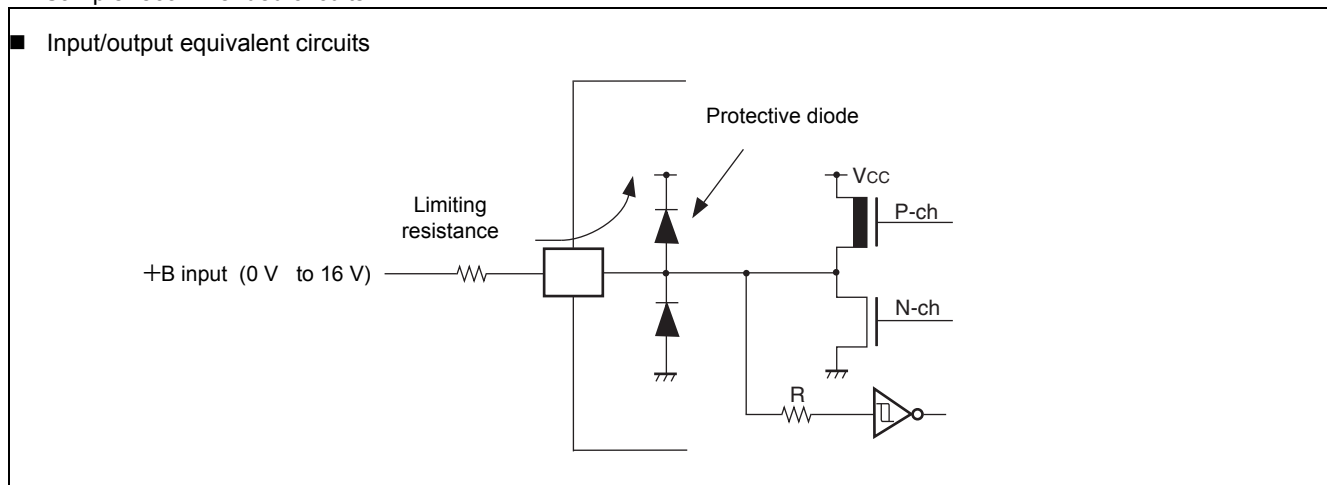
Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A00 _H to 007A1F _H	007C00 _H to 007C1F _H	General- Purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
007A20 _H	007C20 _H	ID Register 0	IDR0	R/W	XXXXXXXX _B XXXXXXXX _B
007A21 _H	007C21 _H				XXXXXXXX _B XXXXXXXX _B
007A22 _H	007C22 _H				XXXXXXXX _B XXXXXXXX _B
007A23 _H	007C23 _H				XXXXXXXX _B XXXXXXXX _B
007A24 _H	007C24 _H	ID Register 1	IDR1	R/W	XXXXXXXX _B XXXXXXXX _B
007A25 _H	007C25 _H				XXXXXXXX _B XXXXXXXX _B
007A26 _H	007C26 _H				XXXXXXXX _B XXXXXXXX _B
007A27 _H	007C27 _H				XXXXXXXX _B XXXXXXXX _B
007A28 _H	007C28 _H	ID Register 2	IDR2	R/W	XXXXXXXX _B XXXXXXXX _B
007A29 _H	007C29 _H				XXXXXXXX _B XXXXXXXX _B
007A2A _H	007C2A _H				XXXXXXXX _B XXXXXXXX _B
007A2B _H	007C2B _H				XXXXXXXX _B XXXXXXXX _B
007A2C _H	007C2C _H	ID Register 3	IDR3	R/W	XXXXXXXX _B XXXXXXXX _B
007A2D _H	007C2D _H				XXXXXXXX _B XXXXXXXX _B
007A2E _H	007C2E _H				XXXXXXXX _B XXXXXXXX _B
007A2F _H	007C2F _H				XXXXXXXX _B XXXXXXXX _B
007A30 _H	007C30 _H	ID Register 4	IDR4	R/W	XXXXXXXX _B XXXXXXXX _B
007A31 _H	007C31 _H				XXXXXXXX _B XXXXXXXX _B
007A32 _H	007C32 _H				XXXXXXXX _B XXXXXXXX _B
007A33 _H	007C33 _H				XXXXXXXX _B XXXXXXXX _B
007A34 _H	007C34 _H	ID Register 5	IDR5	R/W	XXXXXXXX _B XXXXXXXX _B
007A35 _H	007C35 _H				XXXXXXXX _B XXXXXXXX _B
007A36 _H	007C36 _H				XXXXXXXX _B XXXXXXXX _B
007A37 _H	007C37 _H				XXXXXXXX _B XXXXXXXX _B
007A38 _H	007C38 _H	ID Register 6	IDR6	R/W	XXXXXXXX _B XXXXXXXX _B
007A39 _H	007C39 _H				XXXXXXXX _B XXXXXXXX _B
007A3A _H	007C3A _H				XXXXXXXX _B XXXXXXXX _B
007A3B _H	007C3B _H				XXXXXXXX _B XXXXXXXX _B
007A3C _H	007C3C _H	ID Register 7	IDR7	R/W	XXXXXXXX _B XXXXXXXX _B
007A3D _H	007C3D _H				XXXXXXXX _B XXXXXXXX _B
007A3E _H	007C3E _H				XXXXXXXX _B XXXXXXXX _B
007A3F _H	007C3F _H				XXXXXXXX _B XXXXXXXX _B

List of Message Buffers (DLC Registers and Data Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A80 _H to 007A87 _H	007C80 _H to 007C87 _H	Data Register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B
007A88 _H to 007A8F _H	007C88 _H to 007C8F _H	Data Register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
007A90 _H to 007A97 _H	007C90 _H to 007C97 _H	Data Register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
007A98 _H to 007A9F _H	007C98 _H to 007C9F _H	Data Register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
007AA0 _H to 007AA7 _H	007CA0 _H to 007CA7 _H	Data Register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
007AA8 _H to 007AAF _H	007CA8 _H to 007CAF _H	Data Register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
007AB0 _H to 007AB7 _H	007CB0 _H to 007CB7 _H	Data Register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
007AB8 _H to 007ABF _H	007CB8 _H to 007CBF _H	Data Register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
007AC0 _H to 007AC7 _H	007CC0 _H to 007CC7 _H	Data Register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
007AC8 _H to 007ACF _H	007CC8 _H to 007CCF _H	Data Register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
007AD0 _H to 007AD7 _H	007CD0 _H to 007CD7 _H	Data Register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
007AD8 _H to 007ADF _H	007CD8 _H to 007CDF _H	Data Register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
007AE0 _H to 007AE7 _H	007CE0 _H to 007CE7 _H	Data Register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
007AE8 _H to 007AEF _H	007CE8 _H to 007CEF _H	Data Register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B

(Continued)

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:



*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

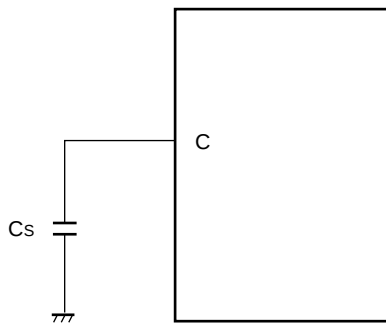
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

11.2 Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	0.1	—	1.0	μF	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.
Operating temperature	T_A	-40	—	+105	$^{\circ}\text{C}$	

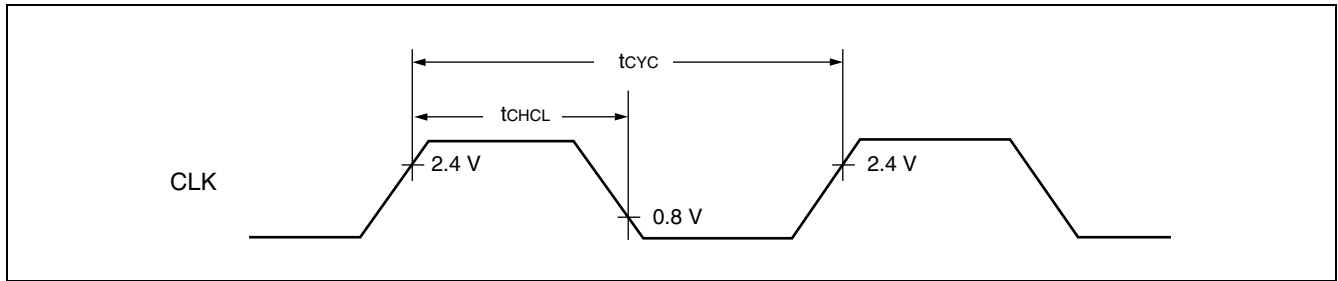
C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

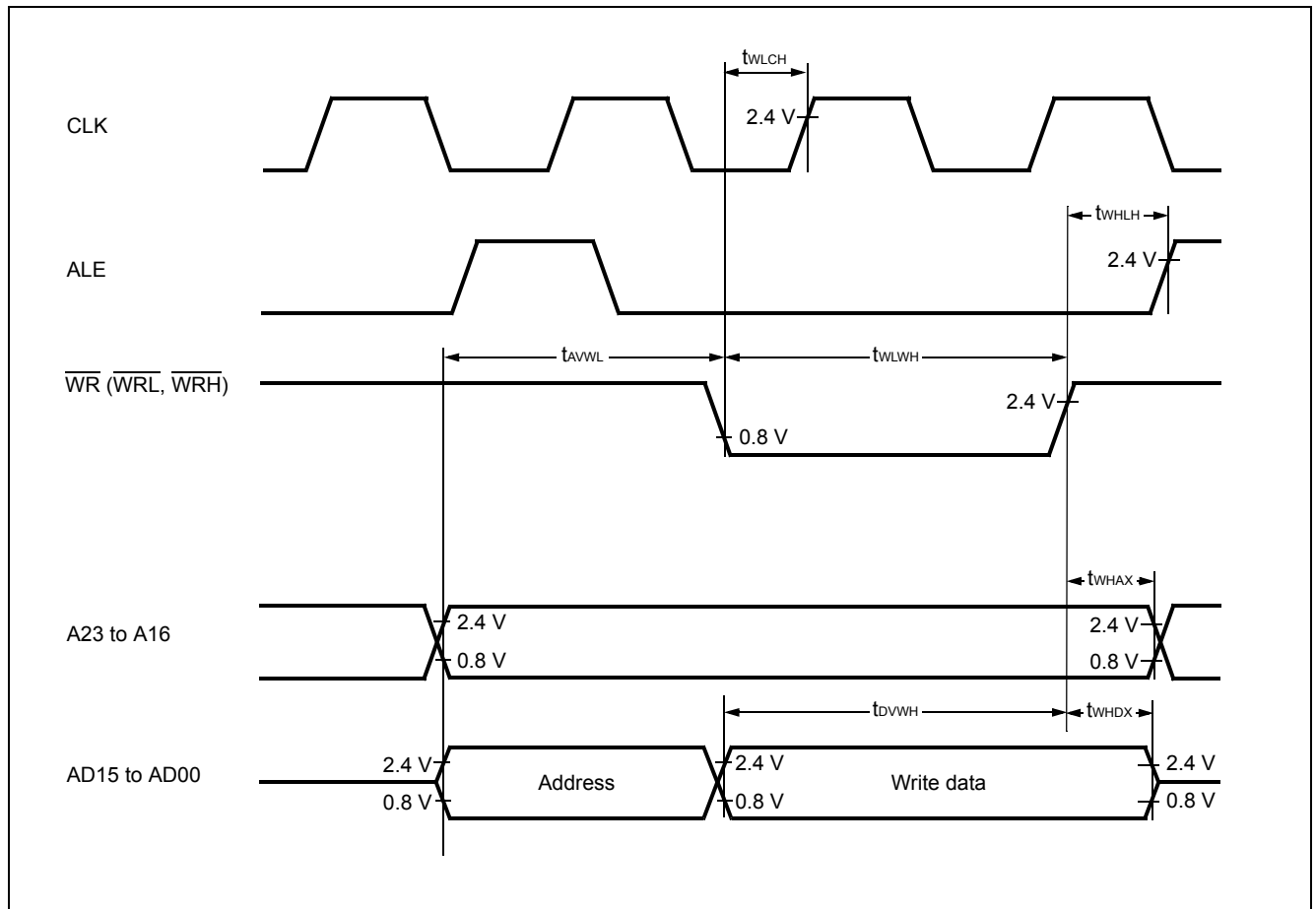
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



11.4.6 Bus Timing (Write)

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Valid address $\rightarrow \overline{\text{WR}} \downarrow$ time	t_{AVWL}	A23 to A16, AD15 to AD00, $\overline{\text{WR}}$	—	$t_{\text{CP}} - 15$	—	ns
$\overline{\text{WR}}$ pulse width	t_{WLWH}	$\overline{\text{WR}}$		$3 t_{\text{CP}}/2 - 20$	—	ns
Valid data output $\rightarrow \overline{\text{WR}} \uparrow$ time	t_{DVWH}	AD15 to AD00, $\overline{\text{WR}}$		$3 t_{\text{CP}}/2 - 20$	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ Data hold time	t_{WHDX}	AD15 to AD00, $\overline{\text{WR}}$		15	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ Address valid time	t_{WHAX}	A23 to A16, $\overline{\text{WR}}$		$t_{\text{CP}}/2 - 10$	—	ns
$\overline{\text{WR}} \uparrow \rightarrow$ ALE $\uparrow$ time	t_{WHLH}	$\overline{\text{WR}}$, ALE		$t_{\text{CP}}/2 - 15$	—	ns
$\overline{\text{WR}} \downarrow \rightarrow$ CLK $\uparrow$ time	t_{WLCH}	$\overline{\text{WR}}$, CLK		$t_{\text{CP}}/2 - 15$	—	ns



11.5 A/D Converter

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$, $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = \text{AV}_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential nonlinearity error	—	—	—	—	± 1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	$\text{AVRL} - 1.5 \times \text{LSB}$	$\text{AVRL} + 0.5 \times \text{LSB}$	$\text{AVRL} + 2.5 \times \text{LSB}$	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	$\text{AVRH} - 3.5 \times \text{LSB}$	$\text{AVRH} - 1.5 \times \text{LSB}$	$\text{AVRH} + 0.5 \times \text{LSB}$	V	
Compare time	—	—	1.0	—	16500	μs	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			2.0				$4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Sampling time	—	—	0.5	—	∞	μs	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			1.2				$4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Analog port input current	I_{AIN}	AN0 to AN23	-0.3	—	+0.3	μA	
Analog input voltage range	V_{AIN}	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	$\text{AVRL} + 2.7$	—	AV_{CC}	V	
	—	AVRL	0	—	$\text{AVRH} - 2.7$	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage current	I_R	AVRH	—	600	900	μA	
	I_{RH}	AVRH	—	—	5	μA	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

*: If the A/D convertor is not operating, a current when CPU is stopped is applicable ($V_{CC} = \text{AV}_{CC} = \text{AVRH} = 5.0\text{ V}$).

Note: : The accuracy gets worse as $|\text{AVRH} - \text{AVRL}|$ becomes smaller.

■ MB90F342E, MB90F342ES, MB90F342CE, MB90F342CES

