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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f347espmc-g

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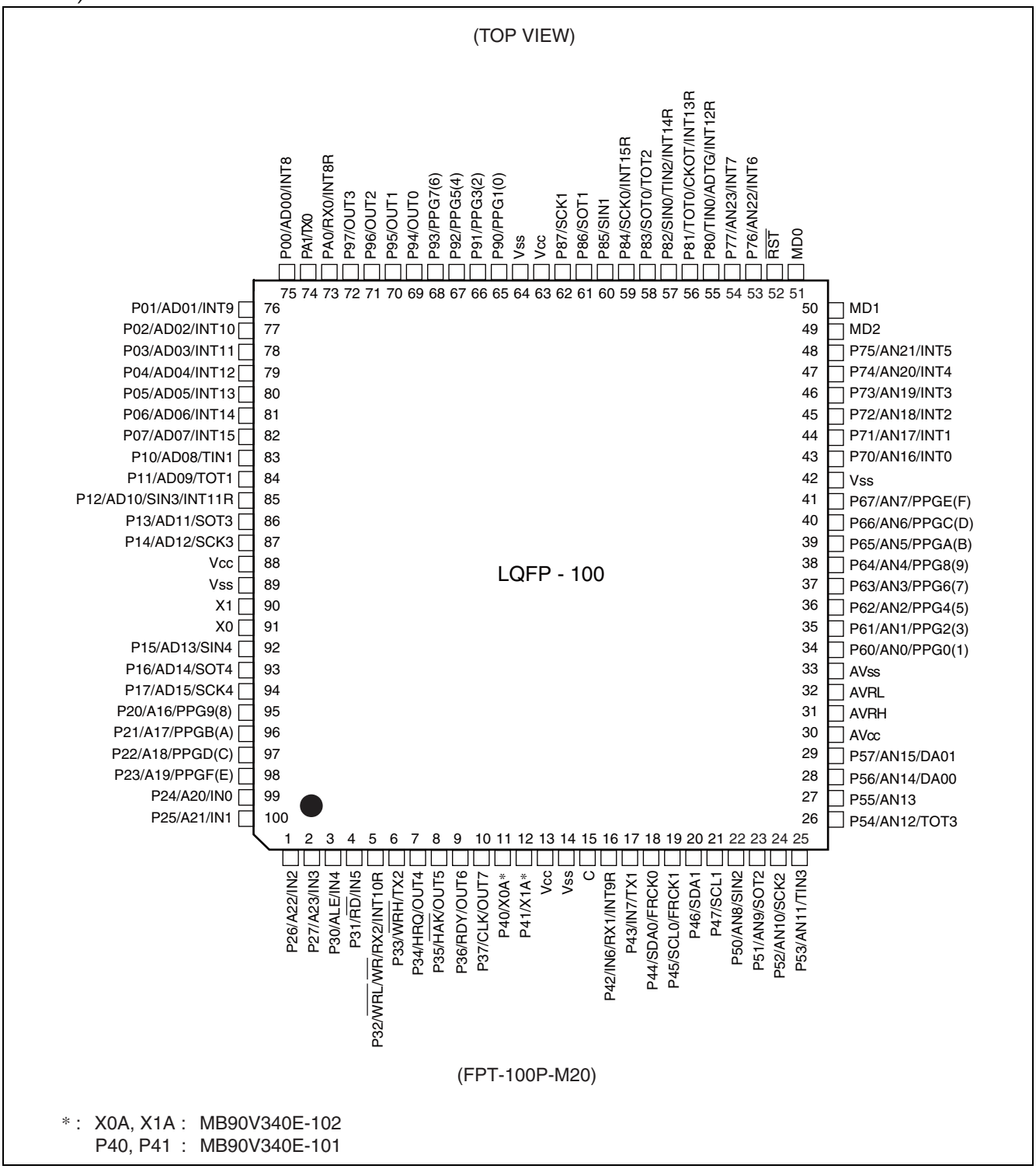

This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
61	59	P84	F	General purpose I/O pin.
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin
62	60	P85	M	General purpose I/O pin.
		SIN1		Serial data input pin for UART1
63	61	P86	F	General purpose I/O pin.
		SOT1		Serial data output pin for UART1
64	62	P87	F	General purpose I/O pin.
		SCK1		Clock I/O pin for UART1
65	63	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
66	64	V_{SS}	—	GND pin
67 to 70	65 to 68	P90 to P93	F	General purpose I/O pins
		PPG1, 3, 5, 7		Output pins for PPGs
71 to 74	69 to 72	P94 to P97	F	General purpose I/O pins
		OUT0 to OUT3		Waveform output pins for output compares. This function is enabled when the OCU enables waveform output.
75	73	PA0	F	General purpose I/O pin.
		RX0		RX input pin for CAN0 Interface
		INT8R		External interrupt request input pin
76	74	PA1	F	General purpose I/O pin.
		TX0		TX Output pin for CAN0
77 to 84	75 to 82	P00 to P07	G	General purpose I/O pins. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins.
85	83	P10	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer

(Continued)

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
86	84	P11	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer
87	85	P12	N	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin
88	86	P13	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
89	87	P14	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3
90	88	V_{CC}	—	Power (3.5 V to 5.5 V) input pin
91	89	V_{SS}	—	GND pin
92	90	X1	A	Main clock output pin
93	91	X0		Main clock input pin
94	92	P15	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.
95	93	P16	G	General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin for the external address/data bus. This function is enabled when the external bus is enabled.

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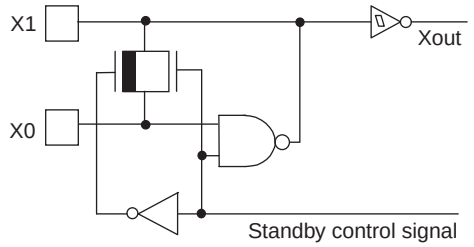
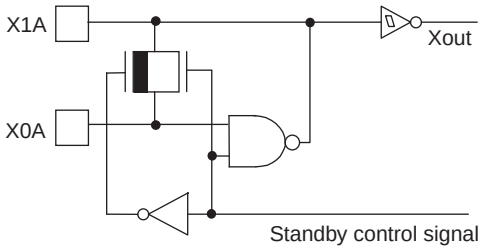
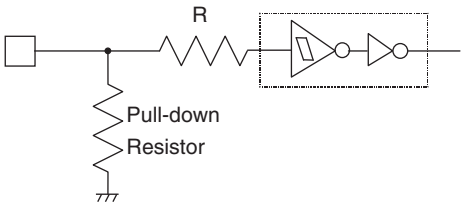
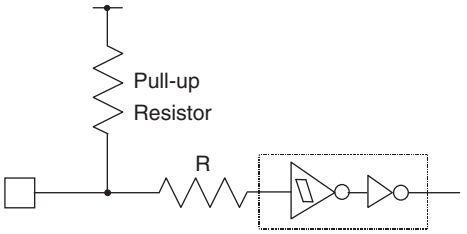
4. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		■ MASK ROM and evaluation products: CMOS hysteresis input pin ■ Flash memory products: CMOS input pin
D		MASK ROM and evaluation products: ■ CMOS hysteresis input pin ■ Pull-down resistor value: approx. 50 kΩ Flash memory products: ■ CMOS input pin ■ No pull-down
E		CMOS hysteresis input pin Pull-up resistor value: approx. 50 kΩ

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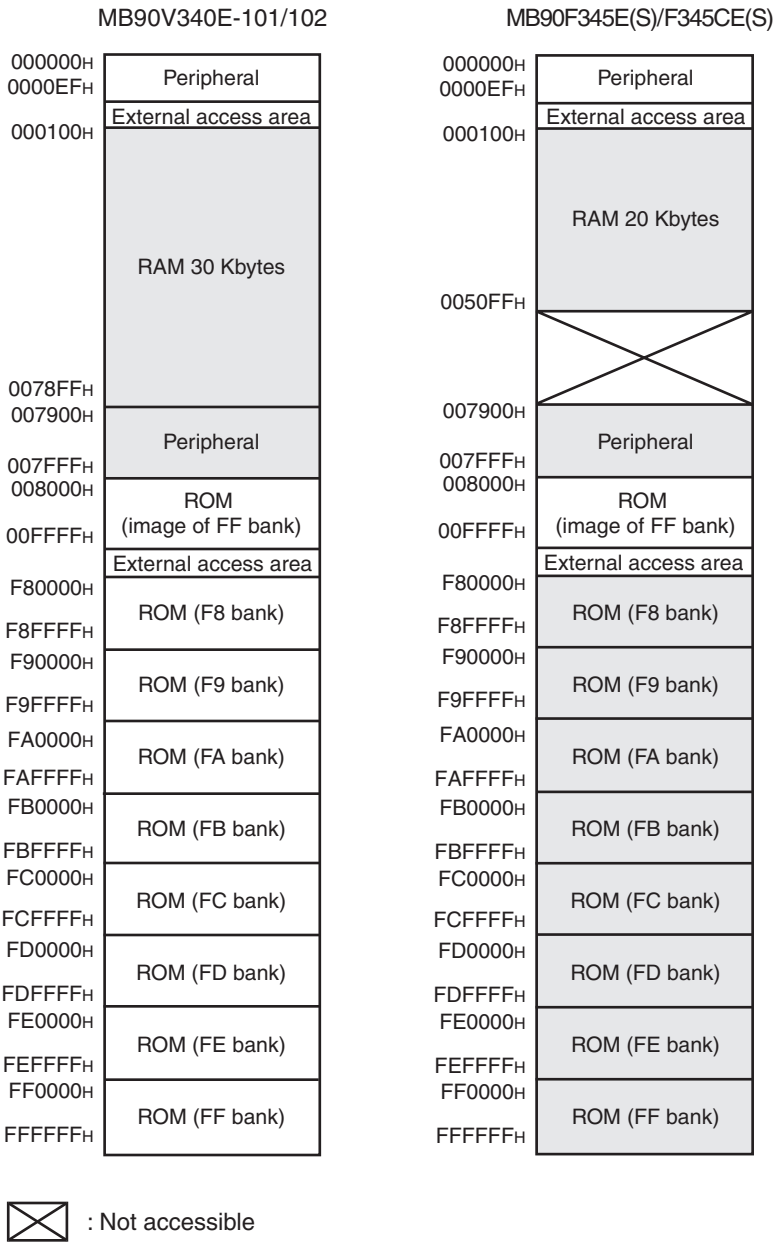
7. Memory Map


MB90V340E-101/102
000000H
0000EFH
Peripheral
External access area
000100H
RAM 30 Kbytes
0078FFH
007900H
Peripheral
007FFFH
008000H
ROM
(image of FF bank)
00FFFFH
External access area
F80000H
ROM (F8 bank)
F8FFFFH
F90000H
ROM (F9 bank)
F9FFFFH
FA0000H
ROM (FA bank)
FAFFFFH
FB0000H
ROM (FB bank)
FBFFFFH
FC0000H
ROM (FC bank)
FCFFFFH
FD0000H
ROM (FD bank)
FDFFFFH
FE0000H
ROM (FE bank)
FEFFFFH
FF0000H
ROM (FF bank)
FFFFFFH
MB90F345E(S)/F345CE(S)
000000H
0000EFH
Peripheral
External access area
000100H
RAM 20 Kbytes
0050FFH
007900H
Peripheral
007FFFH
008000H
ROM
(image of FF bank)
00FFFFH
External access area
F80000H
ROM (F8 bank)
F8FFFFH
F90000H
ROM (F9 bank)
F9FFFFH
FA0000H
ROM (FA bank)
FAFFFFH
FB0000H
ROM (FB bank)
FBFFFFH
FC0000H
ROM (FC bank)
FCFFFFH
FD0000H
ROM (FD bank)
FDFFFFH
FE0000H
ROM (FE bank)
FEFFFFH
FF0000H
ROM (FF bank)
FFFFFFH
: Not accessible

Address	Register	Abbreviation	Access	Resource name	Initial value
007948_H	Timer 0/Reload 0	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	$XXXXXXXX_B$
007949_H			R/W		$XXXXXXXX_B$
$00794A_H$	Timer 1/Reload 1	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	$XXXXXXXX_B$
$00794B_H$			R/W		$XXXXXXXX_B$
$00794C_H$	Timer 2/Reload 2	TMR2/TMRLR2	R/W	16-bit Reload Timer 2	$XXXXXXXX_B$
$00794D_H$			R/W		$XXXXXXXX_B$
$00794E_H$	Timer 3/Reload 3	TMR3/TMRLR3	R/W	16-bit Reload Timer 3	$XXXXXXXX_B$
$00794F_H$			R/W		$XXXXXXXX_B$
007950_H	Serial Mode Register 3	SMR3	W,R/W	UART3	00000000_B
007951_H	Serial Control Register 3	SCR3	W,R/W		00000000_B
007952_H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000_B
007953_H	Serial Status Register 3	SSR3	R,R/W		00001000_B
007954_H	Extended Communication Control Register 3	ECCR3	R,W, R/W		$000000XX_B$
007955_H	Extended Status Control Register	ESCR3	R/W		00000100_B
007956_H	Baud Rate Generator Register 30	BGR30	R/W		00000000_B
007957_H	Baud Rate Generator Register 31	BGR31	R/W		00000000_B
007958_H	Serial Mode Register 4	SMR4	W,R/W	UART4	00000000_B
007959_H	Serial Control Register 4	SCR4	W,R/W		00000000_B
$00795A_H$	Reception/Transmission Data Register 4	RDR4/TDR4	R/W		00000000_B
$00795B_H$	Serial Status Register 4	SSR4	R,R/W		00001000_B
$00795C_H$	Extended Communication Control Register 4	ECCR4	R,W, R/W		$000000XX_B$
$00795D_H$	Extended Status Control Register	ESCR4	R/W		00000100_B
$00795E_H$	Baud Rate Generator Register 40	BGR40	R/W		00000000_B
$00795F_H$	Baud Rate Generator Register 41	BGR41	R/W		00000000_B
007960_H to $00796B_H$	Reserved				
$00796C_H$	Clock Output Enable Register	CLKR	R/W	Clock Monitor	$XXXX0000_B$
$00796D_H$	Reserved				
$00796E_H$	CAN Direct Mode Register	CDMR	R/W	CAN Clock sync	$XXXXXXX0_B$
$00796F_H$	CAN Switch Register	CANSWR	R/W	CAN 0/1	$XXXXXX00_B$

(Continued)

List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A40_H$	$007C40_H$	ID Register 8	IDR8	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A41_H$	$007C41_H$				
$007A42_H$	$007C42_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A43_H$	$007C43_H$				
$007A44_H$	$007C44_H$	ID Register 9	IDR9	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A45_H$	$007C45_H$				
$007A46_H$	$007C46_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A47_H$	$007C47_H$				
$007A48_H$	$007C48_H$	ID Register 10	IDR10	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A49_H$	$007C49_H$				
$007A4A_H$	$007C4A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4B_H$	$007C4B_H$				
$007A4C_H$	$007C4C_H$	ID Register 11	IDR11	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4D_H$	$007C4D_H$				
$007A4E_H$	$007C4E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4F_H$	$007C4F_H$				
$007A50_H$	$007C50_H$	ID Register 12	IDR12	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A51_H$	$007C51_H$				
$007A52_H$	$007C52_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A53_H$	$007C53_H$				
$007A54_H$	$007C54_H$	ID Register 13	IDR13	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A55_H$	$007C55_H$				
$007A56_H$	$007C56_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A57_H$	$007C57_H$				
$007A58_H$	$007C58_H$	ID Register 14	IDR14	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A59_H$	$007C59_H$				
$007A5A_H$	$007C5A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5B_H$	$007C5B_H$				
$007A5C_H$	$007C5C_H$	ID Register 15	IDR15	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5D_H$	$007C5D_H$				
$007A5E_H$	$007C5E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5F_H$	$007C5F_H$				

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A60_H$	$007C60_H$	DLC Register 0	DLCR0	R/W	$XXXXXXXX_B$
$007A61_H$	$007C61_H$				
$007A62_H$	$007C62_H$	DLC Register 1	DLCR1	R/W	$XXXXXXXX_B$
$007A63_H$	$007C63_H$				
$007A64_H$	$007C64_H$	DLC Register 2	DLCR2	R/W	$XXXXXXXX_B$
$007A65_H$	$007C65_H$				
$007A66_H$	$007C66_H$	DLC Register 3	DLCR3	R/W	$XXXXXXXX_B$
$007A67_H$	$007C67_H$				
$007A68_H$	$007C68_H$	DLC Register 4	DLCR4	R/W	$XXXXXXXX_B$
$007A69_H$	$007C69_H$				
$007A6A_H$	$007C6A_H$	DLC Register 5	DLCR5	R/W	$XXXXXXXX_B$
$007A6B_H$	$007C6B_H$				
$007A6C_H$	$007C6C_H$	DLC Register 6	DLCR6	R/W	$XXXXXXXX_B$
$007A6D_H$	$007C6D_H$				
$007A6E_H$	$007C6E_H$	DLC Register 7	DLCR7	R/W	$XXXXXXXX_B$
$007A6F_H$	$007C6F_H$				
$007A70_H$	$007C70_H$	DLC Register 8	DLCR8	R/W	$XXXXXXXX_B$
$007A71_H$	$007C71_H$				
$007A72_H$	$007C72_H$	DLC Register 9	DLCR9	R/W	$XXXXXXXX_B$
$007A73_H$	$007C73_H$				
$007A74_H$	$007C74_H$	DLC Register 10	DLCR10	R/W	$XXXXXXXX_B$
$007A75_H$	$007C75_H$				
$007A76_H$	$007C76_H$	DLC Register 11	DLCR11	R/W	$XXXXXXXX_B$
$007A77_H$	$007C77_H$				
$007A78_H$	$007C78_H$	DLC Register 12	DLCR12	R/W	$XXXXXXXX_B$
$007A79_H$	$007C79_H$				
$007A7A_H$	$007C7A_H$	DLC Register 13	DLCR13	R/W	$XXXXXXXX_B$
$007A7B_H$	$007C7B_H$				
$007A7C_H$	$007C7C_H$	DLC Register 14	DLCR14	R/W	$XXXXXXXX_B$
$007A7D_H$	$007C7D_H$				
$007A7E_H$	$007C7E_H$	DLC Register 15	DLCR15	R/W	$XXXXXXXX_B$
$007A7F_H$	$007C7F_H$				

List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007AF0_H$ to $007AF7_H$	$007CF0_H$ to $007CF7_H$	Data Register 14 (8 bytes)	DTR14	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AF8_H$ to $007AFF_H$	$007CF8_H$ to $007CFF_H$	Data Register 15 (8 bytes)	DTR15	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

(Continued)

Interrupt cause	EI^{2}OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX / UART 4 RX	Y2	14	#39	$FFFF60_H$	ICR14	$0000BE_H$
UART 2 TX / UART 4 TX	Y1	15	#40	$FFFF5C_H$		
Flash Memory	N	——	#41	$FFFF58_H$	ICR15	$0000BF_H$
Delayed Interrupt	N	——	#42	$FFFF54_H$		

Y1 : Usable
Y2 : Usable, with EI^{2}OS stop function
N : Unusable

Note:
- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
- When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

11.3 DC Characteristics

($T_A = -40°C$ to $+105°C$, $V_{CC} = 5.0\ V \pm 10\%$, $f_{CP} \leq 24$ MHz, $V_{SS} = AV_{SS} = 0\ V$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At V_{CC} = 5 V ± 10%)	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	V_{CC} + 0.3	V	Port inputs if TTL input levels are selected
	V_{IHS}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHI}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	V_{CC} − 0.3	—	V_{CC} + 0.3	V	MD input pin
Input L voltage (At V_{CC} = 5 V ± 10%)	V_{ILS}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{ILA}	—	—	V_{SS} − 0.3	—	0.5 V_{CC}	V	Port inputs if Automotive input levels are selected
	V_{ILT}	—	—	V_{SS} − 0.3	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILI}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	V_{SS} − 0.3	—	V_{SS} + 0.3	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	V_{CC} − 0.5	—	—	V	
Output H voltage	V_{OHI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OH} = −3.0 mA	V_{CC} − 0.5	—	—	V	
Output L voltage	V_{OL}	Normal outputs	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Output L voltage	V_{OLI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OL} = 3.0 mA	—	—	0.4	V	

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(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	−1	—	+1	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Except Flash memory devices
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 24 MHz, At normal operation.	—	55	70	mA	
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At writing Flash memory.	—	70	85	mA	Flash memory devices
			V_{CC} = 5.0 V, Internal frequency : 24 MHz, At erasing Flash memory.	—	75	90	mA	Flash memory devices
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 24 MHz, In Sleep mode.	—	25	35	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, In Main Timer mode	—	0.3	0.8	mA	
	$I_{CTSPLL6}$		V_{CC} = 5.0 V, Internal frequency : 24 MHz, In PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		V_{CC} = 5.0 V Internal frequency : 8 kHz, In sub operation T_A = +25°C	—	70	140	µA	
	I_{CCLS}		V_{CC} = 5.0 V Internal frequency : 8 kHz, In sub sleep T_A = +25°C	—	20	50	µA	
	I_{CCT}		V_{CC} = 5.0 V Internal frequency : 8 kHz, In watch mode T_A = +25°C	—	10	35	µA	
	I_{CCH}		V_{CC} = 5.0 V, In Stop mode, T_A = +25°C	—	7	25	µA	
Input capacitance	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}	—	—	5	15	pF	

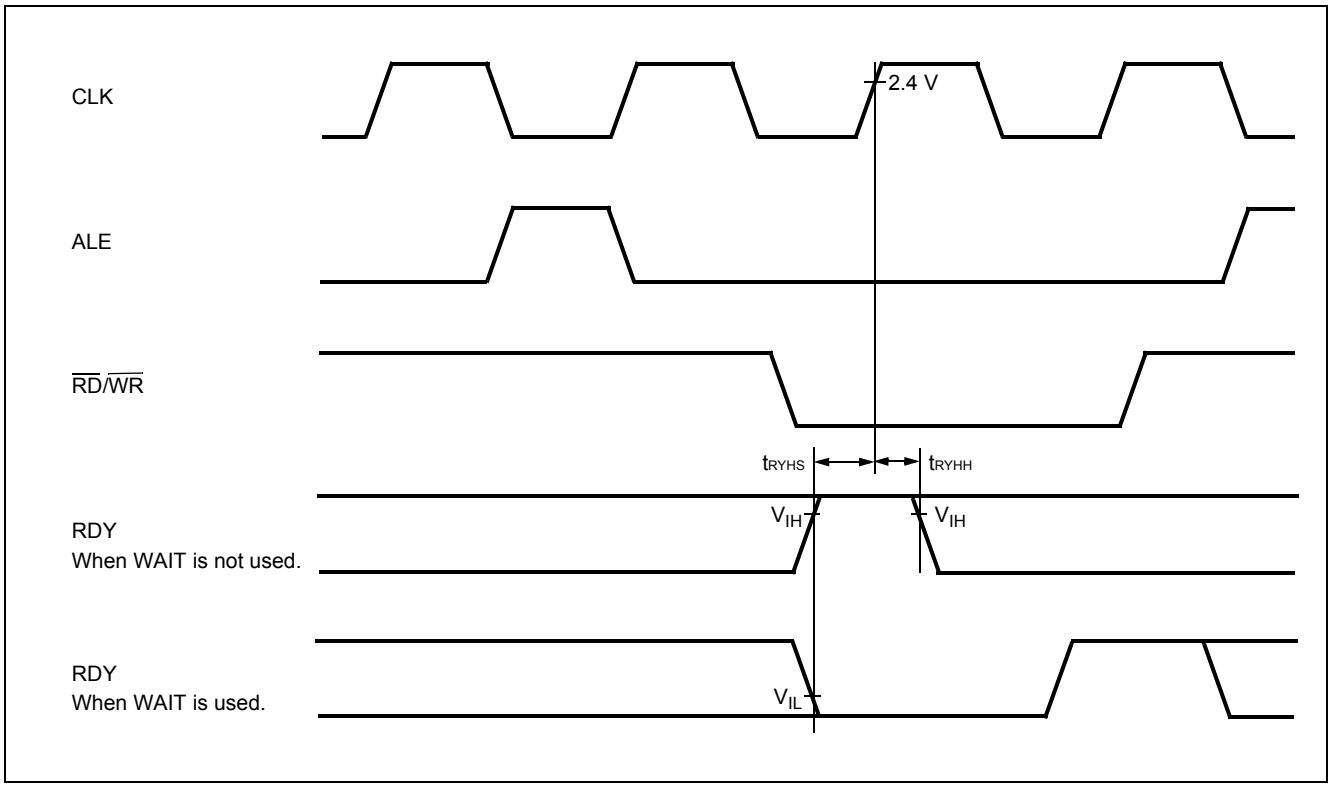
* : The power supply current is measured with an external clock.

11.4.7 Ready Input Timing

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Test Condition	Rated Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	f_{CP} = 16 MHz
				32	—	ns	f_{CP} = 24 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

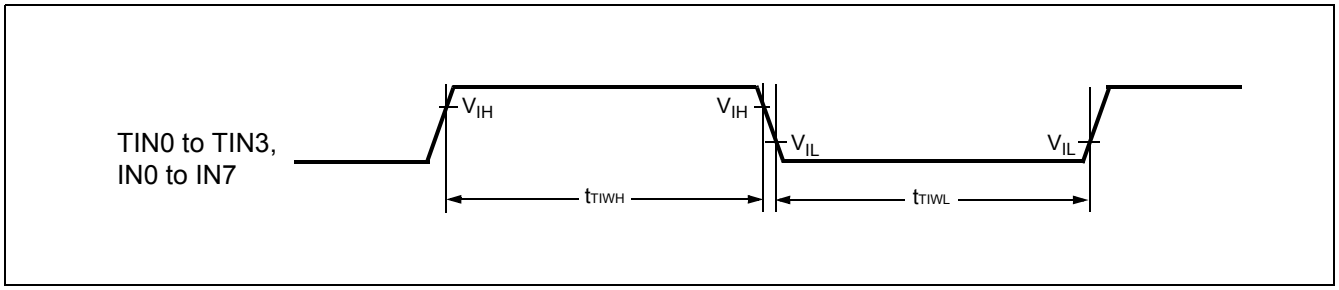
Note: : If the RDY setup time is insufficient, use the auto-ready function.



11.4.11 Timer Related Resource Input Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

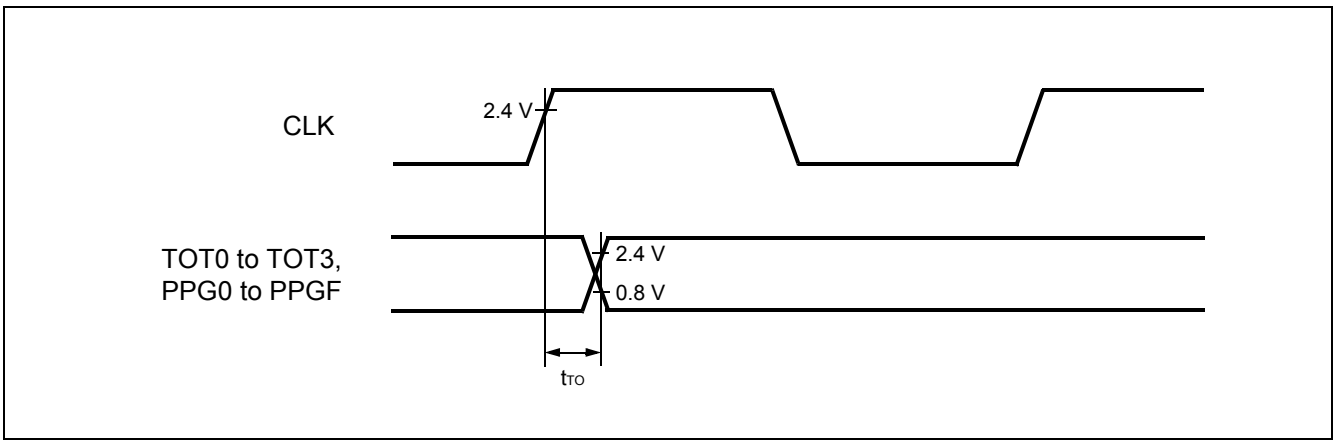
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN3, IN0 to IN7	—	4 t_{CP}	—	ns



11.4.12 Timer Related Resource Output Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT0 to TOT3, PPG0 to PPGF	—	30	—	ns



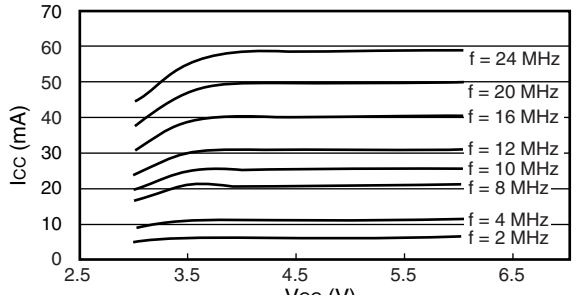
11.8 Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25°C$ $V_{CC} = 5.0$ V	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3600	µs	Except for the over head time of the system
Program/Erase cycle	—	10000	—	—	cycle	
Flash Data Retention Time	Average $T_A = +85°C$	20	—	—	year	*

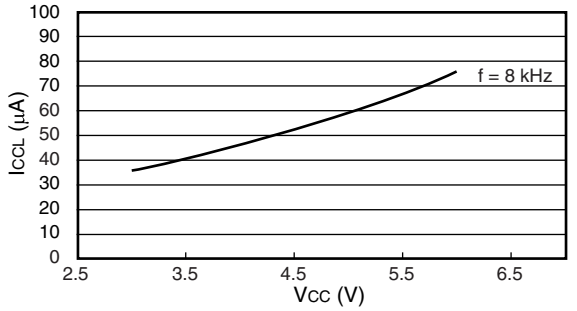
* : This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at +85°C) .

■ MB90F345E, MB90F345ES, MB90F345CE, MB90F345CES

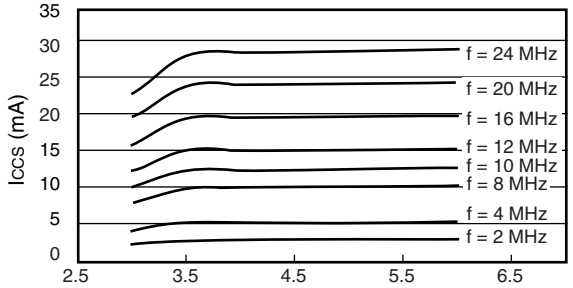
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



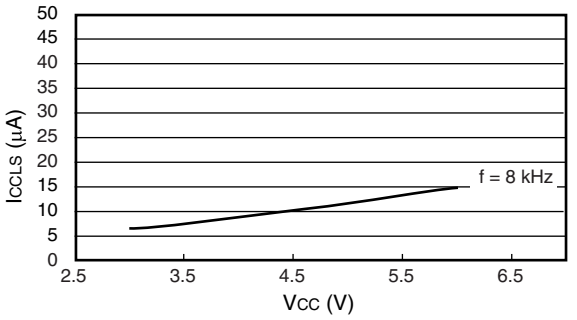
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



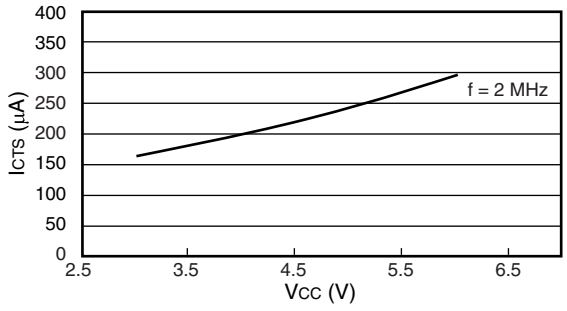
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



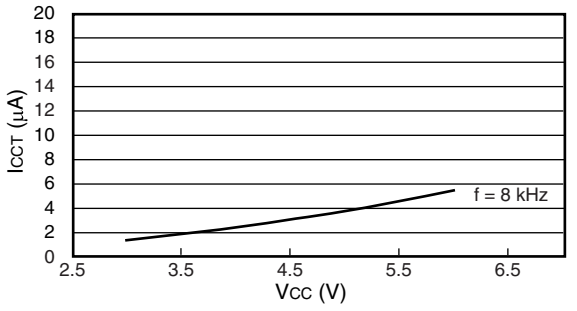
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



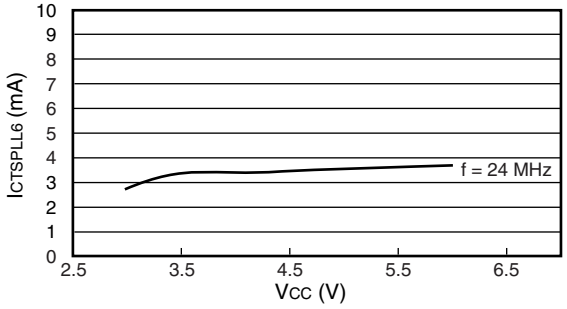
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



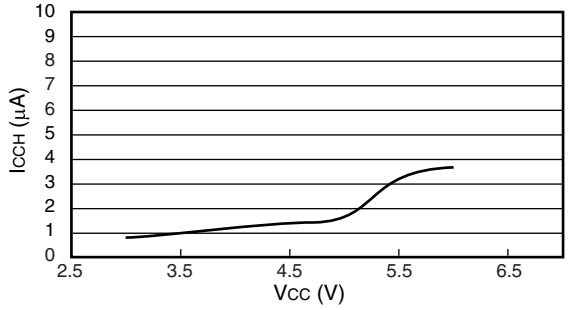
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency

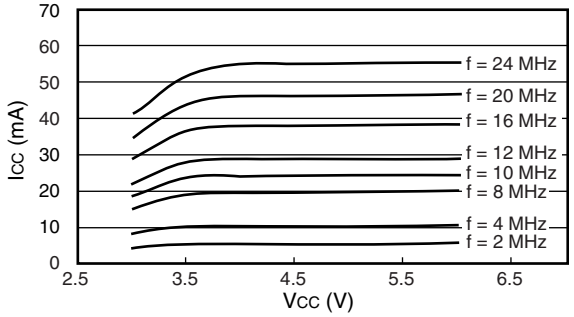


$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

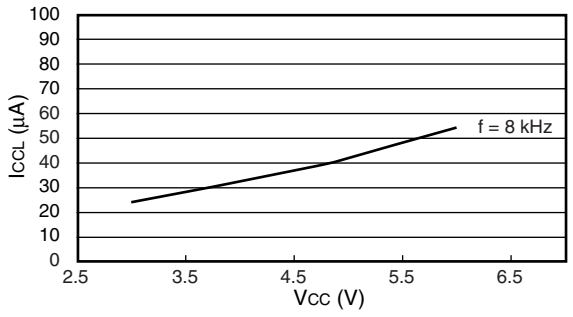


■ MB90347E, MB90347ES, MB90347CE, MB90347CES

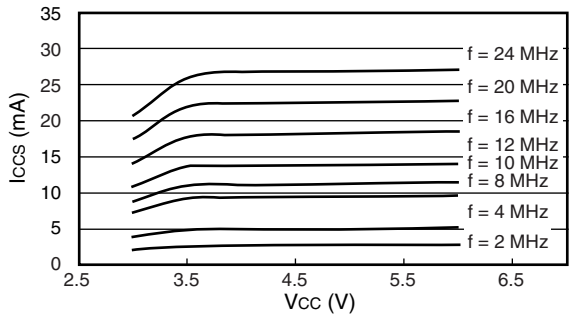
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



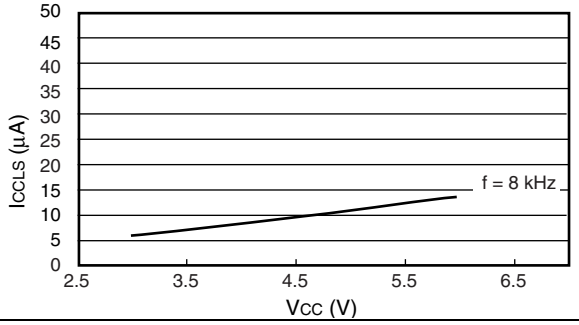
$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



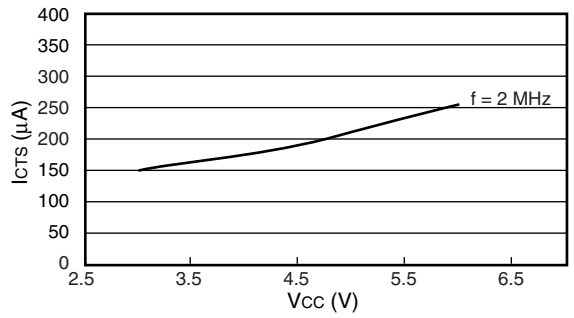
$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



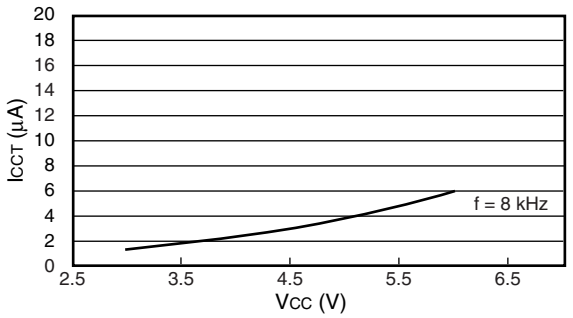
$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



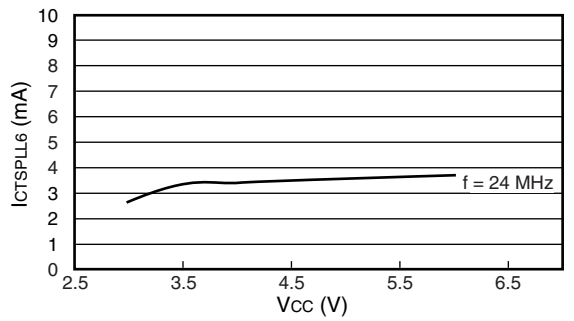
$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



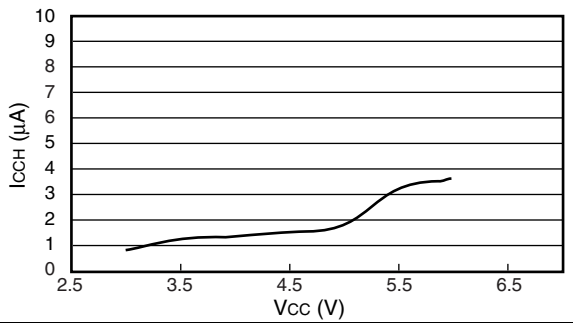
$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

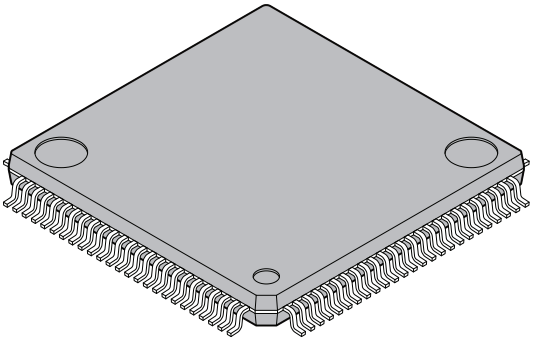


13. Ordering Information

Part number	Package	Remarks
MB90F342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F342ESPF		
MB90F342CEPF		
MB90F342CESPF		
MB90F342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F342ESPMC		
MB90F342CEPMC		
MB90F342CESPMC		
MB90F345EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F345ESPF		
MB90F345CEPF		
MB90F345CESPF		
MB90F345EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F345ESPMC		
MB90F345CEPMC		
MB90F345CESPMC		
MB90F346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F346ESPF		
MB90F346CEPF		
MB90F346CESPF		
MB90F346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F346ESPMC		
MB90F346CEPMC		
MB90F346CESPMC		

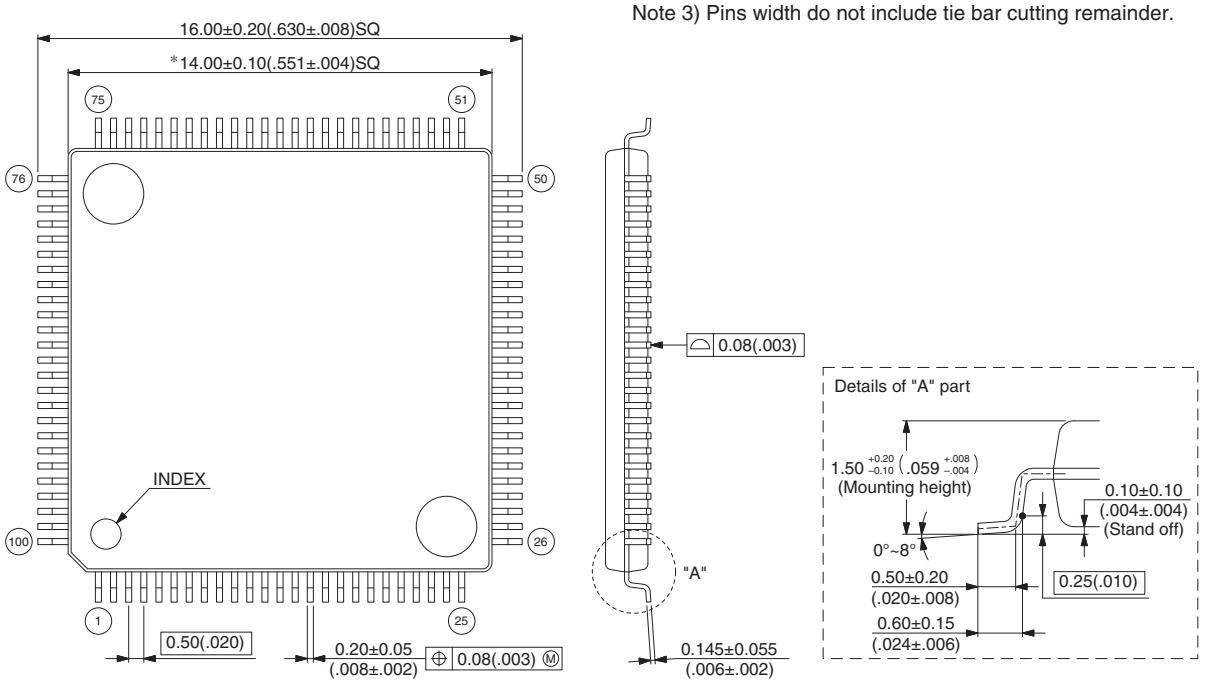
(Continued)

14. Package Dimensions

100-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
(FPT-100P-M20)	Code (Reference)	P-LFQFP100-14×14-0.50

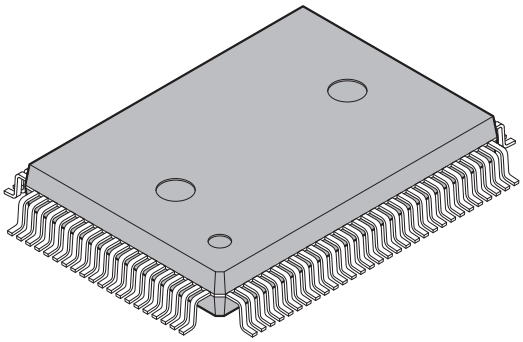
100-pin plastic LQFP
(FPT-100P-M20)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



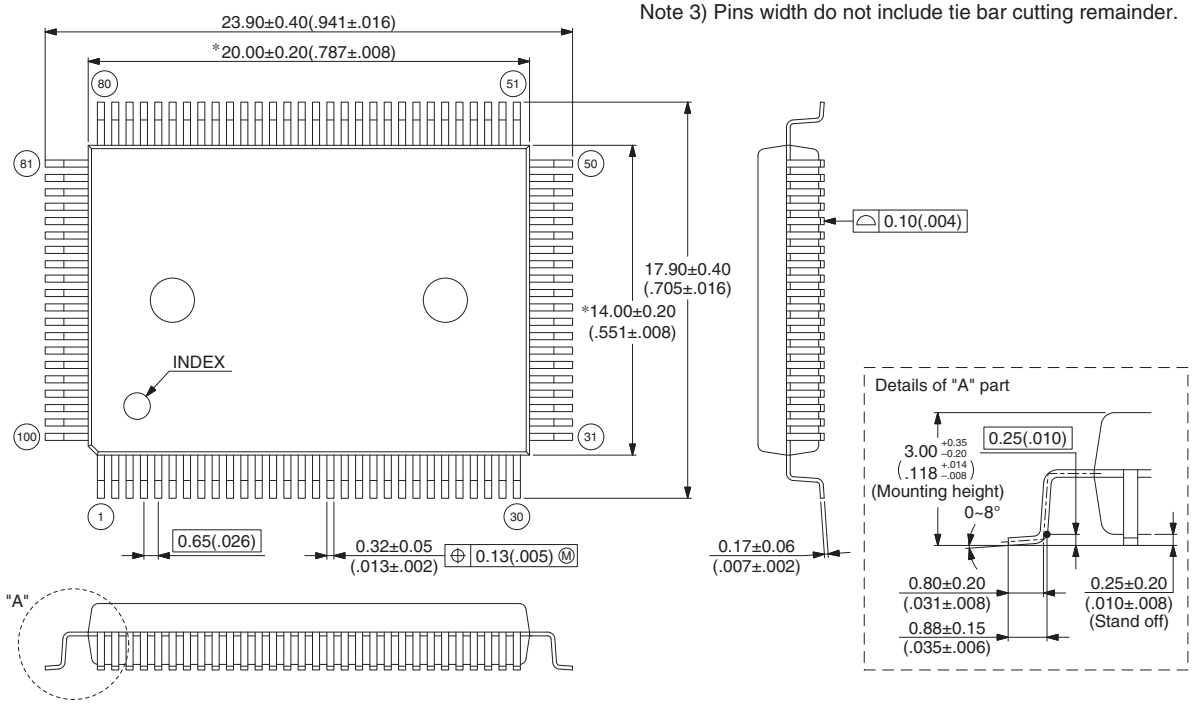
Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

100-pin plastic QFP		
	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65
(FPT-100P-M06)		

100-pin plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.