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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 24MHz |
| Connectivity | CANbus, EBI/EMI, LINbus, SCI, UART/USART |
| Peripherals | DMA, POR, WDT |
| Number of I/O | 82 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 6K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3.5V ~ 5.5V |
| Data Converters | A/D 16x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90f347espmc-gs-er |

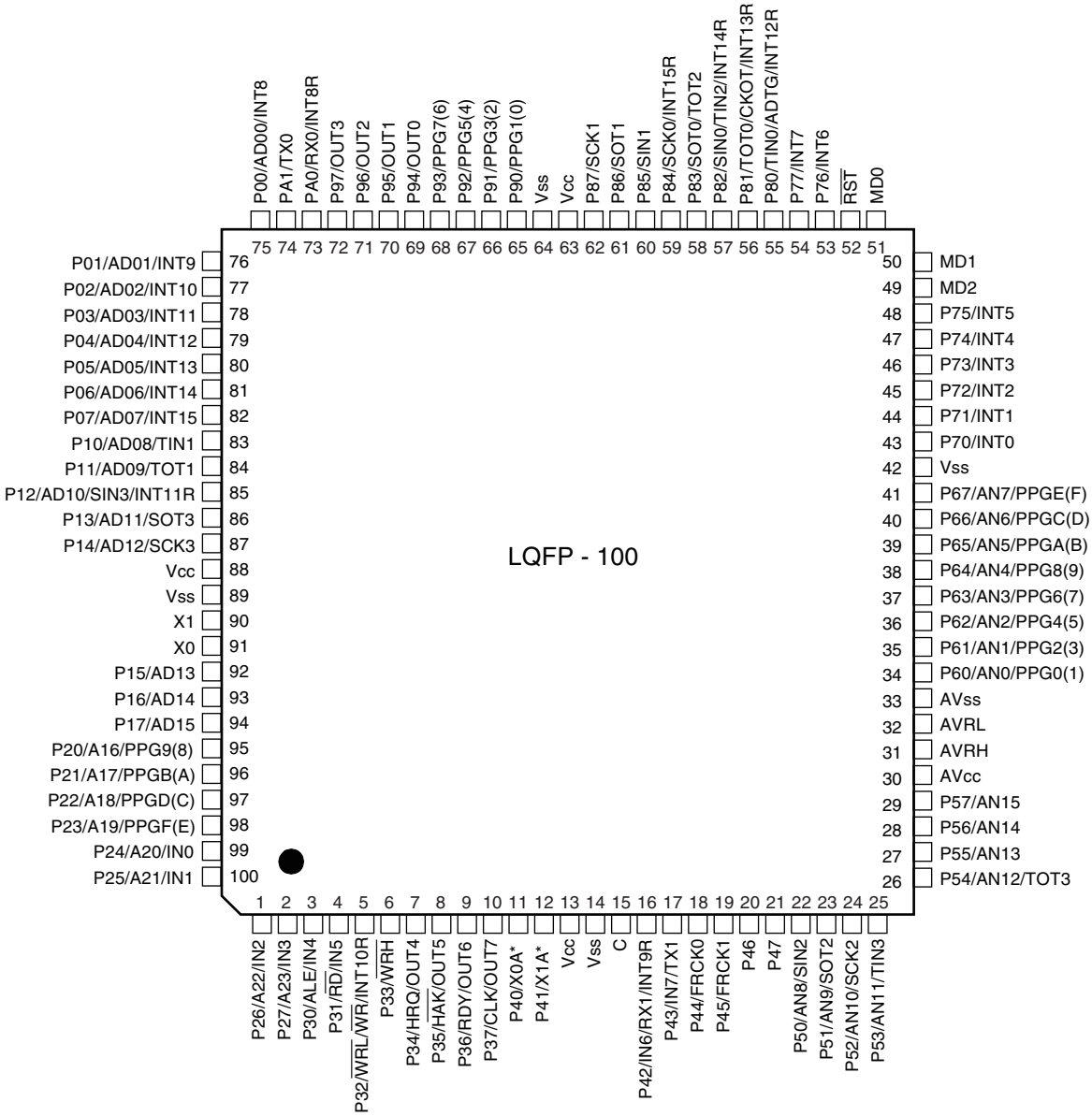
## 1. Product Lineup

| Part Number / Parameter | MB90V340E-101, MB90V340E-102 | MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S) | MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) |
|---|---|---|---|
| Type | Evaluation products | Flash memory products | MASK ROM products |
| CPU | $F^2$MC-16LX CPU | | |
| System clock | On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops)<br>Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6) | | |
| ROM | External | 512 Kbytes :<br>MB90F345E(S), MB90F345CE(S)<br>256 Kbytes :<br>MB90F342E(S), MB90F342CE(S),<br>MB90F349E(S), MB90F349CE(S)<br>128 Kbytes :<br>MB90F347E(S), MB90F347CE(S)<br>64 Kbytes :<br>MB90F346E(S), MB90F346CE(S) | 256 Kbytes :<br>MB90342E(S), MB90342CE(S),<br>MB90349E(S), MB90349CE(S)<br>128 Kbytes :<br>MB90341E(S), MB90341CE(S),<br>MB90347E(S), MB90347CE(S),<br>MB90348E(S), MB90348CE(S)<br>64 Kbytes :<br>MB90346E(S), MB90346CE(S) |
| RAM | 30 Kbytes | 20 Kbytes :<br>MB90F345E(S), MB90F345CE(S)<br>16 Kbytes :<br>MB90F342E(S), MB90F342CE(S),<br>MB90F349E(S), MB90F349CE(S)<br>6 Kbytes :<br>MB90F347E(S), MB90F347CE(S)<br>2 Kbytes :<br>MB90F346E(S), MB90F346CE(S) | 16 Kbytes :<br>MB90341E(S), MB90341CE(S),<br>MB90342E(S), MB90342CE(S),<br>MB90348E(S), MB90348CE(S),<br>MB90349E(S), MB90349CE(S)<br>6 Kbytes :<br>MB90347E(S), MB90347CE(S)<br>2 Kbytes :<br>MB90346E(S), MB90346CE(S) |
| Emulator-specific power supply* | Yes | — | |
| Technology | 0.35 μm CMOS with regulator for built-in power supply | 0.35 μm CMOS with built-in power supply regulator + Flash memory with Charge pump for programming voltage | |
| Operating voltage range | 5 V ± 10% | 3.5 V to 5.5 V : When normal operating (not using A/D converter)<br>4.0 V to 5.5 V : When using the A/D converter/Flash programming<br>4.5 V to 5.5 V : When using the external bus | |
| Temperature range | — | −40°C to +105°C | |
| Package | PGA-299 | QFP-100, LQFP-100 | |
| LIN-UART | 5 channels | 4 channels | |
| | Wide range of baud rate settings using a dedicated baud rate generator (reload timer)<br>Special synchronous options for adapting to different synchronous serial protocols<br>LIN functionality working either as master or slave LIN device | | |
| $I^2C$ (400 kbps) | 2 channels | Devices with a C suffix in the part number : 2 channels<br>Devices without a C suffix in the part number : — | |

*(Continued)*

*(Continued)*

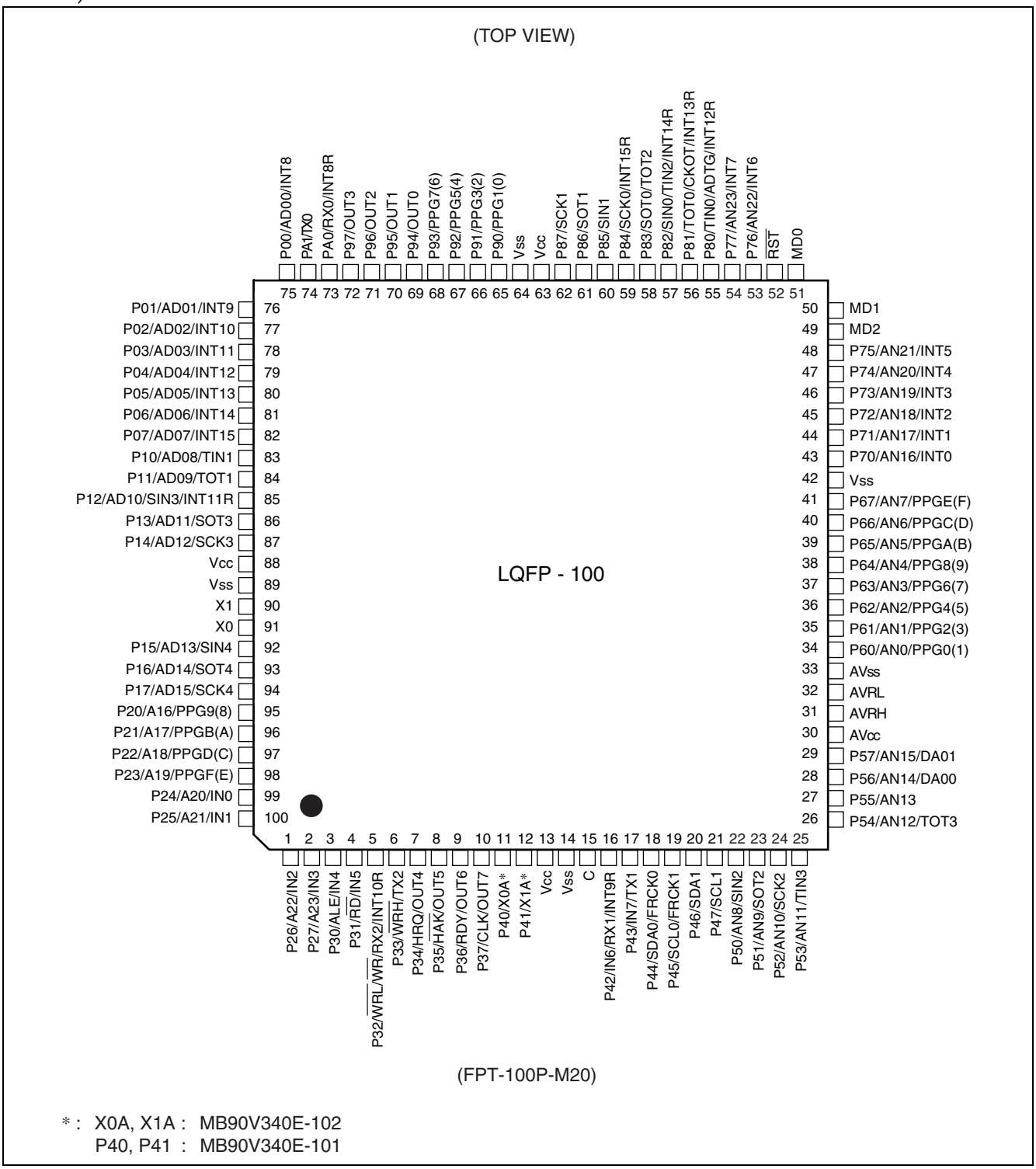
(TOP VIEW)




(FPT-100P-M20)

* : X0A, X1A : devices without an S suffix in the part number
P40, P4 : devices with an S suffix in the part number

*(Continued)*




This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 9 | 7 | P34 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled. |
| | | HRQ | | Hold request input pin. This function is enabled when both the external bus and the hold function are enabled. |
| | | OUT4 | | Waveform output pin for output compare. |
| 10 | 8 | P35 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the hold function is disabled. |
| | | $\overline{\text{HAK}}$ | | Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled. |
| | | OUT5 | | Waveform output pin for output compare. |
| 11 | 9 | P36 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled. |
| | | RDY | | External ready input pin. This function is enabled when both the external bus and the external ready function are enabled. |
| | | OUT6 | | Waveform output pin for output compare. |
| 12 | 10 | P37 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the clock output is disabled. |
| | | CLK | | Clock output pin. This function is enabled when both the external bus and clock output are enabled. |
| | | OUT7 | | Waveform output pin for output compare |
| 13, 14 | 11, 12 | P40, P41 | F | General purpose I/O pins. (devices with an S suffix in the part number and or MB90V340E-101) |
| | | X0A, X1A | B | Oscillation pins for sub clock (devices without an S suffix in the part number and or MB90V340E-102) |
| 15 | 13 | $V_{CC}$ | — | Power (3.5 V to 5.5 V) input pin |
| 16 | 14 | $V_{SS}$ | — | GND pin |
| 17 | 15 | C | K | This is the power supply stabilization capacitor This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 µF. |
| 18 | 16 | P42 | F | General purpose I/O pin. |
| | | IN6 | | Trigger input pin for input capture. |
| | | RX1 | | RX input pin for CAN1 Interface (MB90341E/342E/F342E/F345E only) |
| | | INT9R | | External interrupt request input pin |

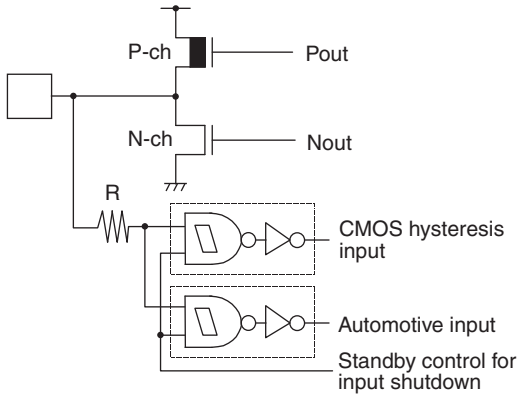
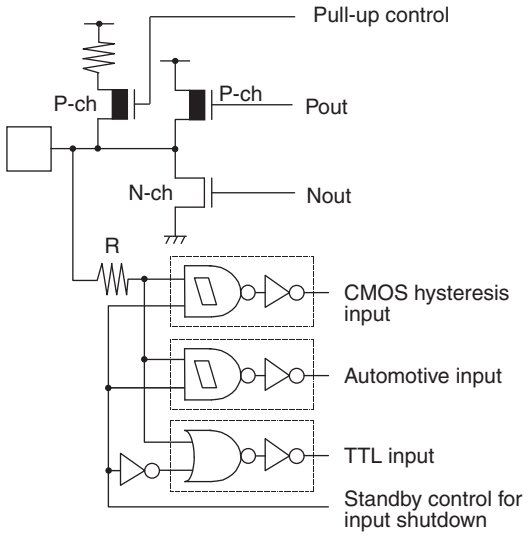
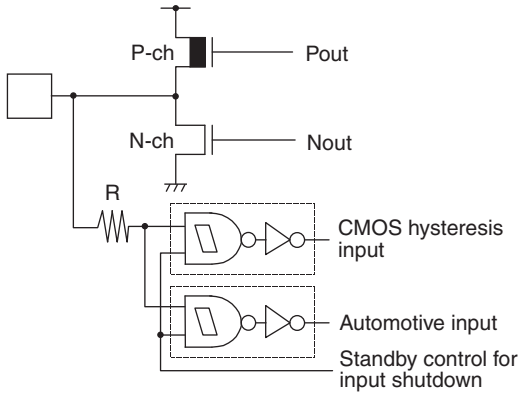
*(Continued)*

| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 33 | 31 | AVRH | L | Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to $AV_{CC}$. |
| 34 | 32 | AVRL | K | Lower reference voltage input pin for the A/D Converter |
| 35 | 33 | $AV_{SS}$ | K | Analog GND pin for the A/D Converter |
| 36 to 43 | 34 to 41 | P60 to P67 | I | General purpose I/O pins. |
| | | AN0 to AN7 | | Analog input pins for the A/D converter |
| | | PPG0, 2, 4, 6, 8, A, C, E | | Output pins for PPGs |
| 44 | 42 | $V_{SS}$ | — | GND pin |
| 45 to 50 | 43 to 48 | P70 to P75 | I | General purpose I/O pins. |
| | | AN16 to AN21 | | Analog input pins for the A/D converter (devices with a C suffix in the part number) |
| | | INT0 to INT5 | | External interrupt request input pins |
| 51 | 49 | MD2 | D | Input pin for specifying the operating mode. |
| 52, 53 | 50, 51 | MD1, MD0 | C | Input pins for specifying the operating mode. |
| 54 | 52 | $\overline{RST}$ | E | Reset input pin |
| 55, 56 | 53, 54 | P76, P77 | I | General purpose I/O pins. |
| | | AN22, AN23 | | Analog input pins for the A/D converter (devices with a C suffix in the part number) |
| | | INT6, INT7 | | External interrupt request input pins |
| 57 | 55 | P80 | F | General purpose I/O pin. |
| | | TIN0 | | Event input pin for the reload timer |
| | | ADTG | | Trigger input pin for the A/D converter |
| | | INT12R | | External interrupt request input pin |
| 58 | 56 | P81 | F | General purpose I/O pin. |
| | | TOT0 | | Output pin for the reload timer |
| | | CKOT | | Output pin for the clock monitor |
| | | INT13R | | External interrupt request input pin |
| 59 | 57 | P82 | M | General purpose I/O pin. |
| | | SIN0 | | Serial data input pin for UART0 |
| | | TIN2 | | Event input pin for the reload timer |
| | | INT14R | | External interrupt request input pin |
| 60 | 58 | P83 | F | General purpose I/O pin. |
| | | SOT0 | | Serial data output pin for UART0 |
| | | TOT2 | | Output pin for the reload timer |

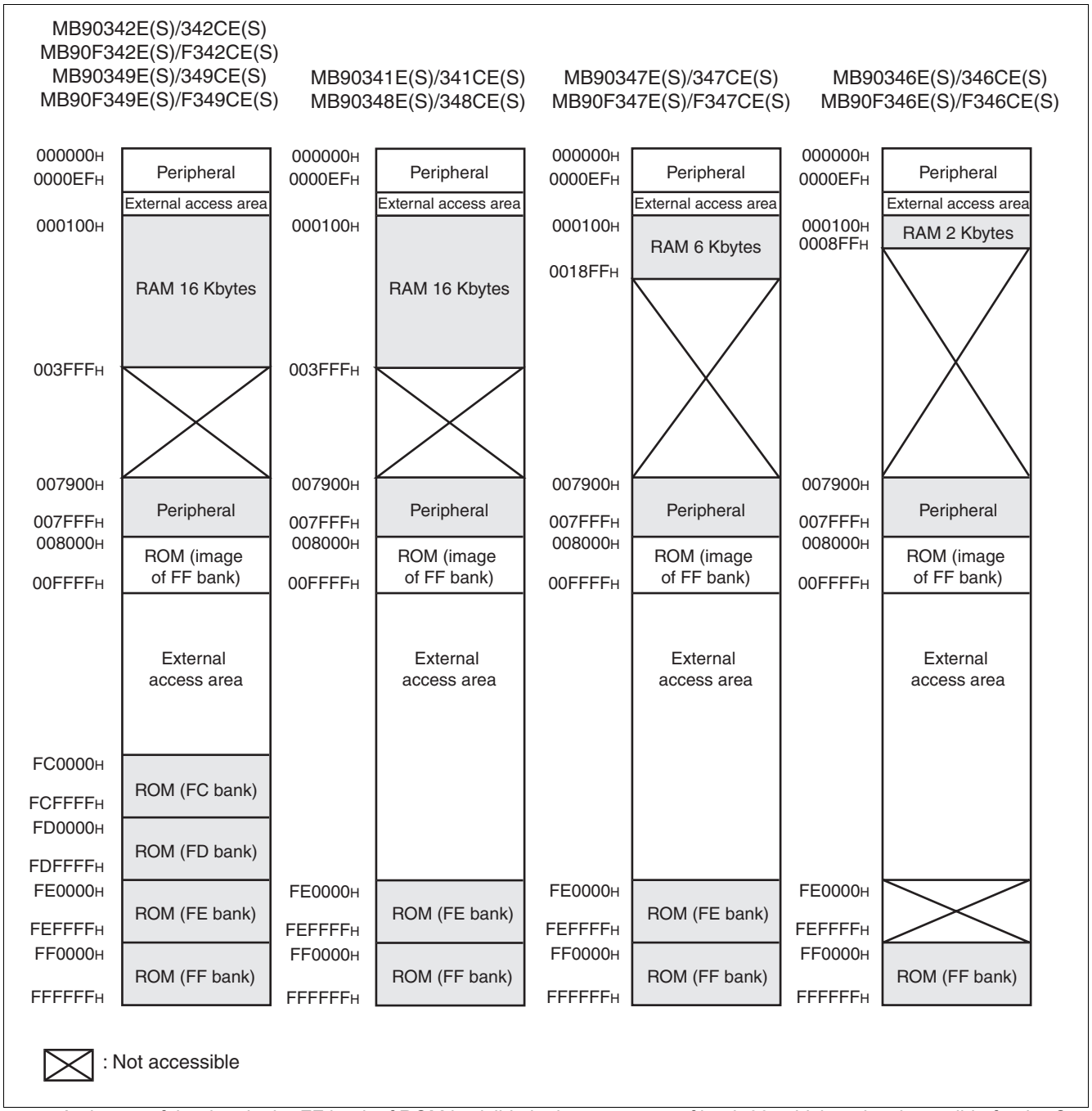
*(Continued)*

| Pin No. | | Pin name | I/O Circuit type*3 | Function |
|---|---|---|---|---|
| QFP100*1 | LQFP100*2 | | | |
| 86 | 84 | P11 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD09 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| | | TOT1 | | Output pin for the reload timer |
| 87 | 85 | P12 | N | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD10 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| | | SIN3 | | Serial data input pin for UART3 |
| | | INT11R | | External interrupt request input pin |
| 88 | 86 | P13 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD11 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| | | SOT3 | | Serial data output pin for UART3 |
| 89 | 87 | P14 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD12 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| | | SCK3 | | Clock I/O pin for UART3 |
| 90 | 88 | $V_{CC}$ | — | Power (3.5 V to 5.5 V) input pin |
| 91 | 89 | $V_{SS}$ | — | GND pin |
| 92 | 90 | X1 | A | Main clock output pin |
| 93 | 91 | X0 | | Main clock input pin |
| 94 | 92 | P15 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD13 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |
| 95 | 93 | P16 | G | General purpose I/O pin. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode. |
| | | AD14 | | I/O pin for the external address/data bus. This function is enabled when the external bus is enabled. |

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| F |  | ■ CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>■ CMOS hysteresis input (with function to disconnect input during standby)<br>■ Automotive input (with function to disconnect input during standby) |
| G |  | ■ CMOS level output ($I_{OL}$ = 4 mA, $I_{OH}$ = –4 mA)<br>■ CMOS hysteresis input (with function to disconnect input during standby)<br>■ Automotive input (with function to disconnect input during standby)<br>■ TTL input (with function to disconnect input during standby)<br>■ Programmable pull-up resistor: 50 kΩ approx. |
| H |  | ■ CMOS level output ($I_{OL}$ = 3 mA, $I_{OH}$ = –3 mA)<br>■ CMOS hysteresis input (with function to disconnect input during standby)<br>■ Automotive input (with function to disconnect input during standby) |

*(Continued)*




**Note:** :An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration.
For example, when the address $00C000_H$ is accessed, the data at $FFC000_H$ in ROM is actually accessed.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
As a result, the image between $FF8000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF7FFF_H$ is visible only in bank FF.

| Address | Register | Abbreviation | Access | Resource name | Initial value |
|---|---|---|---|---|---|
| $0000A5_H$ | Automatic Ready Function Select Register | ARSR | W | External Memory Access | $0011XX00_B$ |
| $0000A6_H$ | External Address Output Control Register | HACR | W | | $00000000_B$ |
| $0000A7_H$ | Bus Control Signal Selection Register | ECSR | W | | $0000000X_B$ |
| $0000A8_H$ | Watchdog Control Register | WDTC | R,W | Watchdog Timer | $XXXXX111_B$ |
| $0000A9_H$ | Time Base Timer Control Register | TBTC | W,R/W | Time Base Timer | $1XX00100_B$ |
| $0000AA_H$ | Watch Timer Control Register | WTC | R,R/W | Watch Timer | $1X001000_B$ |
| $0000AB_H$ | Reserved | | | | |
| $0000AC_H$ | DMA Enable L Register | DERL | R/W | DMA | $00000000_B$ |
| $0000AD_H$ | DMA Enable H Register | DERH | R/W | | $00000000_B$ |
| $0000AE_H$ | Flash Control Status Register (Flash memory devices only. Otherwise reserved) | FMCS | R,R/W | Flash Memory | $000X0000_B$ |
| $0000AF_H$ | Reserved | | | | |
| $0000B0_H$ | Interrupt Control Register 00 | ICR00 | W,R/W | Interrupt Control | $00000111_B$ |
| $0000B1_H$ | Interrupt Control Register 01 | ICR01 | W,R/W | | $00000111_B$ |
| $0000B2_H$ | Interrupt Control Register 02 | ICR02 | W,R/W | | $00000111_B$ |
| $0000B3_H$ | Interrupt Control Register 03 | ICR03 | W,R/W | | $00000111_B$ |
| $0000B4_H$ | Interrupt Control Register 04 | ICR04 | W,R/W | | $00000111_B$ |
| $0000B5_H$ | Interrupt Control Register 05 | ICR05 | W,R/W | | $00000111_B$ |
| $0000B6_H$ | Interrupt Control Register 06 | ICR06 | W,R/W | | $00000111_B$ |
| $0000B7_H$ | Interrupt Control Register 07 | ICR07 | W,R/W | | $00000111_B$ |
| $0000B8_H$ | Interrupt Control Register 08 | ICR08 | W,R/W | | $00000111_B$ |
| $0000B9_H$ | Interrupt Control Register 09 | ICR09 | W,R/W | | $00000111_B$ |
| $0000BA_H$ | Interrupt Control Register 10 | ICR10 | W,R/W | | $00000111_B$ |
| $0000BB_H$ | Interrupt Control Register 11 | ICR11 | W,R/W | | $00000111_B$ |
| $0000BC_H$ | Interrupt Control Register 12 | ICR12 | W,R/W | | $00000111_B$ |
| $0000BD_H$ | Interrupt Control Register 13 | ICR13 | W,R/W | | $00000111_B$ |
| $0000BE_H$ | Interrupt Control Register 14 | ICR14 | W,R/W | | $00000111_B$ |
| $0000BF_H$ | Interrupt Control Register 15 | ICR15 | W,R/W | | $00000111_B$ |
| $0000C0_H$ | D/A Converter Data 0 | DAT0 | R/W | D/A Converter | $XXXXXXXX_B$ |
| $0000C1_H$ | D/A Converter Data 1 | DAT1 | R/W | | $XXXXXXXX_B$ |
| $0000C2_H$ | D/A Control 0 | DACR0 | R/W | | $XXXXXXX0_B$ |
| $0000C3_H$ | D/A Control 1 | DACR1 | R/W | | $XXXXXXX0_B$ |

*(Continued)*

**List of Message Buffers (DLC Registers and Data Registers) (3)**

| Address | | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|---|
| CAN0 | CAN1 | | | | |
| $007AF0_H$ to $007AF7_H$ | $007CF0_H$ to $007CF7_H$ | Data Register 14 (8 bytes) | DTR14 | R/W | $XXXXXXXX_B$ to $XXXXXXXX_B$ |
| $007AF8_H$ to $007AFF_H$ | $007CF8_H$ to $007CFF_H$ | Data Register 15 (8 bytes) | DTR15 | R/W | $XXXXXXXX_B$ to $XXXXXXXX_B$ |

## 11.4 AC Characteristics

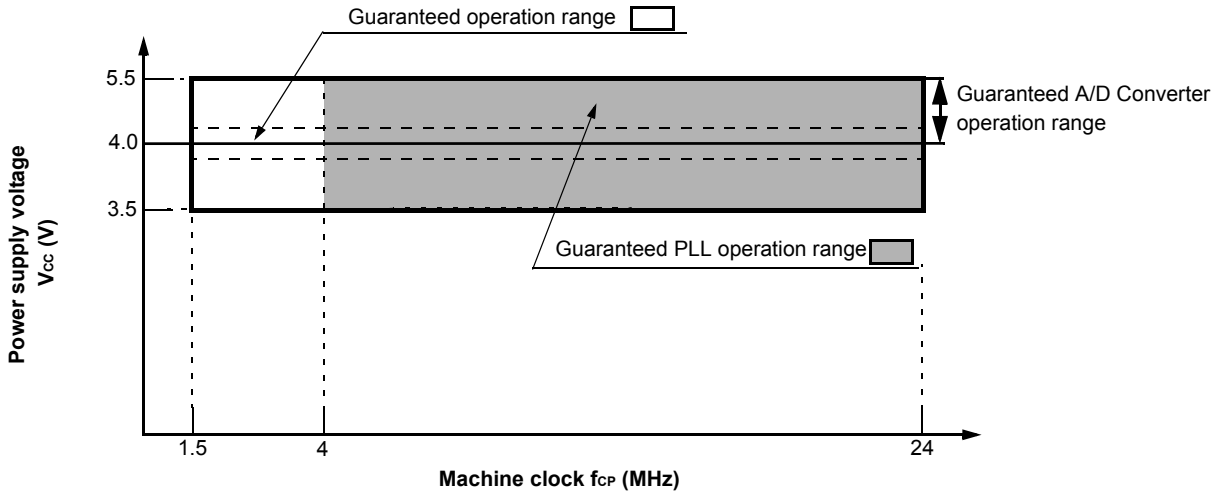
### *11.4.1 Clock Timing*

($T_A$ = –40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$≤ 24 MHz, $V_{SS}$ = $AV_{SS}$ = 0 V)

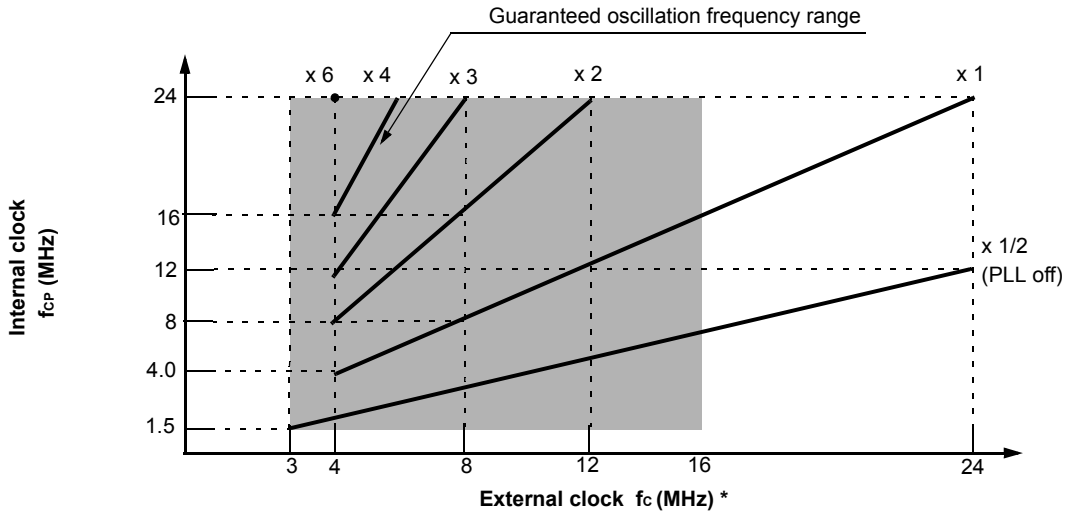
| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $f_C$ | X0, X1 | 3 | — | 16 | MHz | When using an oscillation circuit |
| | | | 4 | — | 16 | MHz | PLL multiplied by 1<br>When using an oscillation circuit |
| | | | 4 | — | 12 | MHz | PLL multiplied by 2<br>When using an oscillation circuit |
| | | | 4 | — | 8 | MHz | PLL multiplied by 3<br>When using an oscillation circuit |
| | | | 4 | — | 6 | MHz | PLL multiplied by 4<br>When using an oscillation circuit |
| | | | — | — | 4 | MHz | PLL multiplied by 6<br>When using an oscillation circuit |
| | | | 3 | — | 24 | MHz | When using an external clock* |
| | $f_{CL}$ | X0A, X1A | — | 32.768 | 100 | kHz | |
| Clock cycle time | $t_{CYL}$ | X0, X1 | 62.5 | — | 333 | ns | When using an oscillation circuit |
| | | X0, X1 | 41.67 | — | 333 | ns | When using an external clock |
| | $t_{CYLL}$ | X0A, X1A | 10 | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | 10 | — | — | ns | Duty ratio is about 30% to 70%. |
| | $P_{WHL}$, $P_{WLL}$ | X0A | 5 | 15.2 | — | µs | |
| Input clock rise and fall time | $t_{CR}$, $t_{CF}$ | X0 | — | — | 5 | ns | When using external clock |
| Internal operating clock frequency (machine clock) | $f_{CP}$ | — | 1.5 | — | 24 | MHz | When using main clock |
| | $f_{CPL}$ | — | — | 8.192 | 50 | kHz | When using sub clock |
| Internal operating clock cycle time (machine clock) | $t_{CP}$ | — | 41.67 | — | 666 | ns | When using main clock |
| | $t_{CPL}$ | — | 20 | 122.1 | — | µs | When using sub clock |

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in “Relation between the external clock frequency and machine clock frequency”.

Guaranteed PLL operation range




**Guaranteed operation range of MB90340E series**




* : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

*11.4.9 LIN-UART0/1/2/3*

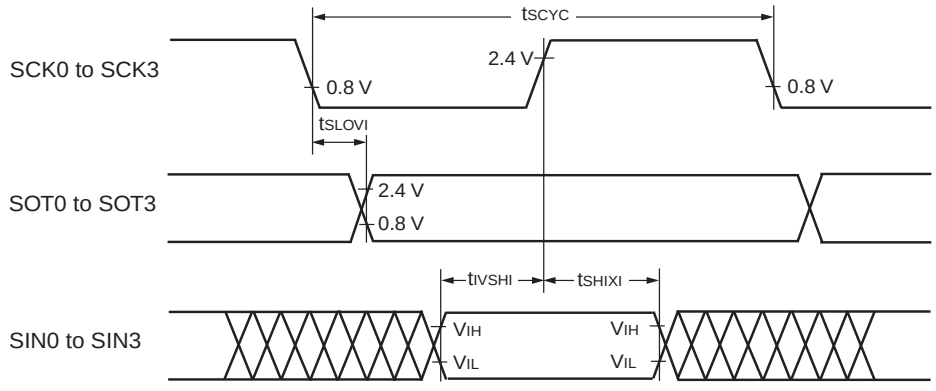
■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0**

($T_A$ = −40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal shift clock mode output pins are $C_L$ = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | −50 | +50 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXI}$ | SCK0 to SCK3, SIN0 to SIN3 | | 0 | — | ns |
| Serial clock “L” pulse width | $t_{SHSL}$ | SCK0 to SCK3 | External shift clock mode output pins are $C_L$ = 80 pF + 1 TTL. | 3 $t_{CP}$ - $t_R$ | — | ns |
| Serial clock “H” pulse width | $t_{SLSH}$ | SCK0 to SCK3 | | $t_{CP}$ + 10 | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCK0 to SCK3, SOT0 to SOT3 | | — | 2 $t_{CP}$ + 60 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHE}$ | SCK0 to SCK3, SIN0 to SIN3 | | 30 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXE}$ | SCK0, SCK1, SIN0 to SIN3 | | $t_{CP}$ + 30 | — | ns |
| SCK fall time | $t_F$ | SCK0 to SCK3 | | — | 10 | ns |
| SCK rise time | $t_R$ | SCK0 to SCK3 | | — | 10 | ns |

**Note:**
- AC characteristic in CLK synchronized mode.
- $C_L$ is load capacity value of pins when testing.
- $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

- Internal Shift Clock Mode

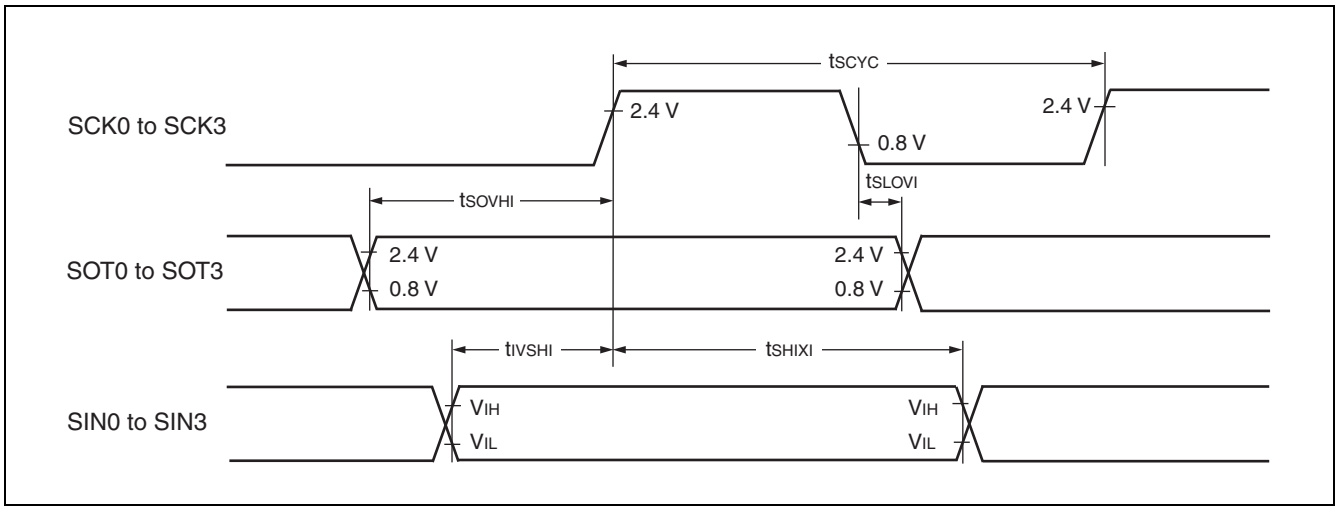


■ **Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1**

($T_A$ = −40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK3 | Internal clock operation output pins are $C_L$ = 80 pF + 1 TTL. | 5 $t_{CP}$ | — | ns |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0 to SCK3, SOT0 to SOT3 | | −50 | +50 | ns |
| Valid SIN → SCK ↑ | $t_{IVSHI}$ | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP}$ + 80 | — | ns |
| SCK ↑ → Valid SIN hold time | $t_{SHIXI}$ | SCK0 to SCK3, SIN0 to SIN3 | | 0 | — | ns |
| SOT → SCK ↑ delay time | $t_{SOVHI}$ | SCK0 to SCK3, SOT0 to SOT3 | | 3 $t_{CP}$ − 70 | — | ns |

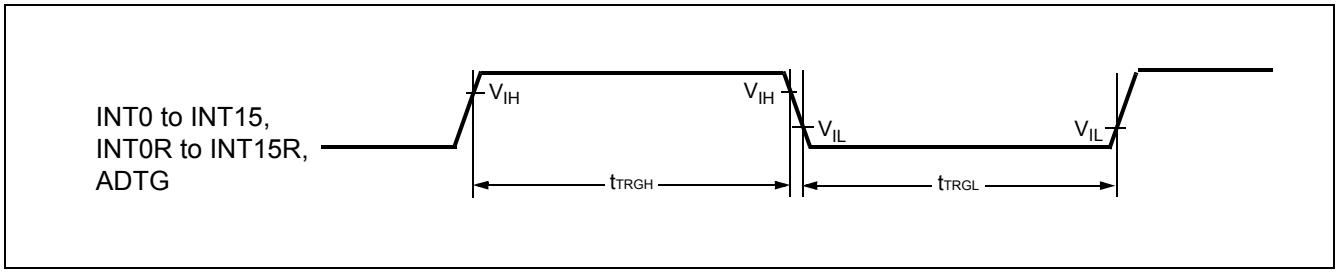
**Note:**
- $C_L$ is load capacity value of pins when testing.
- $t_{CP}$ is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".



### 11.4.10 Trigger Input Timing

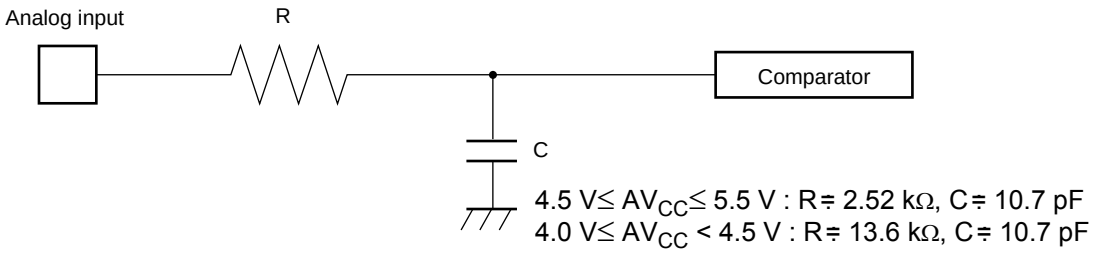
($T_A$ = −40°C to +105°C, $V_{CC}$ = 5.0 V ± 10%, $f_{CP}$ ≤ 24 MHz, $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | INT0 to INT15,<br>INT0R to INT15R,<br>ADTG | — | 5 $t_{CP}$ | — | ns |



If the output impedance of the external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model

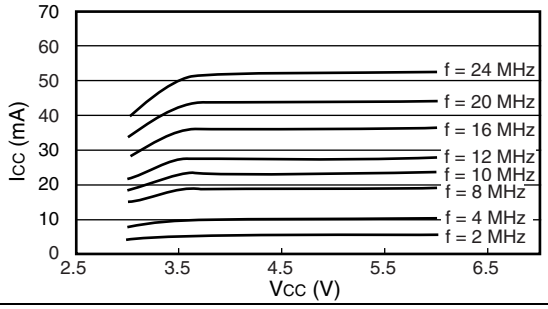



**Note:** : Use the values in the figure only as a guideline.

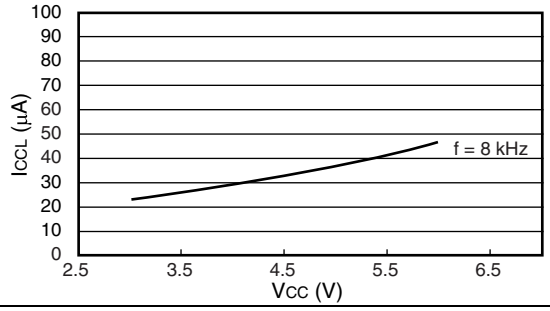
## 12. Example Characteristics

- MB90F346E, MB90F346ES, MB90F346CE, MB90F346CES

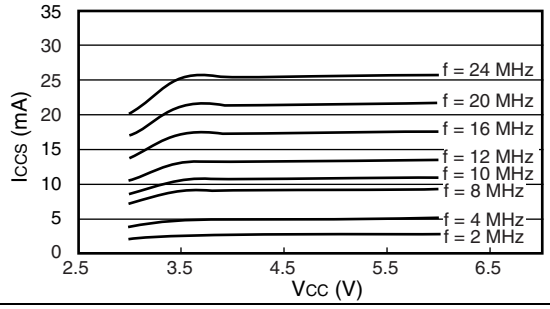
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



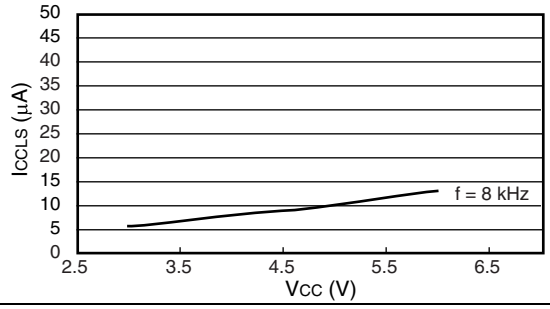

$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



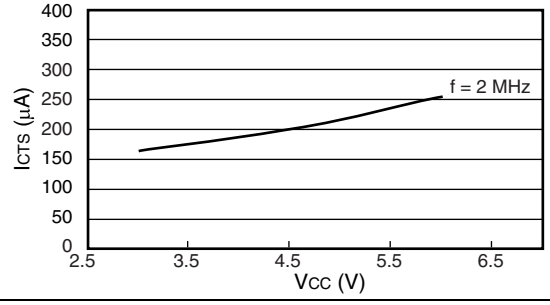

$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



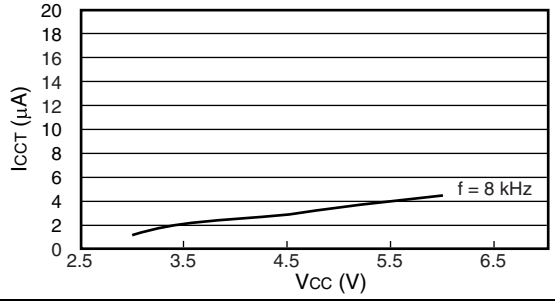

$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



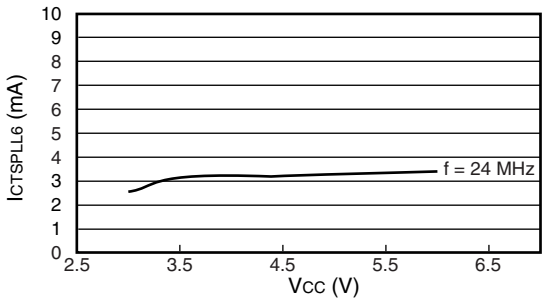

$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency



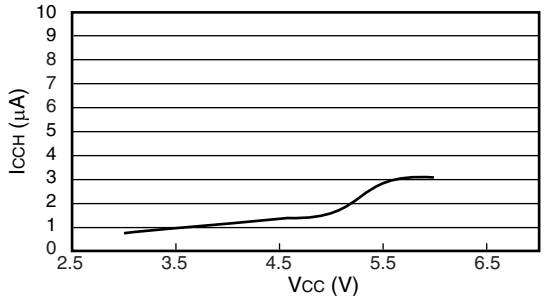

$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency




$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation, f = Internal operation frequency

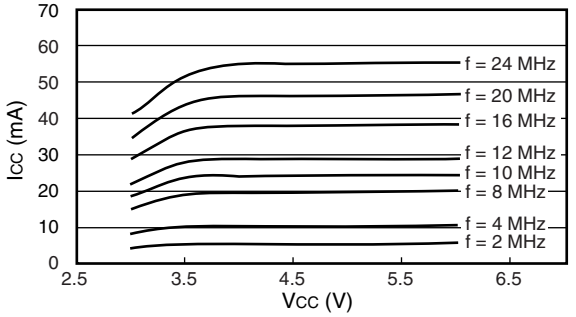



$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped

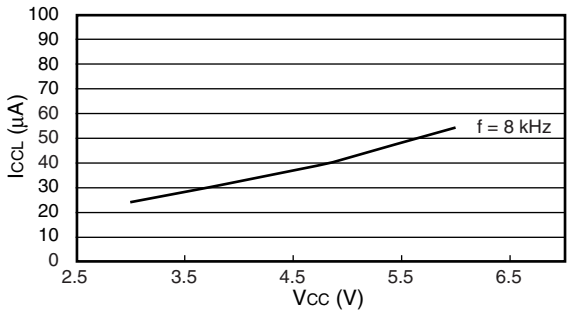


■ MB90346E, MB90346ES, MB90346CE, MB90346CES

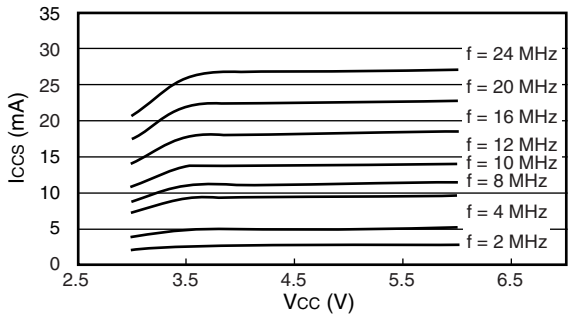
$I_{CC} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



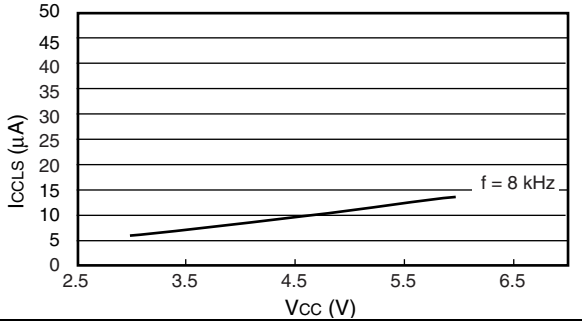

$I_{CCL} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



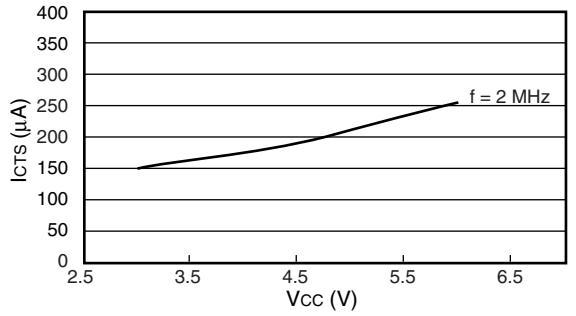

$I_{CCS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



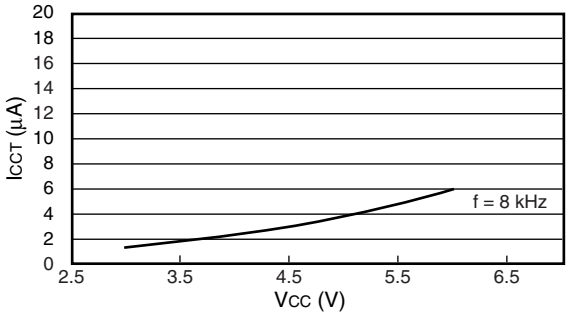

$I_{CCLS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



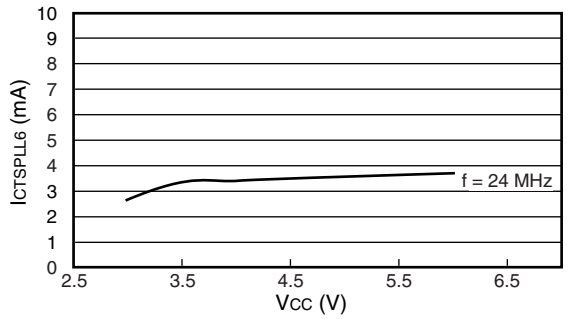

$I_{CTS} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency



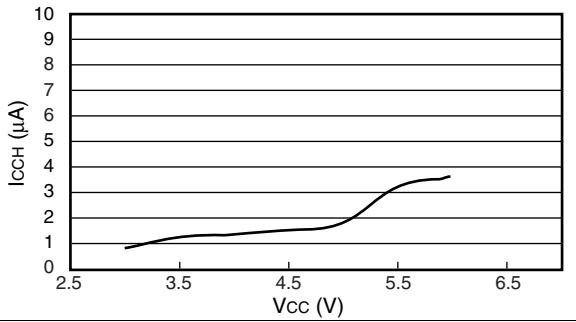

$I_{CCT} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency




$I_{CTSPLL6} - V_{CC}$
$T_A = +25°C$, external clock operation f = Internal operation frequency




$I_{CCH} - V_{CC}$
$T_A = +25°C$, stopped



## 13. Ordering Information

| Part number | Package | Remarks |
|---|---|---|
| MB90F342EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90F342ESPF | | |
| MB90F342CEPF | | |
| MB90F342CESPF | | |
| MB90F342EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90F342ESPMC | | |
| MB90F342CEPMC | | |
| MB90F342CESPMC | | |
| MB90F345EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90F345ESPF | | |
| MB90F345CEPF | | |
| MB90F345CESPF | | |
| MB90F345EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90F345ESPMC | | |
| MB90F345CEPMC | | |
| MB90F345CESPMC | | |
| MB90F346EPF | 100-pin plastic QFP (FPT-100P-M06) | |
| MB90F346ESPF | | |
| MB90F346CEPF | | |
| MB90F346CESPF | | |
| MB90F346EPMC | 100-pin plastic LQFP (FPT-100P-M20) | |
| MB90F346ESPMC | | |
| MB90F346CEPMC | | |
| MB90F346CESPMC | | |

*(Continued)*

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