Infineon Technologies - MB90F347ESPMC-GS-SPE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f347espmc-gs-spe1

Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
19	17	P43	F	General purpose I/O pin.
		IN7		Trigger input pin for input capture.
		TX1		TX Output pin for CAN1 (MB90341E/342E/F342E/F345E only)
20	18	P44	H	General purpose I/O pin.
		SDA0		Serial data I/O pin for I^2C (devices with a C suffix in the part number)
		FRCK0		Input pin for the 16-bit Free-run Timer 0
21	19	P45	H	General purpose I/O pin.
		SCL0		Serial clock I/O pin for I^2C (devices with a C suffix in the part number)
		FRCK1		Input pin for the 16-bit Free-run Timer
22	20	P46	H	General purpose I/O pin.
		SDA1		Serial data I/O pin for I^2C (devices with a C suffix in the part number)
23	21	P47	H	General purpose I/O pin.
		SCL1		Serial clock I/O pin for I^2C (devices with a C suffix in the part number)
24	22	P50	O	General purpose I/O pin.
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
25	23	P51	I	General purpose I/O pin.
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
26	24	P52	I	General purpose I/O pin.
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
27	25	P53	I	General purpose I/O pin.
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer
28	26	P54	I	General purpose I/O pin.
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer
29	27	P55	I	General purpose I/O pin.
		AN13		Analog input pin for the A/D converter
30, 31	28, 29	P56, P57	J	General purpose I/O pins.
		AN14, AN15		Analog input pins for the A/D converter
32	30	AV_{CC}	K	Analog power input pin for the A/D Converter

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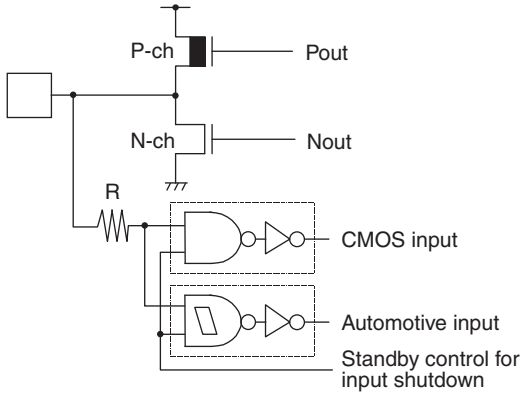
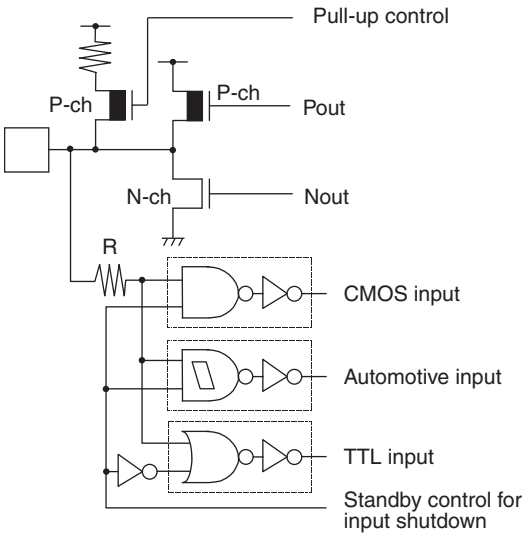
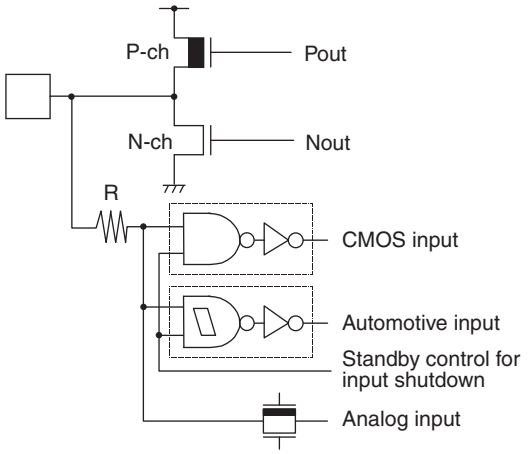
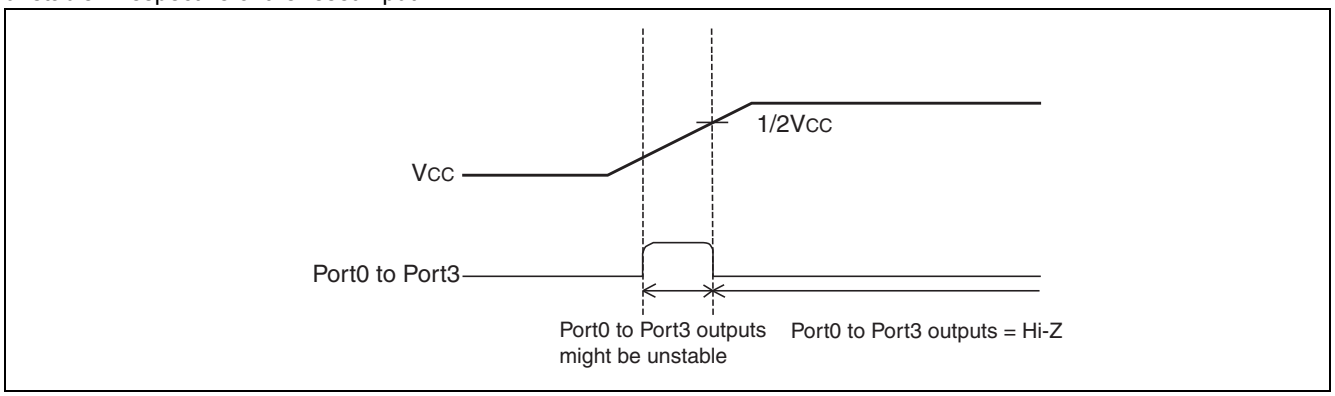
Type	Circuit	Remarks
M		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
N		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) Programmable pull-up resistor: 50 kΩ approx
O		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) ■ CMOS input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ A/D converter analog input

13.Stabilization of power supply voltage

A sudden change in the supply voltage may cause the device to malfunction even within the V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized. For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak- to-peak values) at commercial frequencies (50 MHz/60 MHz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

14.Port 0 to Port 3 Output During Power-on (External-bus Mode)

As shown below, when the power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable irrespective of the reset input.



15.Notes on Using the CAN Function

To use the CAN function, please set the DIRECT bit of the CAN Direct Mode Register (CDMR) to 1.

16.Flash Security Function (except for MB90F346E)

A security bit is located in the area of the flash memory.
If protection code 01_H is written in the security bit, the flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Refer to following table for the address of the security bit.

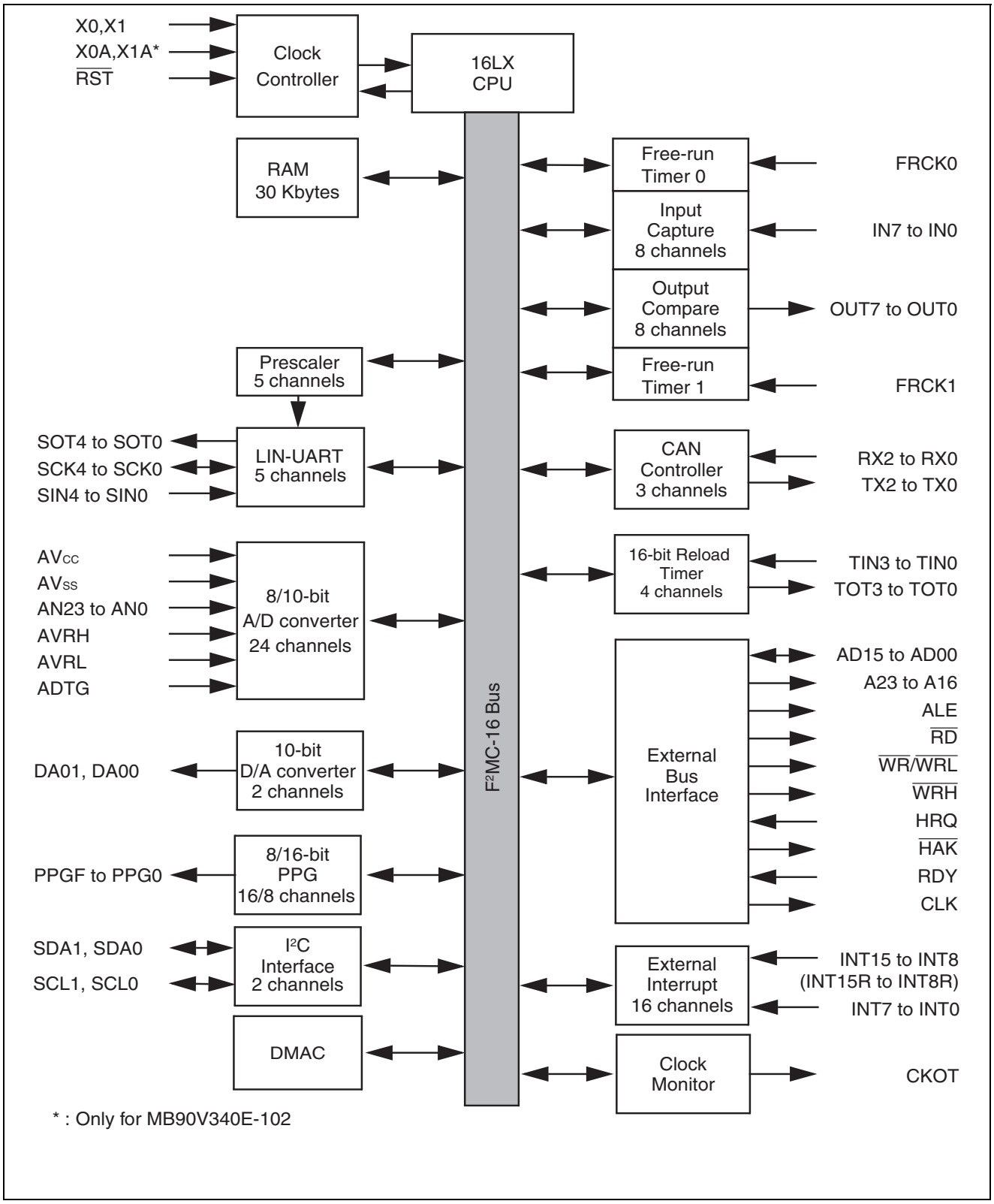
	Flash memory size	Address of the security bit
MB90F347E	Embedded 1 Mbit Flash Memory	$FE0001_H$
MB90F342E MB90F349E	Embedded 2 Mbits Flash Memory	$FC0001_H$
MB90F345E	Embedded 4 Mbits Flash Memory	$F80001_H$

17.Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Retransmit the data if an error occurs because of applying the checksum to the last data in consideration of receiving wrong data due to the noise.

6. Block Diagrams

- MB90V340E-101/102



Address	Register	Abbreviation	Access	Resource name	Initial value
000020_H	Serial Mode Register 0	SMR0	W,R/W	UART0	00000000_B
000021_H	Serial Control Register 0	SCR0	W,R/W		00000000_B
000022_H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000_B
000023_H	Serial Status Register 0	SSR0	R,R/W		00001000_B
000024_H	Extended Communication Control Register 0	ECCR0	R,W, R/W		$000000XX_B$
000025_H	Extended Status/Control Register 0	ESCR0	R/W		00000100_B
000026_H	Baud Rate Generator Register 00	BGR00	R/W		00000000_B
000027_H	Baud Rate Generator Register 01	BGR01	R/W		00000000_B
000028_H	Serial Mode Register 1	SMR1	W,R/W	UART1	00000000_B
000029_H	Serial Control Register 1	SCR1	W,R/W		00000000_B
$00002A_H$	Reception/Transmission Data Register 1	RDR1/TDR1	R/W		00000000_B
$00002B_H$	Serial Status Register 1	SSR1	R,R/W		00001000_B
$00002C_H$	Extended Communication Control Register 1	ECCR1	R,W, R/W		$000000XX_B$
$00002D_H$	Extended Status/Control Register 1	ESCR1	R/W		00000100_B
$00002E_H$	Baud Rate Generator Register 10	BGR10	R/W		00000000_B
$00002F_H$	Baud Rate Generator Register 11	BGR11	R/W		00000000_B
000030_H	PPG 0 Operation Mode Control Register	PPGC0	W,R/W	16-bit PPG 0/1	$0X000XX1_B$
000031_H	PPG 1 Operation Mode Control Register	PPGC1	W,R/W		$0X000001_B$
000032_H	PPG 0/PPG 1 Count Clock Select Register	PPG01	R/W		$000000X0_B$
000033_H	Reserved				
000034_H	PPG 2 Operation Mode Control Register	PPGC2	W,R/W	16-bit PPG 2/3	$0X000XX1_B$
000035_H	PPG 3 Operation Mode Control Register	PPGC3	W,R/W		$0X000001_B$
000036_H	PPG 2/PPG 3 Count Clock Select Register	PPG23	R/W		$000000X0_B$
000037_H	Reserved				
000038_H	PPG 4 Operation Mode Control Register	PPGC4	W,R/W	16-bit PPG 4/5	$0X000XX1_B$
000039_H	PPG 5 Operation Mode Control Register	PPGC5	W,R/W		$0X000001_B$
$00003A_H$	PPG 4/PPG 5 Clock Select Register	PPG45	R/W		$000000X0_B$
$00003B_H$	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000_B
$00003C_H$	PPG 6 Operation Mode Control Register	PPGC6	W,R/W	16-bit PPG 6/7	$0X000XX1_B$
$00003D_H$	PPG 7 Operation Mode Control Register	PPGC7	W,R/W		$0X000001_B$
$00003E_H$	PPG 6/PPG 7 Count Clock Control Register	PPG67	R/W		$000000X0_B$
$00003F_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007900_H	Reload Register L0	PRLL0	R/W	16-bit PPG 0/1	$XXXXXXXX_B$
007901_H	Reload Register H0	PRLH0	R/W		$XXXXXXXX_B$
007902_H	Reload Register L1	PRLL1	R/W		$XXXXXXXX_B$
007903_H	Reload Register H1	PRLH1	R/W		$XXXXXXXX_B$
007904_H	Reload Register L2	PRLL2	R/W	16-bit PPG 2/3	$XXXXXXXX_B$
007905_H	Reload Register H2	PRLH2	R/W		$XXXXXXXX_B$
007906_H	Reload Register L3	PRLL3	R/W		$XXXXXXXX_B$
007907_H	Reload Register H3	PRLH3	R/W		$XXXXXXXX_B$
007908_H	Reload Register L4	PRLL4	R/W	16-bit PPG 4/5	$XXXXXXXX_B$
007909_H	Reload Register H4	PRLH4	R/W		$XXXXXXXX_B$
$00790A_H$	Reload Register L5	PRLL5	R/W		$XXXXXXXX_B$
$00790B_H$	Reload Register H5	PRLH5	R/W		$XXXXXXXX_B$
$00790C_H$	Reload Register L6	PRLL6	R/W	16-bit PPG 6/7	$XXXXXXXX_B$
$00790D_H$	Reload Register H6	PRLH6	R/W		$XXXXXXXX_B$
$00790E_H$	Reload Register L7	PRLL7	R/W		$XXXXXXXX_B$
$00790F_H$	Reload Register H7	PRLH7	R/W		$XXXXXXXX_B$
007910_H	Reload Register L8	PRLL8	R/W	16-bit PPG 8/9	$XXXXXXXX_B$
007911_H	Reload Register H8	PRLH8	R/W		$XXXXXXXX_B$
007912_H	Reload Register L9	PRLL9	R/W		$XXXXXXXX_B$
007913_H	Reload Register H9	PRLH9	R/W		$XXXXXXXX_B$
007914_H	Reload Register LA	PRLLA	R/W	16-bit PPG A/B	$XXXXXXXX_B$
007915_H	Reload Register HA	PRLHA	R/W		$XXXXXXXX_B$
007916_H	Reload Register LB	PRLLB	R/W		$XXXXXXXX_B$
007917_H	Reload Register HB	PRLHB	R/W		$XXXXXXXX_B$
007918_H	Reload Register LC	PRLLC	R/W	16-bit PPG C/D	$XXXXXXXX_B$
007919_H	Reload Register HC	PRLHC	R/W		$XXXXXXXX_B$
$00791A_H$	Reload Register LD	PRLLD	R/W		$XXXXXXXX_B$
$00791B_H$	Reload Register HD	PRLHD	R/W		$XXXXXXXX_B$
$00791C_H$	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	$XXXXXXXX_B$
$00791D_H$	Reload Register HE	PRLHE	R/W		$XXXXXXXX_B$
$00791E_H$	Reload Register LF	PRLLF	R/W		$XXXXXXXX_B$
$00791F_H$	Reload Register HF	PRLHF	R/W		$XXXXXXXX_B$
007920_H	Input Capture 0	IPCP0	R	Input Capture 0/1	$XXXXXXXX_B$
007921_H	Input Capture 0	IPCP0	R		$XXXXXXXX_B$
007922_H	Input Capture 1	IPCP1	R		$XXXXXXXX_B$
007923_H	Input Capture 1	IPCP1	R		$XXXXXXXX_B$

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
007924_H	Input Capture 2	IPCP2	R	Input Capture 2/3	$XXXXXXXX_B$
007925_H	Input Capture 2	IPCP2	R		$XXXXXXXX_B$
007926_H	Input Capture 3	IPCP3	R		$XXXXXXXX_B$
007927_H	Input Capture 3	IPCP3	R		$XXXXXXXX_B$
007928_H	Input Capture 4	IPCP4	R	Input Capture 4/5	$XXXXXXXX_B$
007929_H	Input Capture 4	IPCP4	R		$XXXXXXXX_B$
$00792A_H$	Input Capture 5	IPCP5	R		$XXXXXXXX_B$
$00792B_H$	Input Capture 5	IPCP5	R		$XXXXXXXX_B$
$00792C_H$	Input Capture 6	IPCP6	R	Input Capture 6/7	$XXXXXXXX_B$
$00792D_H$	Input Capture 6	IPCP6	R		$XXXXXXXX_B$
$00792E_H$	Input Capture 7	IPCP7	R		$XXXXXXXX_B$
$00792F_H$	Input Capture 7	IPCP7	R		$XXXXXXXX_B$
007930_H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	$XXXXXXXX_B$
007931_H	Output Compare 0	OCCP0	R/W		$XXXXXXXX_B$
007932_H	Output Compare 1	OCCP1	R/W		$XXXXXXXX_B$
007933_H	Output Compare 1	OCCP1	R/W		$XXXXXXXX_B$
007934_H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	$XXXXXXXX_B$
007935_H	Output Compare 2	OCCP2	R/W		$XXXXXXXX_B$
007936_H	Output Compare 3	OCCP3	R/W		$XXXXXXXX_B$
007937_H	Output Compare 3	OCCP3	R/W		$XXXXXXXX_B$
007938_H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	$XXXXXXXX_B$
007939_H	Output Compare 4	OCCP4	R/W		$XXXXXXXX_B$
$00793A_H$	Output Compare 5	OCCP5	R/W		$XXXXXXXX_B$
$00793B_H$	Output Compare 5	OCCP5	R/W		$XXXXXXXX_B$
$00793C_H$	Output Compare 6	OCCP6	R/W	Output Compare 6/7	$XXXXXXXX_B$
$00793D_H$	Output Compare 6	OCCP6	R/W		$XXXXXXXX_B$
$00793E_H$	Output Compare 7	OCCP7	R/W		$XXXXXXXX_B$
$00793F_H$	Output Compare 7	OCCP7	R/W		$XXXXXXXX_B$
007940_H	Timer Data 0	TCDT0	R/W	Free-run Timer 0	00000000_B
007941_H	Timer Data 0	TCDT0	R/W		00000000_B
007942_H	Timer Control Status 0	TCCSL0	R/W		00000000_B
007943_H	Timer Control Status 0	TCCSH0	R/W		$0XXXXXXX_B$
007944_H	Timer Data 1	TCDT1	R/W	Free-run Timer 1	00000000_B
007945_H	Timer Data 1	TCDT1	R/W		00000000_B
007946_H	Timer Control Status 1	TCCSL1	R/W		00000000_B
007947_H	Timer Control Status 1	TCCSH1	R/W		$0XXXXXXX_B$

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List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A40_H$	$007C40_H$	ID Register 8	IDR8	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A41_H$	$007C41_H$				
$007A42_H$	$007C42_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A43_H$	$007C43_H$				
$007A44_H$	$007C44_H$	ID Register 9	IDR9	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A45_H$	$007C45_H$				
$007A46_H$	$007C46_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A47_H$	$007C47_H$				
$007A48_H$	$007C48_H$	ID Register 10	IDR10	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A49_H$	$007C49_H$				
$007A4A_H$	$007C4A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4B_H$	$007C4B_H$				
$007A4C_H$	$007C4C_H$	ID Register 11	IDR11	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4D_H$	$007C4D_H$				
$007A4E_H$	$007C4E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4F_H$	$007C4F_H$				
$007A50_H$	$007C50_H$	ID Register 12	IDR12	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A51_H$	$007C51_H$				
$007A52_H$	$007C52_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A53_H$	$007C53_H$				
$007A54_H$	$007C54_H$	ID Register 13	IDR13	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A55_H$	$007C55_H$				
$007A56_H$	$007C56_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A57_H$	$007C57_H$				
$007A58_H$	$007C58_H$	ID Register 14	IDR14	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A59_H$	$007C59_H$				
$007A5A_H$	$007C5A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5B_H$	$007C5B_H$				
$007A5C_H$	$007C5C_H$	ID Register 15	IDR15	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5D_H$	$007C5D_H$				
$007A5E_H$	$007C5E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5F_H$	$007C5F_H$				

List of Message Buffers (DLC Registers and Data Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A80_H$ to $007A87_H$	$007C80_H$ to $007C87_H$	Data Register 0 (8 bytes)	DTR0	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A88_H$ to $007A8F_H$	$007C88_H$ to $007C8F_H$	Data Register 1 (8 bytes)	DTR1	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A90_H$ to $007A97_H$	$007C90_H$ to $007C97_H$	Data Register 2 (8 bytes)	DTR2	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A98_H$ to $007A9F_H$	$007C98_H$ to $007C9F_H$	Data Register 3 (8 bytes)	DTR3	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AA0_H$ to $007AA7_H$	$007CA0_H$ to $007CA7_H$	Data Register 4 (8 bytes)	DTR4	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AA8_H$ to $007AAF_H$	$007CA8_H$ to $007CAF_H$	Data Register 5 (8 bytes)	DTR5	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AB0_H$ to $007AB7_H$	$007CB0_H$ to $007CB7_H$	Data Register 6 (8 bytes)	DTR6	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AB8_H$ to $007ABF_H$	$007CB8_H$ to $007CBF_H$	Data Register 7 (8 bytes)	DTR7	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AC0_H$ to $007AC7_H$	$007CC0_H$ to $007CC7_H$	Data Register 8 (8 bytes)	DTR8	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AC8_H$ to $007ACF_H$	$007CC8_H$ to $007CCF_H$	Data Register 9 (8 bytes)	DTR9	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AD0_H$ to $007AD7_H$	$007CD0_H$ to $007CD7_H$	Data Register 10 (8 bytes)	DTR10	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AD8_H$ to $007ADF_H$	$007CD8_H$ to $007CDF_H$	Data Register 11 (8 bytes)	DTR11	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AE0_H$ to $007AE7_H$	$007CE0_H$ to $007CE7_H$	Data Register 12 (8 bytes)	DTR12	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AE8_H$ to $007AEF_H$	$007CE8_H$ to $007CEF_H$	Data Register 13 (8 bytes)	DTR13	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

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Interrupt cause	EI^{2}OS Support	DMA channel number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
UART 2 RX / UART 4 RX	Y2	14	#39	$FFFF60_H$	ICR14	$0000BE_H$
UART 2 TX / UART 4 TX	Y1	15	#40	$FFFF5C_H$		
Flash Memory	N	——	#41	$FFFF58_H$	ICR15	$0000BF_H$
Delayed Interrupt	N	——	#42	$FFFF54_H$		

Y1 : Usable
Y2 : Usable, with EI^{2}OS stop function
N : Unusable

Note:
- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
- When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

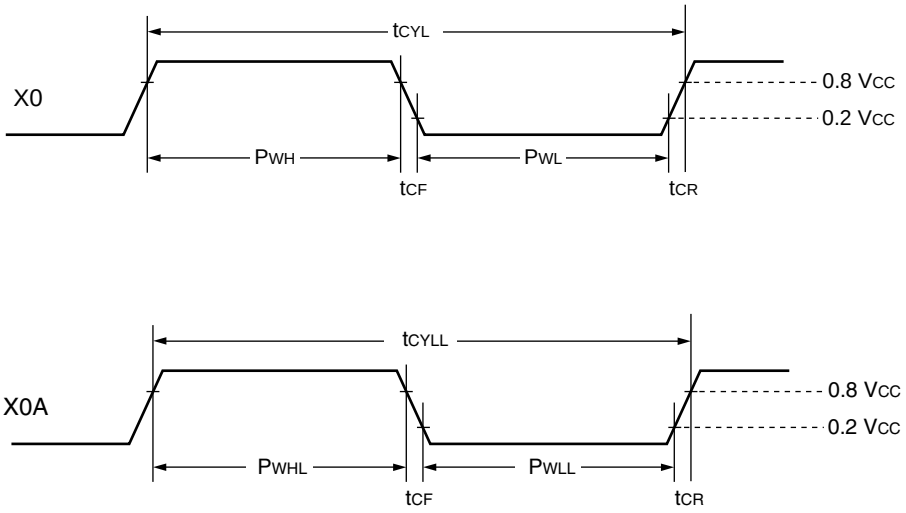
11.3 DC Characteristics

($T_A = -40°C$ to $+105°C$, $V_{CC} = 5.0\ V \pm 10\%$, $f_{CP} \leq 24$ MHz, $V_{SS} = AV_{SS} = 0\ V$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At V_{CC} = 5 V ± 10%)	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	V_{CC} + 0.3	V	Port inputs if TTL input levels are selected
	V_{IHS}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHI}	—	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	V_{CC} − 0.3	—	V_{CC} + 0.3	V	MD input pin
Input L voltage (At V_{CC} = 5 V ± 10%)	V_{ILS}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{ILA}	—	—	V_{SS} − 0.3	—	0.5 V_{CC}	V	Port inputs if Automotive input levels are selected
	V_{ILT}	—	—	V_{SS} − 0.3	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILI}	—	—	V_{SS} − 0.3	—	0.3 V_{CC}	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	V_{SS} − 0.3	—	V_{SS} + 0.3	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH} = −4.0 mA	V_{CC} − 0.5	—	—	V	
Output H voltage	V_{OHI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OH} = −3.0 mA	V_{CC} − 0.5	—	—	V	
Output L voltage	V_{OL}	Normal outputs	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Output L voltage	V_{OLI}	I^2C current outputs	V_{CC} = 4.5 V, I_{OL} = 3.0 mA	—	—	0.4	V	

(Continued)

Clock Timing



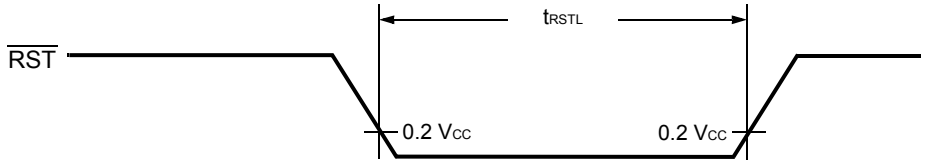
11.4.2 Reset Standby Input

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0.0 V)

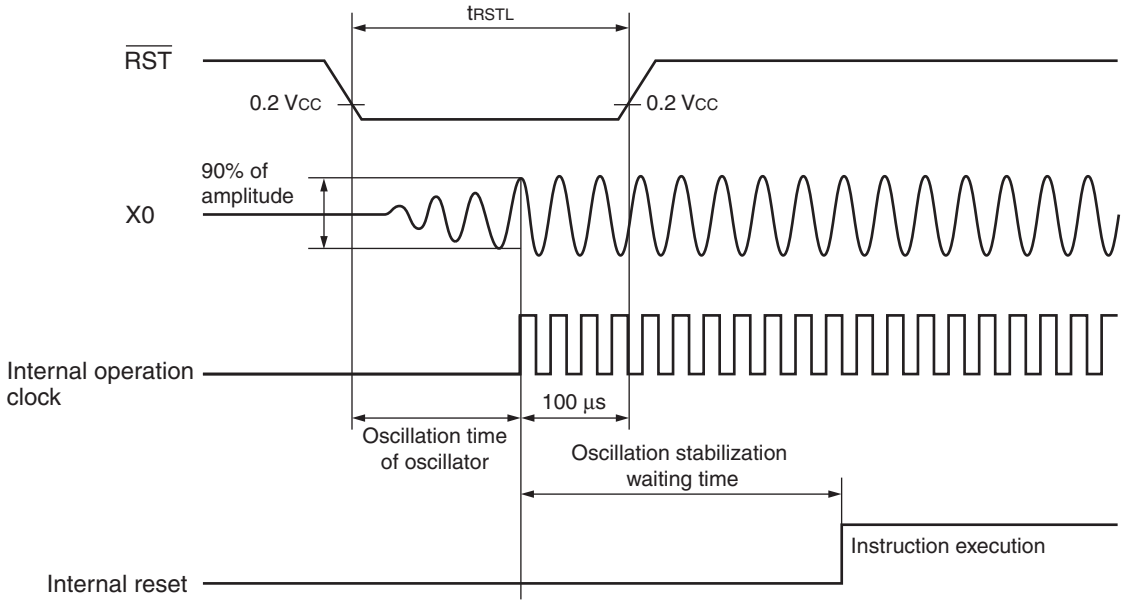
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	500	—	ns	Under normal operation
			Oscillation time of oscillator* + 100 µs	—	µs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	µs	In Time Timer mode

* : The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

- **Under normal operation:**



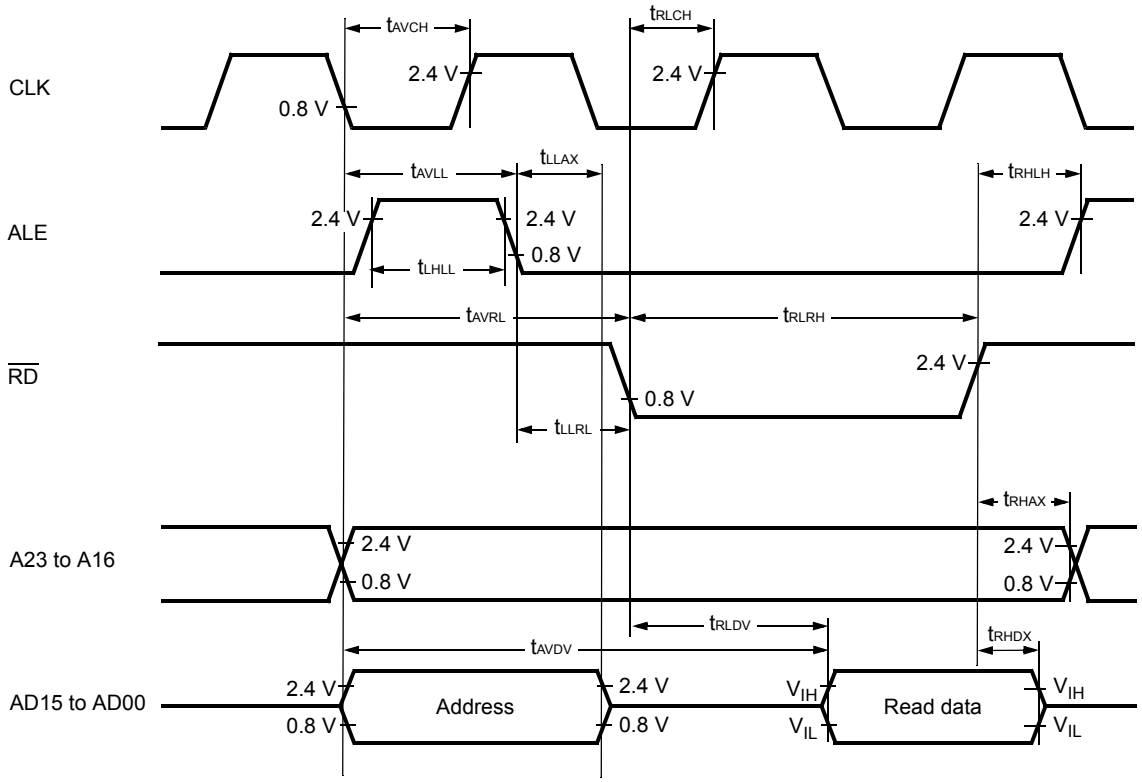
- **In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:**



11.4.5 Bus Timing (Read)

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	t_{LHLL}	ALE		$t_{CP}/2 - 10$	—	ns
Valid address → ALE ↓ time	t_{AVLL}	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns
ALE ↓ → Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	A23 to A16, AD15 to AD00, $\overline{RD}$		$t_{CP} - 15$	—	ns
Valid address → Valid data input	t_{AVDV}	A23 to A16, AD15 to AD00		—	$5\ t_{CP}/2 - 60$	ns
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	—	$3\ t_{CP}/2 - 20$	—	ns
$\overline{RD}$ ↓ → Valid data input	t_{RLDV}	$\overline{RD}$, AD15 to AD00		—	$3\ t_{CP}/2 - 50$	ns
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	$\overline{RD}$, AD15 to AD00		0	—	ns
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		$t_{CP}/2 - 15$	—	ns
$\overline{RD}$ ↑ → Address valid time	t_{RHAX}	$\overline{RD}$, A23 to A16		$t_{CP}/2 - 10$	—	ns
Valid address → CLK ↑ time	t_{AVCH}	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		$t_{CP}/2 - 15$	—	ns
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	ALE, $\overline{RD}$		$t_{CP}/2 - 15$	—	ns

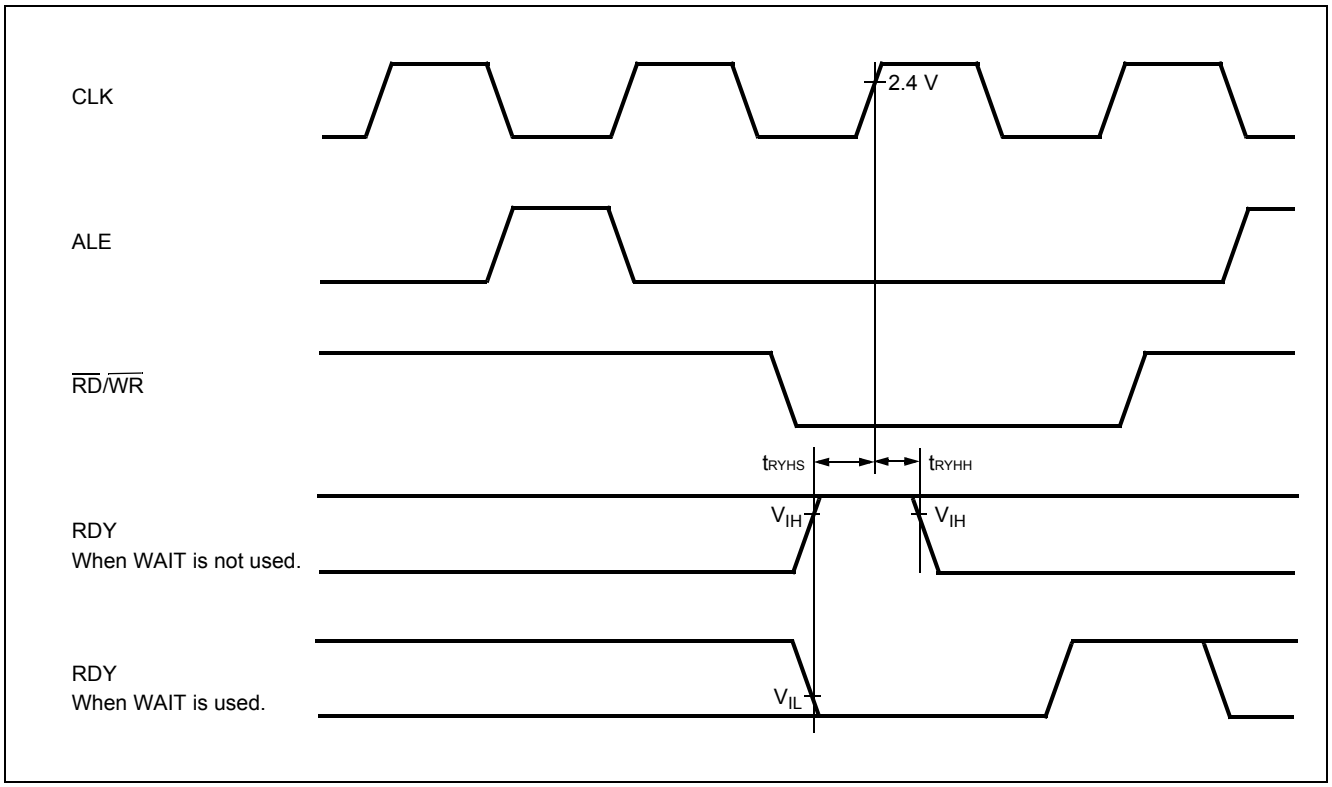


11.4.7 Ready Input Timing

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Test Condition	Rated Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	f_{CP} = 16 MHz
				32	—	ns	f_{CP} = 24 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note: : If the RDY setup time is insufficient, use the auto-ready function.

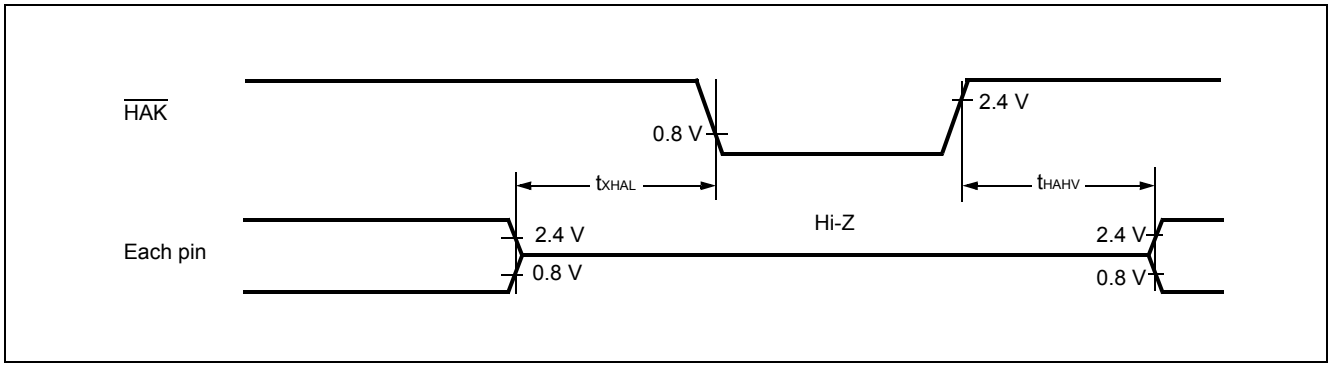


11.4.8 Hold Timing

($T_A = -40°C$ to $+105°C$, $V_{CC} = 5.0\ V \pm 10\%$, $V_{SS} = 0.0\ V$, $f_{CP} \leq 24$ MHz)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}	ns
$\overline{HAK}$ ↑ time → Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}	2 t_{CP}	ns

Note: : There is more than 1 cycle from when HRQ reads in until the $\overline{HAK}$ is changed.

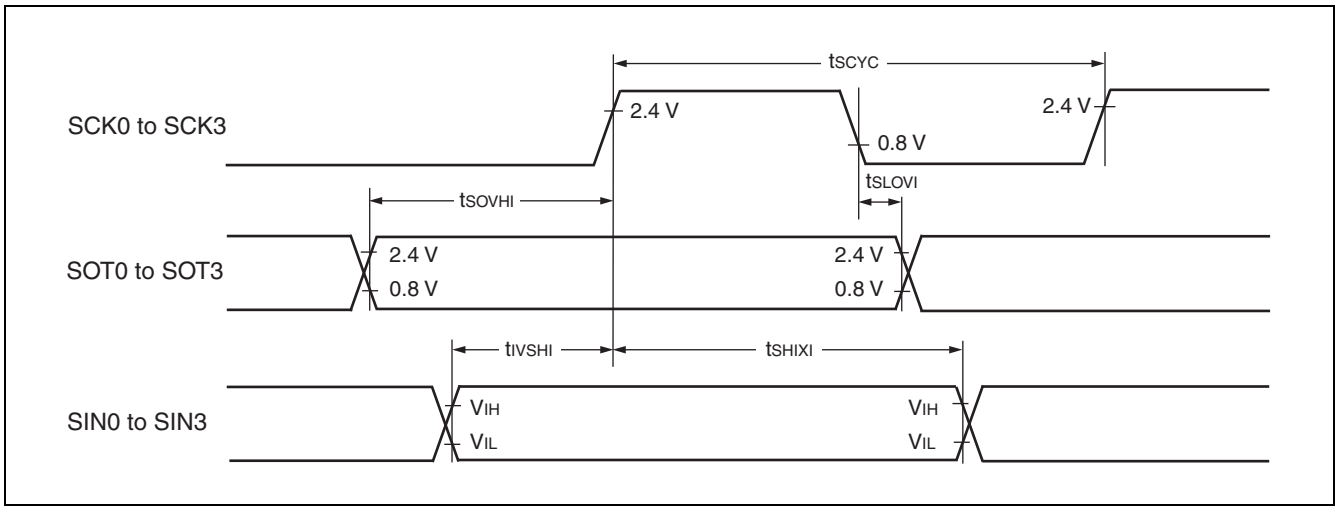


■ **Bit setting: ESCR:SCES = 1, ECCR:SCDE = 1**

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		−50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK0 to SCK3, SOT0 to SOT3		3 t_{CP} − 70	—	ns

Note:
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to "Clock Timing".



11.4.13 I^2C Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V)

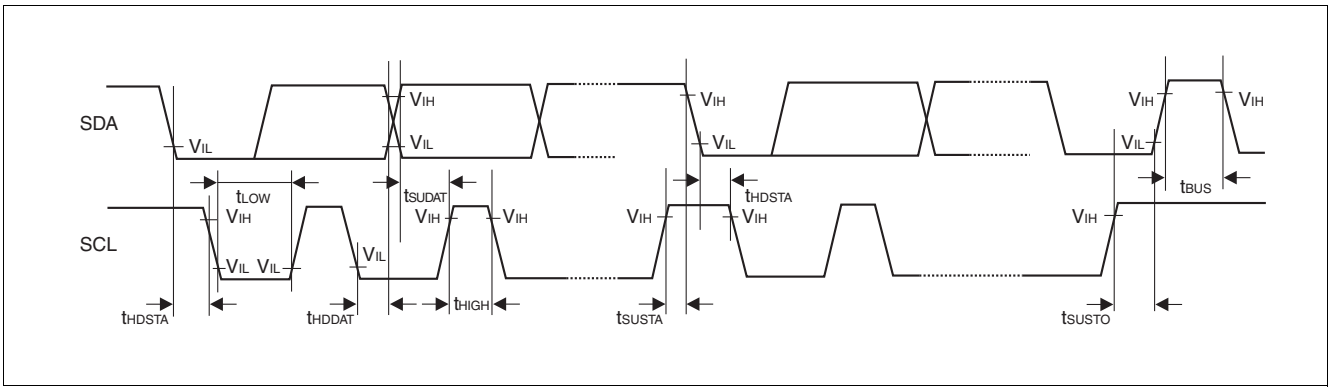
Parameter	Symbol	Condition	Standard-mode		Fast-mode*1		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*2	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓ → SCL ↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time (repeated) START condition SCL ↑ → SDA ↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*3	0	0.9*4	µs
Data set-up time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1:For use at over 100 kHz, set the machine clock to at least 6 MHz.

*2:R,C: Pull-up resistor and load capacitor of the SCL and SDA lines.

*3:The maximum t_{HDDAT} meets the requirement that it does not extend the "L" width (t_{LOW}) of the SCL signal.

*4:A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.



11.5 A/D Converter

(T_A = −40°C to +105°C, 3.0 V≤ AVRH − AVRL, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP}≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	AVRL − 1.5 × LSB	AVRL + 0.5 × LSB	AVRL + 2.5 × LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	AVRH − 3.5 × LSB	AVRH − 1.5 × LSB	AVRH + 0.5 × LSB	V	
Compare time	—	—	1.0	—	16500	µs	4.5 V≤ AV_{CC}≤ 5.5 V
			2.0				4.0 V≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	∞	µs	4.5 V≤ AV_{CC}≤ 5.5 V
			1.2				4.0 V≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN23	−0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 2.7	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

*: If the A/D convertor is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .
Note: : The accuracy gets worse as |AVRH − AVRL| becomes smaller.

11.6 Definition of A/D Converter Terms

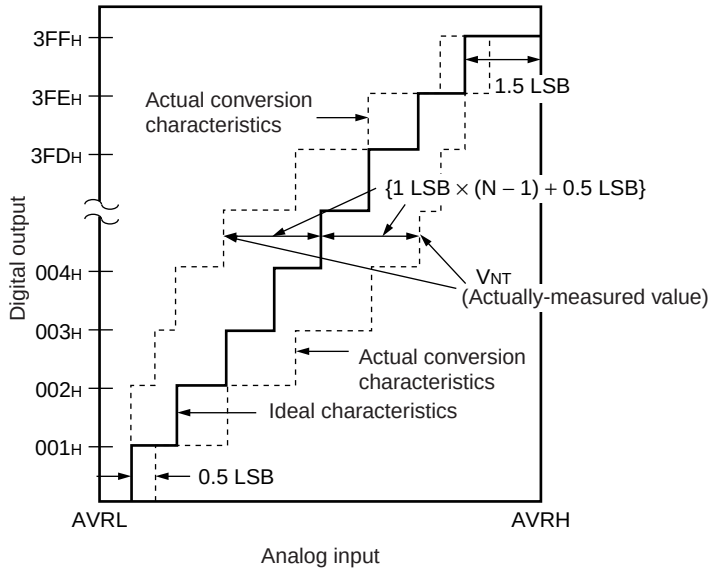
Resolution : Analog variation that is recognized by the A/D converter.

Non linearity error : The deviation between the actual conversion characteristics and a line that joins the zero-transition line (“00 0000 0000” ← → “00 0000 0001”) to the full-scale transition line (“11 1111 1110” ← → “11 1111 1111”) .

Differential linearity error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Total error : Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

N : Value of the digital output from the A/D converter

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH − 1.5 LSB [V]

V_{NT} : A voltage at which the digital output transitions from $(N - 1)_H$ to N_H.

(Continued)