Infineon Technologies - MB90F347ESPMC-GS9013SPE1 Datasheet

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What is "Embedded - Microcontrollers"?

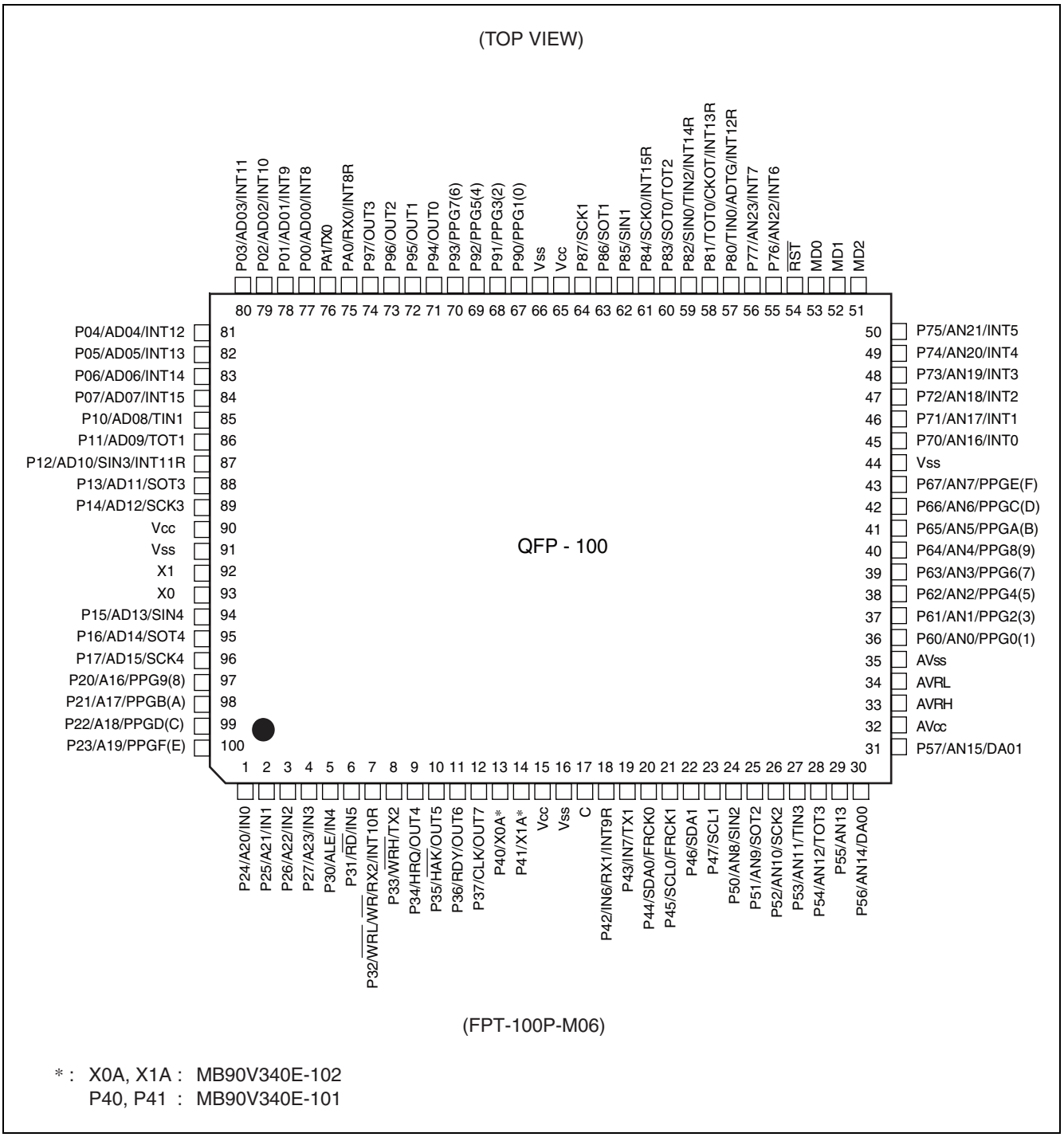
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f347espmc-gs9013spe1

Part Number / Parameter	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
A/D Converter	24 input channels	Devices with a C suffix in the part number : 24 channels Devices without a C suffix in the part number : 16 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs include sample time (per one channel)		
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function		
16-bit Free-run Timer (2 channels)	Generates an interrupt signal on overflow Supports Timer Clear when the output compare finds a match Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock freq.) Free-run Timer 0 (clock input FRCK0) corresponds to ICU 0/1/2/3, OCU 0/1/2/3 Free-run Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7		
16-bit Output Compare (8 channels)	Generates an interrupt signal when one of the 16-bit free-run timer matches the output compare register A pair of compare registers can be used to generate an output signal.		
16-bit Input Capture (8 channels)	Captures the value of the 16-bit free-run timer and generates an interrupt when triggered by a pin input (rising edge, falling edge, or both rising and falling edges).		
8/16-bit Programmable Pulse Generator	8 channels (16-bit) /16 channels (8-bit) Sixteen 8-bit reload counters Sixteen 8-bit reload registers for L pulse width Sixteen 8-bit reload registers for H pulse width		
	Supports 8-bit and 16-bit operation modes A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operating clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)		
CAN Interface	3 channels	2 channels : MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S) 1 channel : MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	2 channels : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S) 1 channel : MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission in response to Remote Frames Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps		

■ MB90V340E-101/MB90V340E-102



This pin assignment is for using MB90V340E-101/102 via probecable as MB90340E.

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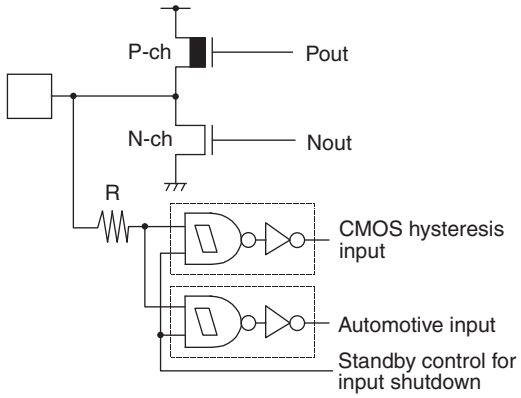
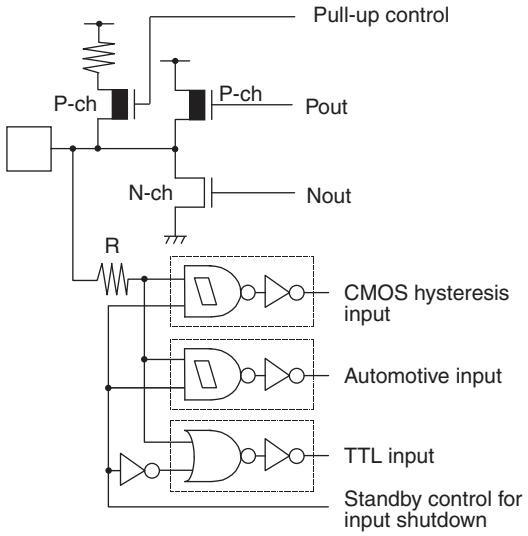
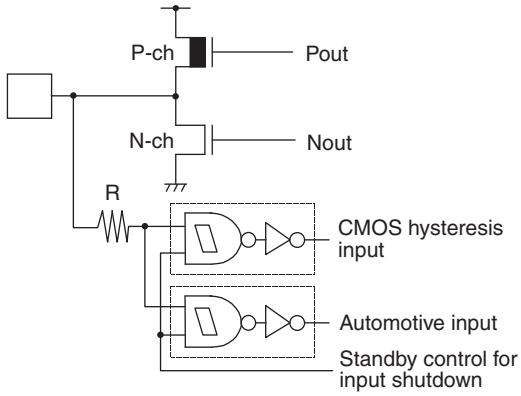
Type	Circuit	Remarks
F		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)
G		■ CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby) ■ TTL input (with function to disconnect input during standby) ■ Programmable pull-up resistor: 50 kΩ approx.
H		■ CMOS level output (I_{OL} = 3 mA, I_{OH} = –3 mA) ■ CMOS hysteresis input (with function to disconnect input during standby) ■ Automotive input (with function to disconnect input during standby)

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5. Handling Devices

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

2. Handling unused pins

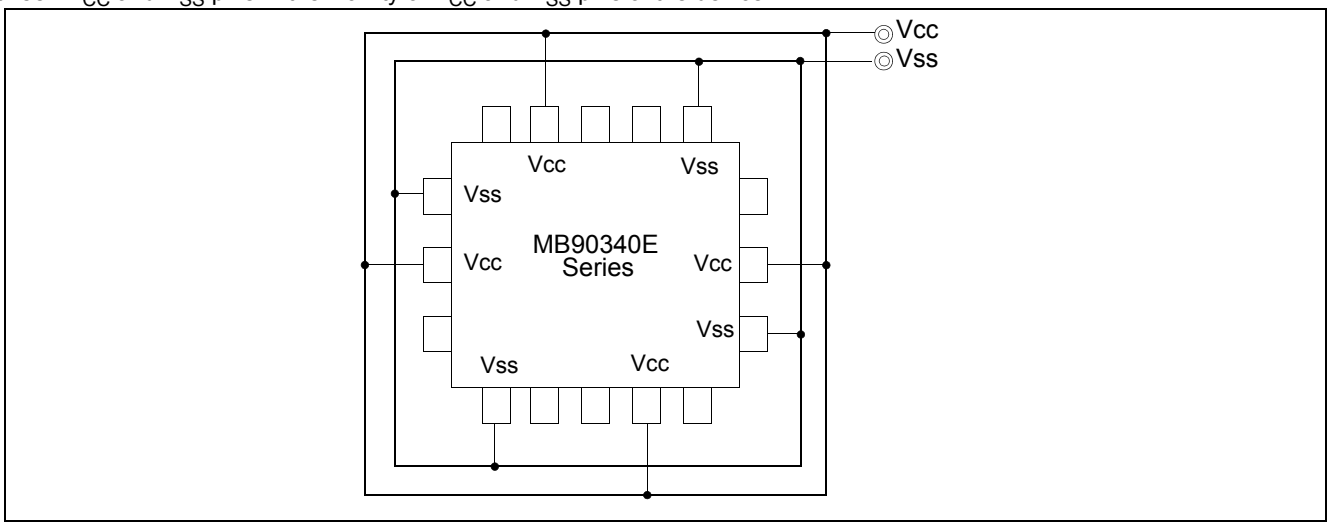
Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 kΩ or more.

3. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally.
Connect V_{CC} and V_{SS} pins to the device from the current supply source at a possibly low impedance.

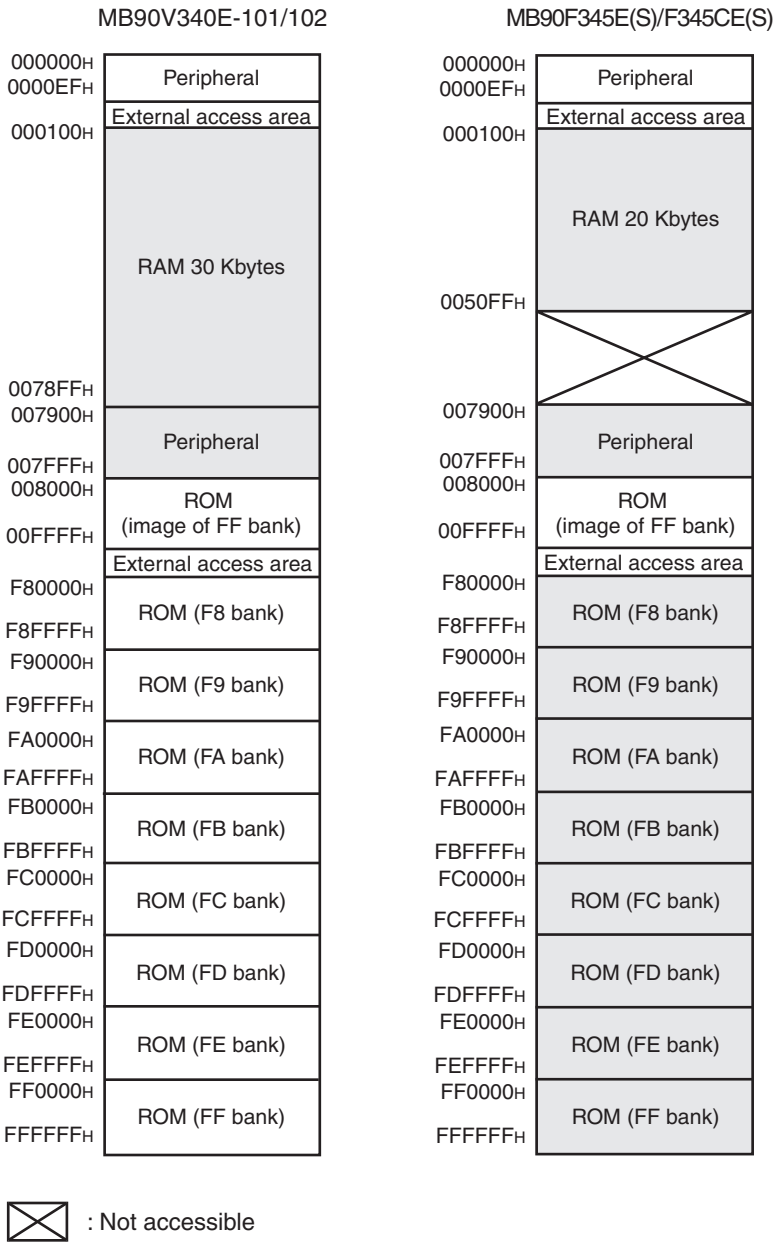
- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 µF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

7. Memory Map


MB90V340E-101/102
000000H
0000EFH
Peripheral
External access area
000100H
RAM 30 Kbytes
0078FFH
007900H
Peripheral
007FFFH
008000H
ROM
(image of FF bank)
00FFFFH
External access area
F80000H
ROM (F8 bank)
F8FFFFH
F90000H
ROM (F9 bank)
F9FFFFH
FA0000H
ROM (FA bank)
FAFFFFH
FB0000H
ROM (FB bank)
FBFFFFH
FC0000H
ROM (FC bank)
FCFFFFH
FD0000H
ROM (FD bank)
FDFFFFH
FE0000H
ROM (FE bank)
FEFFFFH
FF0000H
ROM (FF bank)
FFFFFFH
MB90F345E(S)/F345CE(S)
000000H
0000EFH
Peripheral
External access area
000100H
RAM 20 Kbytes
0050FFH
007900H
Peripheral
007FFFH
008000H
ROM
(image of FF bank)
00FFFFH
External access area
F80000H
ROM (F8 bank)
F8FFFFH
F90000H
ROM (F9 bank)
F9FFFFH
FA0000H
ROM (FA bank)
FAFFFFH
FB0000H
ROM (FB bank)
FBFFFFH
FC0000H
ROM (FC bank)
FCFFFFH
FD0000H
ROM (FD bank)
FDFFFFH
FE0000H
ROM (FE bank)
FEFFFFH
FF0000H
ROM (FF bank)
FFFFFFH
: Not accessible

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
$0079E0_H$	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	$XXXXXXXX_B$
$0079E1_H$	Detect Address Setting 0	PADR0	R/W		$XXXXXXXX_B$
$0079E2_H$	Detect Address Setting 0	PADR0	R/W		$XXXXXXXX_B$
$0079E3_H$	Detect Address Setting 1	PADR1	R/W		$XXXXXXXX_B$
$0079E4_H$	Detect Address Setting 1	PADR1	R/W		$XXXXXXXX_B$
$0079E5_H$	Detect Address Setting 1	PADR1	R/W		$XXXXXXXX_B$
$0079E6_H$	Detect Address Setting 2	PADR2	R/W		$XXXXXXXX_B$
$0079E7_H$	Detect Address Setting 2	PADR2	R/W		$XXXXXXXX_B$
$0079E8_H$	Detect Address Setting 2	PADR2	R/W		$XXXXXXXX_B$
$0079E9_H$ to $0079EF_H$	Reserved				
$0079F0_H$	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	$XXXXXXXX_B$
$0079F1_H$	Detect Address Setting 3	PADR3	R/W		$XXXXXXXX_B$
$0079F2_H$	Detect Address Setting 3	PADR3	R/W		$XXXXXXXX_B$
$0079F3_H$	Detect Address Setting 4	PADR4	R/W		$XXXXXXXX_B$
$0079F4_H$	Detect Address Setting 4	PADR4	R/W		$XXXXXXXX_B$
$0079F5_H$	Detect Address Setting 4	PADR4	R/W		$XXXXXXXX_B$
$0079F6_H$	Detect Address Setting 5	PADR5	R/W		$XXXXXXXX_B$
$0079F7_H$	Detect Address Setting 5	PADR5	R/W		$XXXXXXXX_B$
$0079F8_H$	Detect Address Setting 5	PADR5	R/W		$XXXXXXXX_B$
$0079F9_H$ to $0079FF_H$	Reserved				
$007A00_H$ to $007AFF_H$	Reserved for CAN Controller 0. Refer to “CAN Controllers				
$007B00_H$ to $007BFF_H$	Reserved for CAN Controller 0. Refer to “CAN Controllers”				
$007C00_H$ to $007CFF_H$	Reserved for CAN Controller 1. Refer to “CAN Controllers”				
$007D00_H$ to $007DFF_H$	Reserved for CAN Controller 1. Refer to “CAN Controllers”				
$007E00_H$ to $007FFF_H$	Reserved				

Note:
- Initial value of “X” represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

List of Message Buffers (ID Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007A00_H$ to $007A1F_H$	$007C00_H$ to $007C1F_H$	General-Purpose RAM	——	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A20_H$	$007C20_H$	ID Register 0	IDR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A21_H$	$007C21_H$				
$007A22_H$	$007C22_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A23_H$	$007C23_H$				
$007A24_H$	$007C24_H$	ID Register 1	IDR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A25_H$	$007C25_H$				
$007A26_H$	$007C26_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A27_H$	$007C27_H$				
$007A28_H$	$007C28_H$	ID Register 2	IDR2	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A29_H$	$007C29_H$				
$007A2A_H$	$007C2A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A2B_H$	$007C2B_H$				
$007A2C_H$	$007C2C_H$	ID Register 3	IDR3	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A2D_H$	$007C2D_H$				
$007A2E_H$	$007C2E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A2F_H$	$007C2F_H$				
$007A30_H$	$007C30_H$	ID Register 4	IDR4	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A31_H$	$007C31_H$				
$007A32_H$	$007C32_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A33_H$	$007C33_H$				
$007A34_H$	$007C34_H$	ID Register 5	IDR5	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A35_H$	$007C35_H$				
$007A36_H$	$007C36_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A37_H$	$007C37_H$				
$007A38_H$	$007C38_H$	ID Register 6	IDR6	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A39_H$	$007C39_H$				
$007A3A_H$	$007C3A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A3B_H$	$007C3B_H$				
$007A3C_H$	$007C3C_H$	ID Register 7	IDR7	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A3D_H$	$007C3D_H$				
$007A3E_H$	$007C3E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A3F_H$	$007C3F_H$				

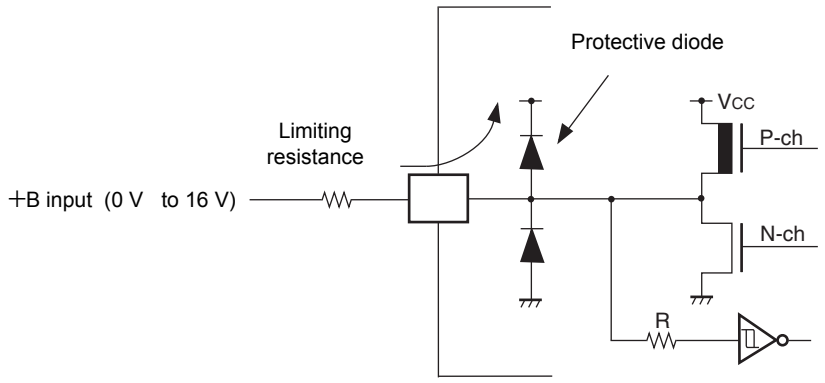
List of Message Buffers (DLC Registers and Data Registers) (3)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
$007AF0_H$ to $007AF7_H$	$007CF0_H$ to $007CF7_H$	Data Register 14 (8 bytes)	DTR14	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AF8_H$ to $007AFF_H$	$007CF8_H$ to $007CFF_H$	Data Register 15 (8 bytes)	DTR15	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

(Continued)

- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

■ Input/output equivalent circuits



*6: The maximum output current is defined as the peak value of the current of any one of the corresponding pins.

*7: The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.

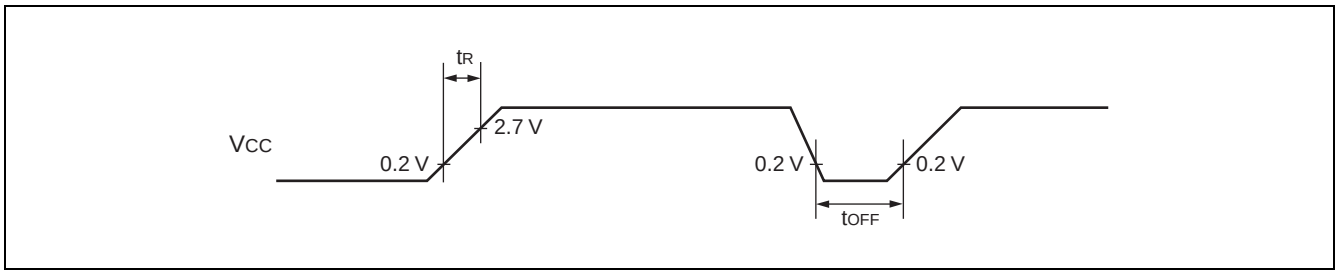
*8: The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

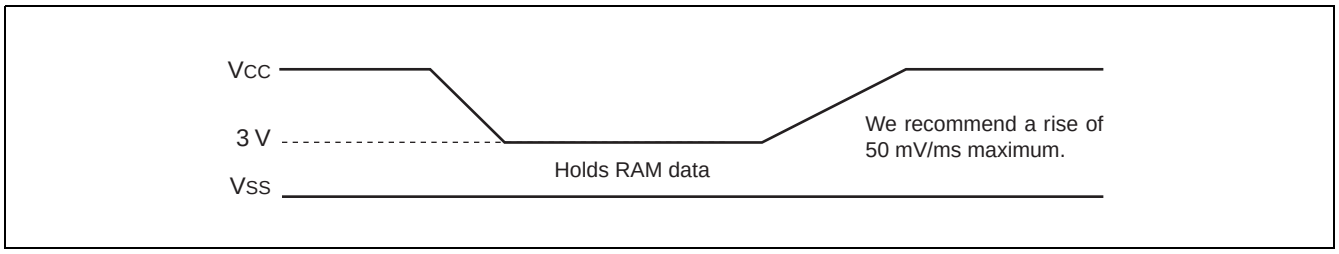
11.4.3 Power On Reset

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Waiting time until power-on



Note: : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



11.4.4 Clock Output Timing

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	f_{CP} = 16 MHz
				41.67	—	ns	f_{CP} = 24 MHz
CLK ↑ → CLK ↓	t_{CHCL}	CLK	—	20	—	ns	f_{CP} = 16 MHz
				13	—	ns	f_{CP} = 24 MHz

11.4.9 LIN-UART0/1/2/3

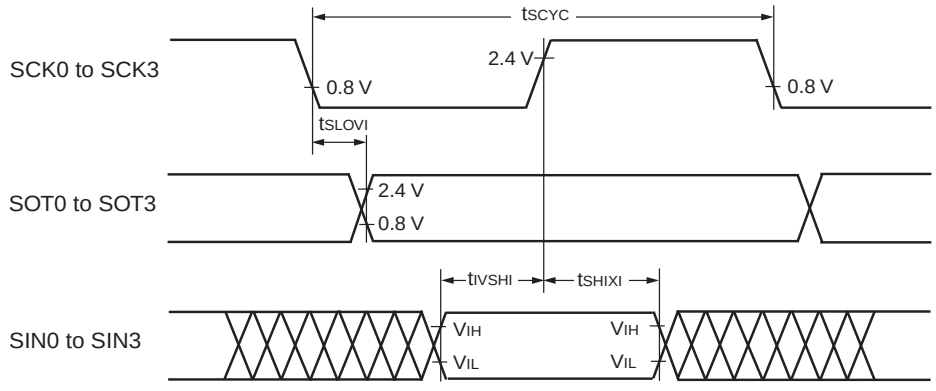
■ **Bit setting: ESCR:SCES = 0, ECCR:SCDE = 0**

(T_A = −40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 24 MHz, V_{SS} = 0 V)

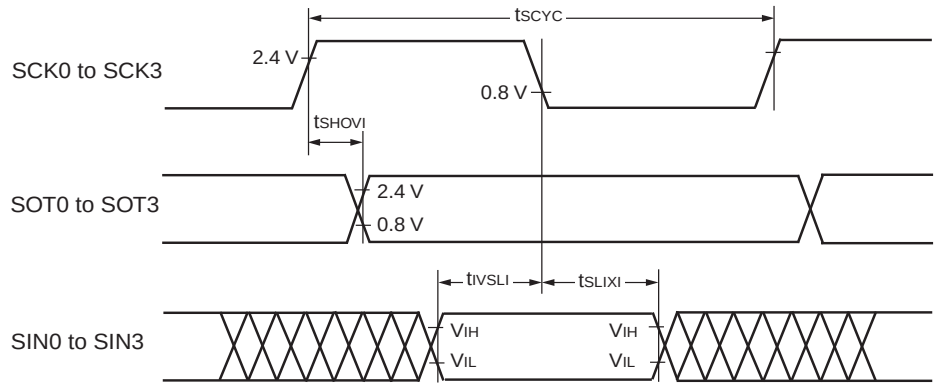
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode output pins are C_L = 80 pF + 1 TTL.	5 t_{CP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCK0 to SCK3, SOT0 to SOT3		−50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK0 to SCK3, SIN0 to SIN3		t_{CP} + 80	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
Serial clock “L” pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode output pins are C_L = 80 pF + 1 TTL.	3 t_{CP} - t_R	—	ns
Serial clock “H” pulse width	t_{SLSH}	SCK0 to SCK3		t_{CP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCK0 to SCK3, SOT0 to SOT3		—	2 t_{CP} + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK0 to SCK3, SIN0 to SIN3		30	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCK0, SCK1, SIN0 to SIN3		t_{CP} + 30	—	ns
SCK fall time	t_F	SCK0 to SCK3		—	10	ns
SCK rise time	t_R	SCK0 to SCK3		—	10	ns

Note:
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “ (1) Clock Timing”.

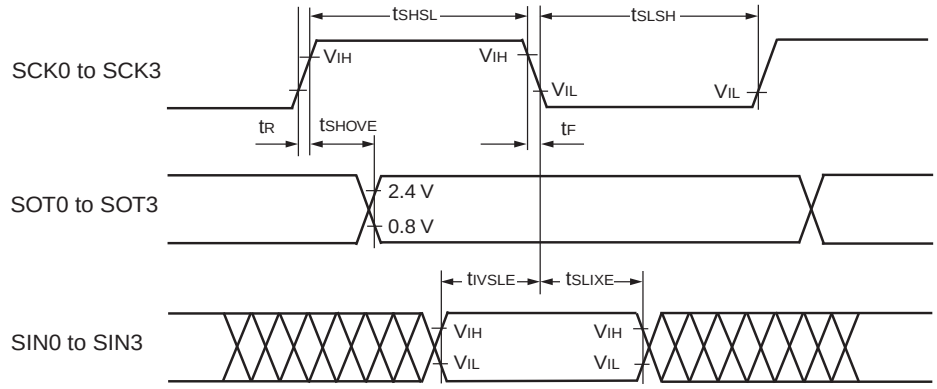
- Internal Shift Clock Mode



- Internal Shift Clock Mode



- External Shift Clock Mode



11.5 A/D Converter

(T_A = −40°C to +105°C, 3.0 V≤ AVRH − AVRL, V_{CC} = AV_{CC} = 5.0 V ± 10%, f_{CP}≤ 24 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	AVRL − 1.5 × LSB	AVRL + 0.5 × LSB	AVRL + 2.5 × LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	AVRH − 3.5 × LSB	AVRH − 1.5 × LSB	AVRH + 0.5 × LSB	V	
Compare time	—	—	1.0	—	16500	µs	4.5 V≤ AV_{CC}≤ 5.5 V
			2.0				4.0 V≤ AV_{CC} < 4.5 V
Sampling time	—	—	0.5	—	∞	µs	4.5 V≤ AV_{CC}≤ 5.5 V
			1.2				4.0 V≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN23	−0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN23	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 2.7	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	600	900	µA	
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN23	—	—	4	LSB	

*: If the A/D convertor is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .
Note: : The accuracy gets worse as |AVRH − AVRL| becomes smaller.

11.6 Definition of A/D Converter Terms

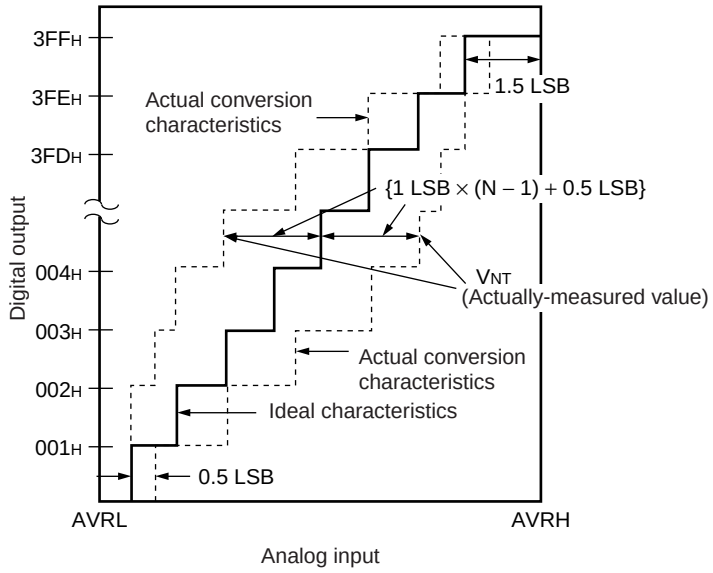
Resolution : Analog variation that is recognized by the A/D converter.

Non linearity error : The deviation between the actual conversion characteristics and a line that joins the zero-transition line (“00 0000 0000” ← → “00 0000 0001”) to the full-scale transition line (“11 1111 1110” ← → “11 1111 1111”) .

Differential linearity error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Total error : Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

N : Value of the digital output from the A/D converter

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

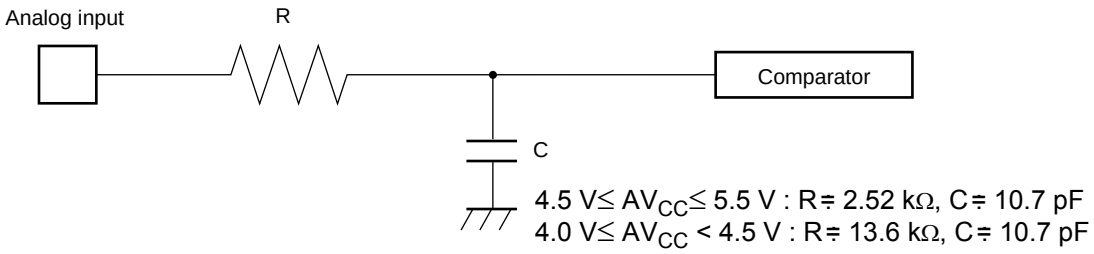
V_{FST} (Ideal value) = AVRH − 1.5 LSB [V]

V_{NT} : A voltage at which the digital output transitions from $(N - 1)_H$ to N_H.

(Continued)

If the output impedance of the external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model

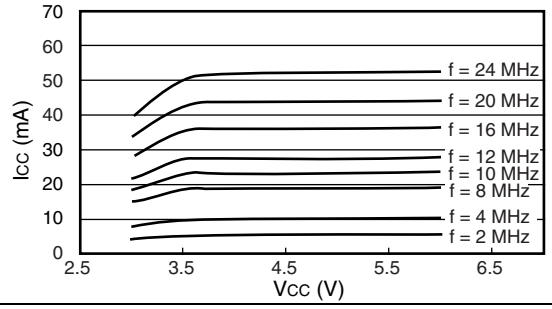


Note: : Use the values in the figure only as a guideline.

■ MB90F347E, MB90F347ES, MB90F347CE, MB90F347CES

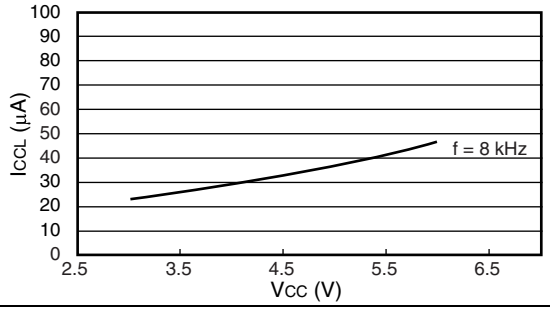
$I_{CC} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



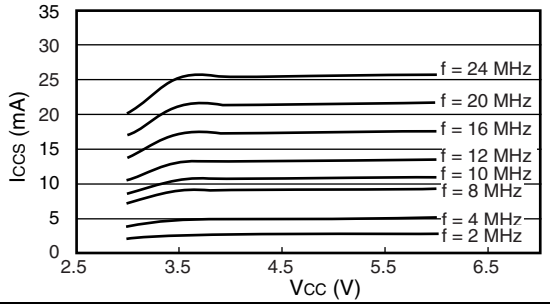
$I_{CCL} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



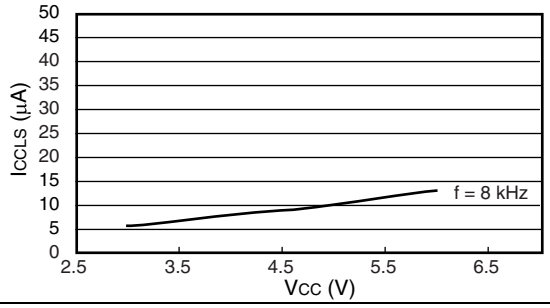
$I_{CCS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



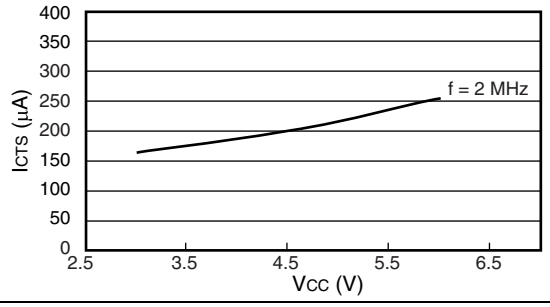
$I_{CCLS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



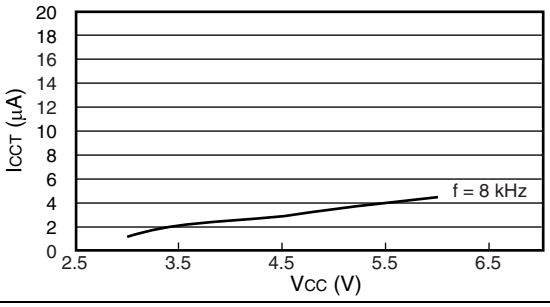
$I_{CTS} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



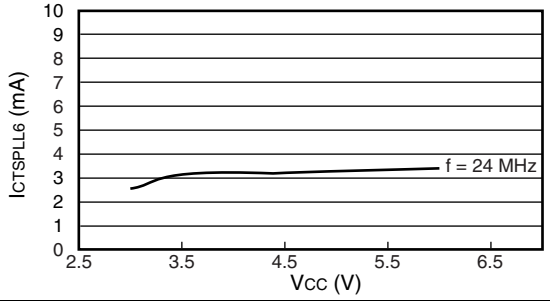
$I_{CCT} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



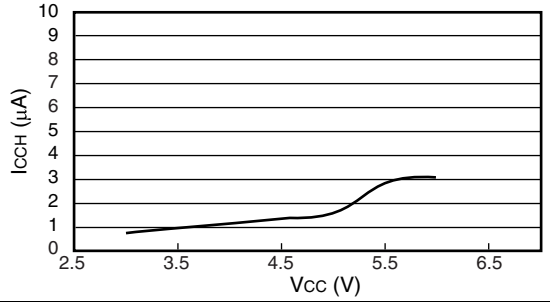
$I_{CTSPLL6} - V_{CC}$

$T_A = +25°C$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$

$T_A = +25°C$, stopped



13. Ordering Information

Part number	Package	Remarks
MB90F342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F342ESPF		
MB90F342CEPF		
MB90F342CESPF		
MB90F342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F342ESPMC		
MB90F342CEPMC		
MB90F342CESPMC		
MB90F345EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F345ESPF		
MB90F345CEPF		
MB90F345CESPF		
MB90F345EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F345ESPMC		
MB90F345CEPMC		
MB90F345CESPMC		
MB90F346EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F346ESPF		
MB90F346CEPF		
MB90F346CESPF		
MB90F346EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F346ESPMC		
MB90F346CEPMC		
MB90F346CESPMC		

(Continued)

Part number	Package	Remarks
MB90F347EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F347ESPF		
MB90F347CEPF		
MB90F347CESPF		
MB90F347EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F347ESPMC		
MB90F347CEPMC		
MB90F347CESPMC		
MB90F349EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90F349ESPF		
MB90F349CEPF		
MB90F349CESPF		
MB90F349EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90F349ESPMC		
MB90F349CEPMC		
MB90F349CESPMC		
MB90341EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90341ESPF		
MB90341CEPF		
MB90341CESPF		
MB90341EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90341ESPMC		
MB90341CEPMC		
MB90341CESPMC		
MB90342EPF	100-pin plastic QFP (FPT-100P-M06)	
MB90342ESPF		
MB90342CEPF		
MB90342CESPF		
MB90342EPMC	100-pin plastic LQFP (FPT-100P-M20)	
MB90342ESPMC		
MB90342CEPMC		
MB90342CESPMC		

(Continued)

15. Major Changes

Spansiion Publication Number: DS07-13747-4E

Page	Section	Change Results
___	___	Deleted the part numbers; MB90F343E(S), MB90F343CE(S)
51	Electrical Characteristics Absolute Maximum Ratings	Added “*6” in remark for “L" level maximum output current and “H” level maximum output current. Added “*7” in remark for “L" level average output current and “H” level average output current. Added “*8” in remark for “L"level average overall output current and “H” level average overall output current.
52		Added as follows. “*6:The maximum output current is defined as the peak value of the current of any one of the corresponding pins.” “*7:The average output current is defined as the value of the average current flowing over 100 ms at any one of the corresponding pins.” “*8:The average total output current is defined as the value of the average current flowing over 100 ms at all of the corresponding pins.”

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90340E Series F2MC-16LX 16-bit Microcontroller Datasheet Document Number: 002-04498				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	08/23/2010	Migrated to Cypress and assigned document number 002-04498. No change to document contents or format.
*A	5221535	AKIH	05/04/2016	Updated to Cypress template

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