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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

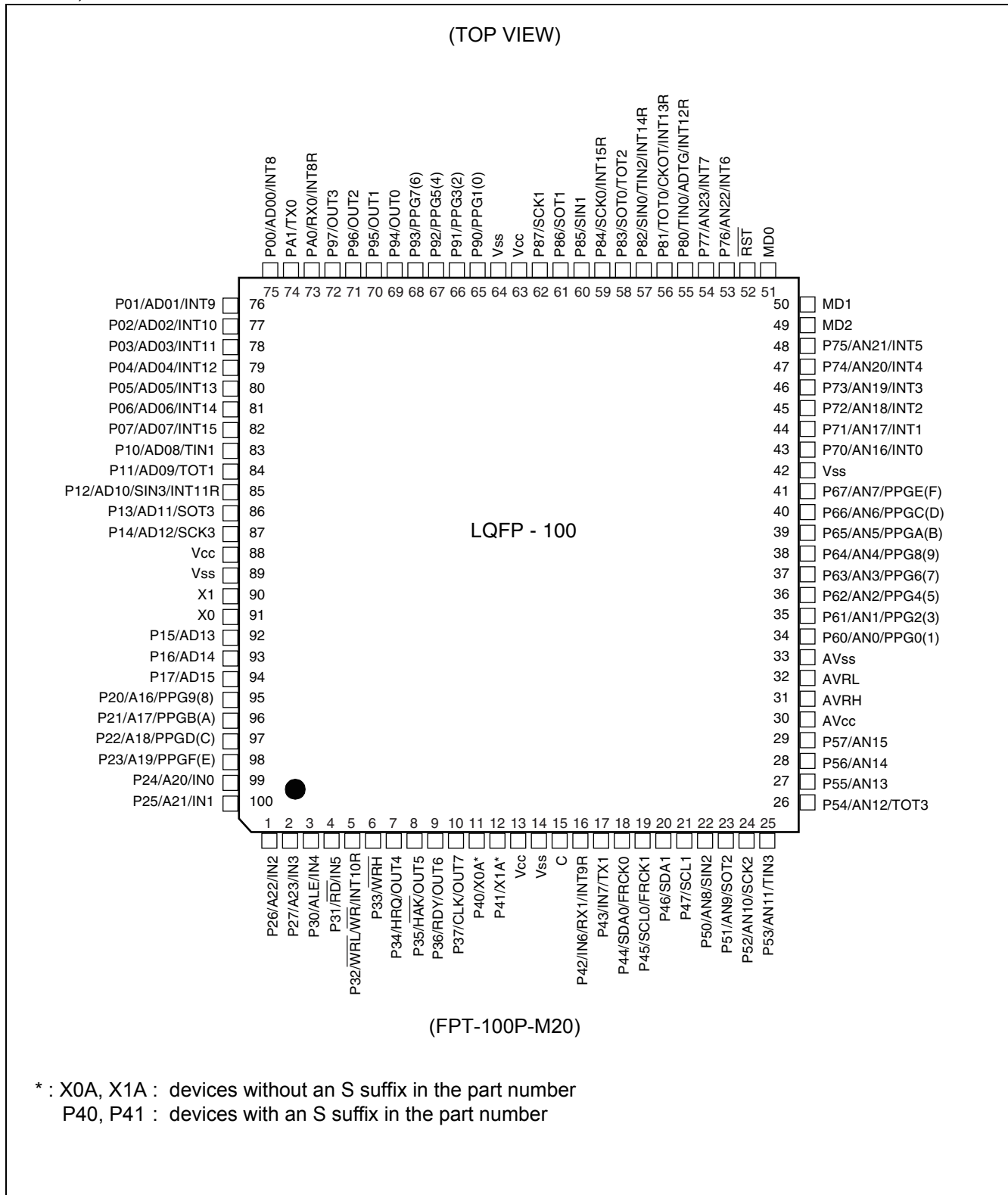
Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	24MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	3.5V ~ 5.5V
Data Converters	A/D 16x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90f347espmc-gse2

1. Product Lineup

Part Number			
Parameter	MB90V340E-101, MB90V340E-102	MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90F346E(S), MB90F346CE(S), MB90F347E(S), MB90F347CE(S), MB90F349E(S), MB90F349CE(S)	MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90346E(S), MB90346CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S)
Type	Evaluation products	Flash memory products	MASK ROM products
CPU	F ² MC-16LX CPU		
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (4 MHz osc. PLL × 6)		
ROM	External	512 Kbytes : MB90F345E(S), MB90F345CE(S) 256 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 128 Kbytes : MB90F347E(S), MB90F347CE(S) 64 Kbytes : MB90F346E(S), MB90F346CE(S)	256 Kbytes : MB90342E(S), MB90342CE(S), MB90349E(S), MB90349CE(S) 128 Kbytes : MB90341E(S), MB90341CE(S), MB90347E(S), MB90347CE(S), MB90348E(S), MB90348CE(S) 64 Kbytes : MB90346E(S), MB90346CE(S)
RAM	30 Kbytes	20 Kbytes : MB90F345E(S), MB90F345CE(S) 16 Kbytes : MB90F342E(S), MB90F342CE(S), MB90F349E(S), MB90F349CE(S) 6 Kbytes : MB90F347E(S), MB90F347CE(S) 2 Kbytes : MB90F346E(S), MB90F346CE(S)	16 Kbytes : MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S) 6 Kbytes : MB90347E(S), MB90347CE(S) 2 Kbytes : MB90346E(S), MB90346CE(S)
Emulator-specific power supply*	Yes	—	
Technology	0.35 μm CMOS with regulator for built-in power supply	0.35 μm CMOS with built-in power supply regulator + Flash memory with Charge pump for programming voltage	
Operating voltage range	5 V ± 10%	3.5 V to 5.5 V : When normal operating (not using A/D converter) 4.0 V to 5.5 V : When using the A/D converter/Flash programming 4.5 V to 5.5 V : When using the external bus	
Temperature range	—	−40°C to +105°C	
Package	PGA-299	QFP-100, LQFP-100	
LIN-UART	5 channels	4 channels	
	Wide range of baud rate settings using a dedicated baud rate generator (reload timer) Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device		
I ² C (400 kbps)	2 channels	Devices with a C suffix in the part number : 2 channels Devices without a C suffix in the part number : —	

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Pin No.		Pin name	I/O Circuit type*3	Function
QFP100*1	LQFP100*2			
33	31	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV _{CC} .
34	32	AVRL	K	Lower reference voltage input pin for the A/D Converter
35	33	AV _{SS}	K	Analog GND pin for the A/D Converter
36 to 43	34 to 41	P60 to P67	I	General purpose I/O pins.
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, 2, 4, 6, 8, A, C, E		Output pins for PPGs
44	42	V _{SS}	—	GND pin
45 to 50	43 to 48	P70 to P75	I	General purpose I/O pins.
		AN16 to AN21		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT0 to INT5		External interrupt request input pins
51	49	MD2	D	Input pin for specifying the operating mode.
52, 53	50, 51	MD1, MD0	C	Input pins for specifying the operating mode.
54	52	RST	E	Reset input pin
55, 56	53, 54	P76, P77	I	General purpose I/O pins.
		AN22, AN23		Analog input pins for the A/D converter (devices with a C suffix in the part number)
		INT6, INT7		External interrupt request input pins
57	55	P80	F	General purpose I/O pin.
		TIN0		Event input pin for the reload timer
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin
58	56	P81	F	General purpose I/O pin.
		TOT0		Output pin for the reload timer
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin
59	57	P82	M	General purpose I/O pin.
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer
		INT14R		External interrupt request input pin
60	58	P83	F	General purpose I/O pin.
		SOT0		Serial data output pin for UART0
		TOT2		Output pin for the reload timer

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5. Handling Devices

1. Preventing latch-up

CMOS IC may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC} , AV_{RH}) exceed the digital power-supply voltage.

2. Handling unused pins

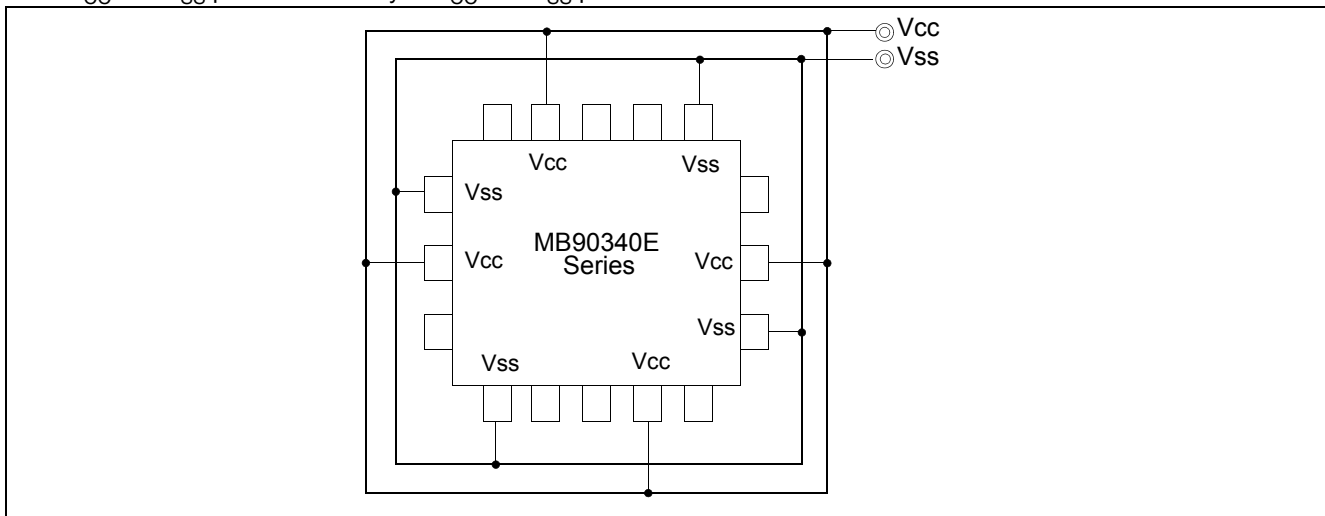
Leaving unused input terminals open may lead to permanent damage due to malfunction and latch-up; pull up or pull down the terminals through the resistors of 2 k Ω or more.

3. Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent malfunction such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally. Connect V_{CC} and V_{SS} pins to the device from the current supply source at a possibly low impedance.

- As a measure against power supply noise, it is recommended to connect a capacitor of about 0.1 μ F as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



4. Mode Pins (MD0 to MD2)

Connect the mode pins directly to V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

5. Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , $AVRH$, $AVRL$) and analog inputs ($AN0$ to $AN23$) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed $AVRH$ or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

6. Connection of Unused A/D Converter Pins when the A/D Converter is Used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

7. Crystal Oscillator Circuit

The X0, X1 pins and X0A, X1A pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

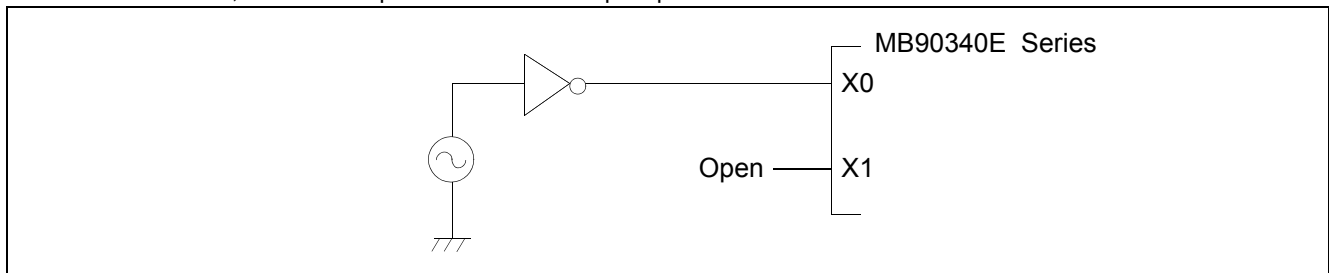
For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

8. Pull-up/down resistors

The MB90340E Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

9. Using external clock

To use an external clock, drive the X0 pin and leave the X1 pin open.



10. Precautions when not using a sub clock signal

If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

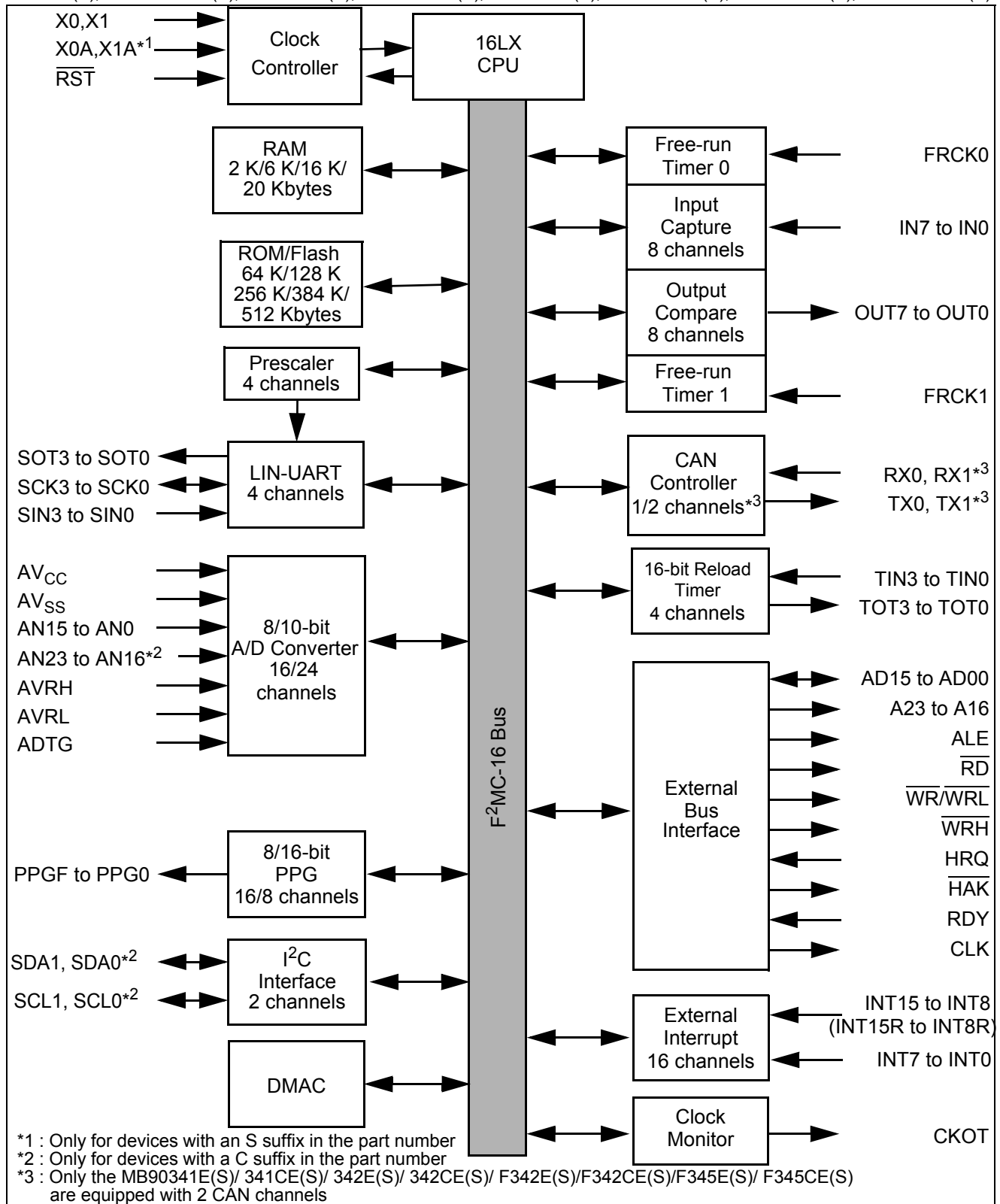
11. Notes on operation in PLL clock mode

If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

12. Notes on Power-On

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50 μ s or more (0.2 V to 2.7 V)

■ MB90341E(S), MB90341CE(S), MB90342E(S), MB90342CE(S), MB90F342E(S), MB90F342CE(S), MB90F345E(S), MB90F345CE(S), MB90346E(S), MB90346CE(S), MB90F346E(S), MB90F346CE(S), MB90347E(S), MB90347CE(S), MB90F347E(S), MB90F347CE(S), MB90348E(S), MB90348CE(S), MB90349E(S), MB90349CE(S), MB90F349E(S), MB90F349CE(S)



8. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
000000 _H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX _B
000001 _H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX _B
000002 _H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX _B
000003 _H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX _B
000004 _H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX _B
000005 _H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX _B
000006 _H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX _B
000007 _H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX _B
000008 _H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX _B
000009 _H	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXXX _B
00000A _H	Port A Data Register	PDRA	R/W	Port A	XXXXXXXX _B
00000B _H	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	1111111 _B
00000C _H	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	1111111 _B
00000D _H	Port 7 Analog Input Enable Register	ADER7	R/W	Port 7, A/D	1111111 _B
00000E _H	Input Level Select Register 0	ILSR0	R/W	Ports	XXXXXXXX _B
00000F _H	Input Level Select Register 1	ILSR1	R/W	Ports	XXXX0XXX _B
000010 _H	Port 0 Direction Register	DDR0	R/W	Port 0	0000000 _B
000011 _H	Port 1 Direction Register	DDR1	R/W	Port 1	0000000 _B
000012 _H	Port 2 Direction Register	DDR2	R/W	Port 2	0000000 _B
000013 _H	Port 3 Direction Register	DDR3	R/W	Port 3	0000000 _B
000014 _H	Port 4 Direction Register	DDR4	R/W	Port 4	0000000 _B
000015 _H	Port 5 Direction Register	DDR5	R/W	Port 5	0000000 _B
000016 _H	Port 6 Direction Register	DDR6	R/W	Port 6	0000000 _B
000017 _H	Port 7 Direction Register	DDR7	R/W	Port 7	0000000 _B
000018 _H	Port 8 Direction Register	DDR8	R/W	Port 8	0000000 _B
000019 _H	Port 9 Direction Register	DDR9	R/W	Port 9	0000000 _B
00001A _H	Port A Direction Register	DDRA	R/W	Port A	00000100 _B
00001B _H	Reserved				
00001C _H	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	0000000 _B
00001D _H	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	0000000 _B
00001E _H	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	0000000 _B
00001F _H	Port 3 Pull-up Control Register	PUCR3	W, R/W	Port 3	0000000 _B

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Address	Register	Abbreviation	Access	Resource name	Initial value
007900 _H	Reload Register L0	PRL0	R/W	16-bit PPG 0/1	XXXXXXXX _B
007901 _H	Reload Register H0	PRLH0	R/W		XXXXXXXX _B
007902 _H	Reload Register L1	PRL1	R/W		XXXXXXXX _B
007903 _H	Reload Register H1	PRLH1	R/W		XXXXXXXX _B
007904 _H	Reload Register L2	PRL2	R/W	16-bit PPG 2/3	XXXXXXXX _B
007905 _H	Reload Register H2	PRLH2	R/W		XXXXXXXX _B
007906 _H	Reload Register L3	PRL3	R/W		XXXXXXXX _B
007907 _H	Reload Register H3	PRLH3	R/W		XXXXXXXX _B
007908 _H	Reload Register L4	PRL4	R/W	16-bit PPG 4/5	XXXXXXXX _B
007909 _H	Reload Register H4	PRLH4	R/W		XXXXXXXX _B
00790A _H	Reload Register L5	PRL5	R/W		XXXXXXXX _B
00790B _H	Reload Register H5	PRLH5	R/W		XXXXXXXX _B
00790C _H	Reload Register L6	PRL6	R/W	16-bit PPG 6/7	XXXXXXXX _B
00790D _H	Reload Register H6	PRLH6	R/W		XXXXXXXX _B
00790E _H	Reload Register L7	PRL7	R/W		XXXXXXXX _B
00790F _H	Reload Register H7	PRLH7	R/W		XXXXXXXX _B
007910 _H	Reload Register L8	PRL8	R/W	16-bit PPG 8/9	XXXXXXXX _B
007911 _H	Reload Register H8	PRLH8	R/W		XXXXXXXX _B
007912 _H	Reload Register L9	PRL9	R/W		XXXXXXXX _B
007913 _H	Reload Register H9	PRLH9	R/W		XXXXXXXX _B
007914 _H	Reload Register LA	PRLA	R/W	16-bit PPG A/B	XXXXXXXX _B
007915 _H	Reload Register HA	PRLHA	R/W		XXXXXXXX _B
007916 _H	Reload Register LB	PRLB	R/W		XXXXXXXX _B
007917 _H	Reload Register HB	PRLHB	R/W		XXXXXXXX _B
007918 _H	Reload Register LC	PRLC	R/W	16-bit PPG C/D	XXXXXXXX _B
007919 _H	Reload Register HC	PRLHC	R/W		XXXXXXXX _B
00791A _H	Reload Register LD	PRLD	R/W		XXXXXXXX _B
00791B _H	Reload Register HD	PRLHD	R/W		XXXXXXXX _B
00791C _H	Reload Register LE	PRLLE	R/W	16-bit PPG E/F	XXXXXXXX _B
00791D _H	Reload Register HE	PRLHE	R/W		XXXXXXXX _B
00791E _H	Reload Register LF	PRLLF	R/W		XXXXXXXX _B
00791F _H	Reload Register HF	PRLHF	R/W		XXXXXXXX _B
007920 _H	Input Capture 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
007921 _H	Input Capture 0	IPCP0	R		XXXXXXXX _B
007922 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B
007923 _H	Input Capture 1	IPCP1	R		XXXXXXXX _B

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Address	Register	Abbreviation	Access	Resource name	Initial value
0079E0 _H	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	XXXXXXXX _B
0079E1 _H	Detect Address Setting 0	PADR0	R/W		XXXXXXXX _B
0079E2 _H	Detect Address Setting 0	PADR0	R/W		XXXXXXXX _B
0079E3 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E4 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E5 _H	Detect Address Setting 1	PADR1	R/W		XXXXXXXX _B
0079E6 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E7 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E8 _H	Detect Address Setting 2	PADR2	R/W		XXXXXXXX _B
0079E9 _H to 0079EF _H	Reserved				
0079F0 _H	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	XXXXXXXX _B
0079F1 _H	Detect Address Setting 3	PADR3	R/W		XXXXXXXX _B
0079F2 _H	Detect Address Setting 3	PADR3	R/W		XXXXXXXX _B
0079F3 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F4 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F5 _H	Detect Address Setting 4	PADR4	R/W		XXXXXXXX _B
0079F6 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F7 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F8 _H	Detect Address Setting 5	PADR5	R/W		XXXXXXXX _B
0079F9 _H to 0079FF _H	Reserved				
007A00 _H to 007AFF _H	Reserved for CAN Controller 0. Refer to “CAN Controllers				
007B00 _H to 007BFF _H	Reserved for CAN Controller 0. Refer to “CAN Controllers”				
007C00 _H to 007CFF _H	Reserved for CAN Controller 1. Refer to “CAN Controllers”				
007D00 _H to 007DFF _H	Reserved for CAN Controller 1. Refer to “CAN Controllers”				
007E00 _H to 007FFF _H	Reserved				

Note:

- Initial value of “X” represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading “X”.

List of Message Buffers (ID Registers) (2)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A40 _H	007C40 _H	ID Register 8	IDR8	R/W	XXXXXXXX _B XXXXXXXX _B
007A41 _H	007C41 _H				XXXXXXXX _B XXXXXXXX _B
007A42 _H	007C42 _H				
007A43 _H	007C43 _H				
007A44 _H	007C44 _H	ID Register 9	IDR9	R/W	XXXXXXXX _B XXXXXXXX _B
007A45 _H	007C45 _H				XXXXXXXX _B XXXXXXXX _B
007A46 _H	007C46 _H				
007A47 _H	007C47 _H				
007A48 _H	007C48 _H	ID Register 10	IDR10	R/W	XXXXXXXX _B XXXXXXXX _B
007A49 _H	007C49 _H				XXXXXXXX _B XXXXXXXX _B
007A4A _H	007C4A _H				
007A4B _H	007C4B _H				
007A4C _H	007C4C _H	ID Register 11	IDR11	R/W	XXXXXXXX _B XXXXXXXX _B
007A4D _H	007C4D _H				XXXXXXXX _B XXXXXXXX _B
007A4E _H	007C4E _H				
007A4F _H	007C4F _H				
007A50 _H	007C50 _H	ID Register 12	IDR12	R/W	XXXXXXXX _B XXXXXXXX _B
007A51 _H	007C51 _H				XXXXXXXX _B XXXXXXXX _B
007A52 _H	007C52 _H				
007A53 _H	007C53 _H				
007A54 _H	007C54 _H	ID Register 13	IDR13	R/W	XXXXXXXX _B XXXXXXXX _B
007A55 _H	007C55 _H				XXXXXXXX _B XXXXXXXX _B
007A56 _H	007C56 _H				
007A57 _H	007C57 _H				
007A58 _H	007C58 _H	ID Register 14	IDR14	R/W	XXXXXXXX _B XXXXXXXX _B
007A59 _H	007C59 _H				XXXXXXXX _B XXXXXXXX _B
007A5A _H	007C5A _H				
007A5B _H	007C5B _H				
007A5C _H	007C5C _H	ID Register 15	IDR15	R/W	XXXXXXXX _B XXXXXXXX _B
007A5D _H	007C5D _H				XXXXXXXX _B XXXXXXXX _B
007A5E _H	007C5E _H				
007A5F _H	007C5F _H				

List of Message Buffers (DLC Registers and Data Registers) (1)

Address		Register	Abbreviation	Access	Initial Value
CAN0	CAN1				
007A60 _H	007C60 _H	DLC Register 0	DLCR0	R/W	XXXXXXXX _B
007A61 _H	007C61 _H				
007A62 _H	007C62 _H				
007A63 _H	007C63 _H	DLC Register 1	DLCR1	R/W	XXXXXXXX _B
007A64 _H	007C64 _H				
007A65 _H	007C65 _H	DLC Register 2	DLCR2	R/W	XXXXXXXX _B
007A66 _H	007C66 _H				
007A67 _H	007C67 _H	DLC Register 3	DLCR3	R/W	XXXXXXXX _B
007A68 _H	007C68 _H				
007A69 _H	007C69 _H	DLC Register 4	DLCR4	R/W	XXXXXXXX _B
007A6A _H	007C6A _H				
007A6B _H	007C6B _H	DLC Register 5	DLCR5	R/W	XXXXXXXX _B
007A6C _H	007C6C _H				
007A6D _H	007C6D _H	DLC Register 6	DLCR6	R/W	XXXXXXXX _B
007A6E _H	007C6E _H				
007A6F _H	007C6F _H	DLC Register 7	DLCR7	R/W	XXXXXXXX _B
007A70 _H	007C70 _H				
007A71 _H	007C71 _H	DLC Register 8	DLCR8	R/W	XXXXXXXX _B
007A72 _H	007C72 _H				
007A73 _H	007C73 _H	DLC Register 9	DLCR9	R/W	XXXXXXXX _B
007A74 _H	007C74 _H				
007A75 _H	007C75 _H	DLC Register 10	DLCR10	R/W	XXXXXXXX _B
007A76 _H	007C76 _H				
007A77 _H	007C77 _H	DLC Register 11	DLCR11	R/W	XXXXXXXX _B
007A78 _H	007C78 _H				
007A79 _H	007C79 _H	DLC Register 12	DLCR12	R/W	XXXXXXXX _B
007A7A _H	007C7A _H				
007A7B _H	007C7B _H	DLC Register 13	DLCR13	R/W	XXXXXXXX _B
007A7C _H	007C7C _H				
007A7D _H	007C7D _H	DLC Register 14	DLCR14	R/W	XXXXXXXX _B
007A7E _H	007C7E _H				
007A7F _H	007C7F _H	DLC Register 15	DLCR15	R/W	XXXXXXXX _B

11.3 DC Characteristics

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{IHS}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{IHA}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Port inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	$V_{CC} + 0.3$	V	Port inputs if TTL input levels are selected
	V_{IHS}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{IHI}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{IHM}	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Port inputs if CMOS hysteresis input levels are selected (except P12, P44, P45, P46, P47, P50, P82, P85)
	V_{ILA}	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Port inputs if Automotive input levels are selected
	V_{ILT}	—	—	$V_{SS} - 0.3$	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P12, P50, P82, P85 inputs if CMOS input levels are selected
	V_{ILI}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P44, P45, P46, P47 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	$\overline{\text{RST}}$ input pin (CMOS hysteresis)
	V_{ILM}	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	V_{OHI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output L voltage	V_{OL}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Output L voltage	V_{OLI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 3.0\text{ mA}$	—	—	0.4	V	

(Continued)

(Continued)

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	—	$V_{CC} = 5.5\text{ V}$, $V_{SS} < V_I < V_{CC}$	-1	—	+1	μA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{\text{RST}}$	—	25	50	100	$\text{k}\Omega$	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	$\text{k}\Omega$	Except Flash memory devices
Power supply current*	I_{CC}	V_{CC}	$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At normal operation.	—	55	70	mA	
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At writing Flash memory.	—	70	85	mA	Flash memory devices
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At erasing Flash memory.	—	75	90	mA	Flash memory devices
	I_{CCS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, In Sleep mode.	—	25	35	mA	
	I_{CTS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 2 MHz, In Main Timer mode	—	0.3	0.8	mA	
	$I_{CTSPLL6}$		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, In PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In sub operation $T_A = +25^{\circ}\text{C}$	—	70	140	μA	
	I_{CCLS}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In sub sleep $T_A = +25^{\circ}\text{C}$	—	20	50	μA	
	I_{CCT}		$V_{CC} = 5.0\text{ V}$ Internal frequency : 8 kHz, In watch mode $T_A = +25^{\circ}\text{C}$	—	10	35	μA	
	I_{CCH}		$V_{CC} = 5.0\text{ V}$, In Stop mode, $T_A = +25^{\circ}\text{C}$	—	7	25	μA	
Input capacitance	C_{IN}	Other than C, AV_{CC} , AV_{SS} , $AVRH$, $AVRL$, V_{CC} , V_{SS}	—	—	5	15	pF	

* : The power supply current is measured with an external clock.

11.4 AC Characteristics

11.4.1 Clock Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

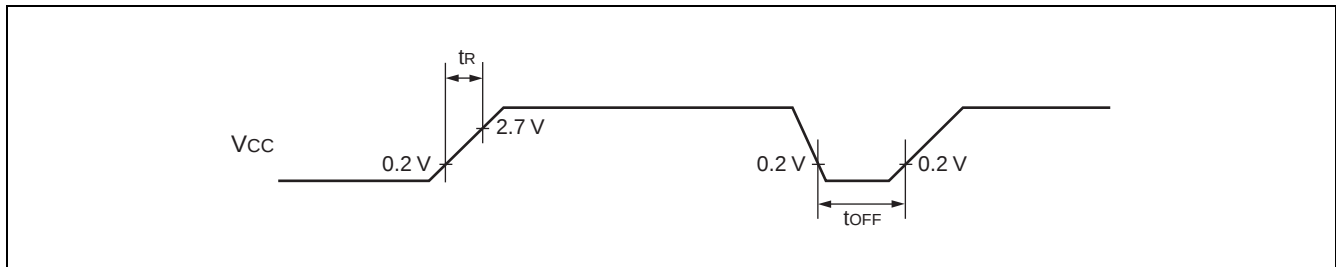
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	When using an oscillation circuit
			4	—	16	MHz	PLL multiplied by 1 When using an oscillation circuit
			4	—	12	MHz	PLL multiplied by 2 When using an oscillation circuit
			4	—	8	MHz	PLL multiplied by 3 When using an oscillation circuit
			4	—	6	MHz	PLL multiplied by 4 When using an oscillation circuit
			—	—	4	MHz	PLL multiplied by 6 When using an oscillation circuit
			3	—	24	MHz	When using an external clock*
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0, X1	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	When using main clock
	t_{CPL}	—	20	122.1	—	μs	When using sub clock

* : When selecting the PLL clock, the range of clock frequency is limited. Use this product within the range as mentioned in "Relation between the external clock frequency and machine clock frequency".

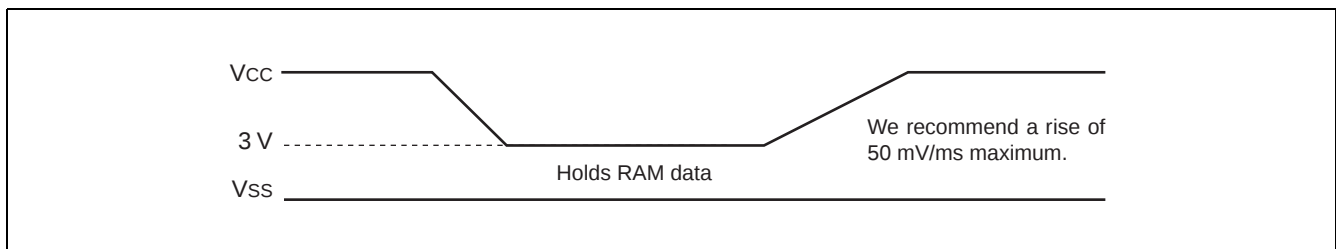
11.4.3 Power On Reset

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}	—	1	—	ms	Waiting time until power-on



Note: : If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



11.4.4 Clock Output Timing

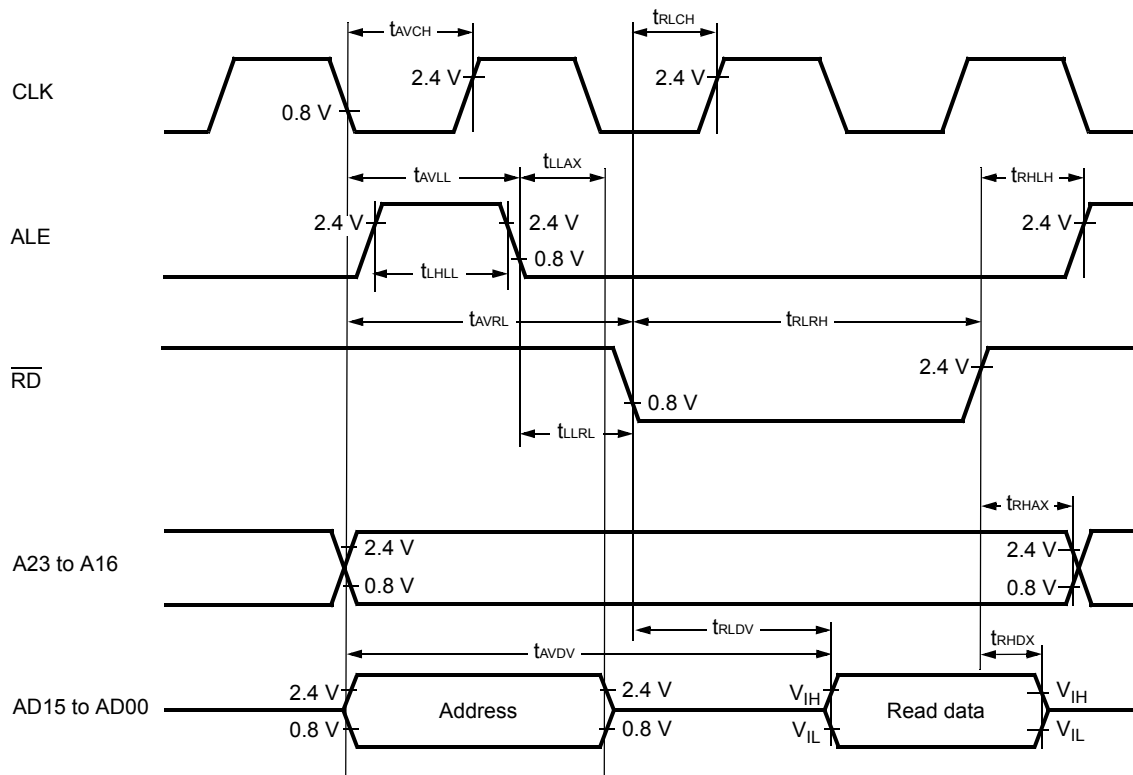
($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	$f_{CP} = 16\text{ MHz}$
				41.67	—	ns	$f_{CP} = 24\text{ MHz}$
CLK $\uparrow \rightarrow$ CLK $\downarrow$	t_{CHCL}	CLK	—	20	—	ns	$f_{CP} = 16\text{ MHz}$
				13	—	ns	$f_{CP} = 24\text{ MHz}$

11.4.5 Bus Timing (Read)

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 10$	—	ns
Valid address → ALE ↓ time	t_{AVLL}	ALE, A23 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns
ALE ↓ → Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns
Valid address → RD ↓ time	t_{AVRL}	A23 to A16, AD15 to AD00, $\overline{\text{RD}}$		$t_{CP} - 15$	—	ns
Valid address → Valid data input	t_{AVDV}	A23 to A16, AD15 to AD00		—	$5 t_{CP}/2 - 60$	ns
$\overline{\text{RD}}$ pulse width	t_{RLRH}	$\overline{\text{RD}}$		$3 t_{CP}/2 - 20$	—	ns
$\overline{\text{RD}}$ ↓ → Valid data input	t_{RLDV}	$\overline{\text{RD}}$, AD15 to AD00		—	$3 t_{CP}/2 - 50$	ns
$\overline{\text{RD}}$ ↑ → Data hold time	t_{RHDX}	$\overline{\text{RD}}$, AD15 to AD00		0	—	ns
$\overline{\text{RD}}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{\text{RD}}$, ALE		$t_{CP}/2 - 15$	—	ns
$\overline{\text{RD}}$ ↑ → Address valid time	t_{RHAX}	$\overline{\text{RD}}$, A23 to A16		$t_{CP}/2 - 10$	—	ns
Valid address → CLK ↑ time	t_{AVCH}	A23 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns
$\overline{\text{RD}}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{\text{RD}}$, CLK		$t_{CP}/2 - 15$	—	ns
ALE ↓ → $\overline{\text{RD}}$ ↓ time	t_{LLRL}	ALE, $\overline{\text{RD}}$		$t_{CP}/2 - 15$	—	ns



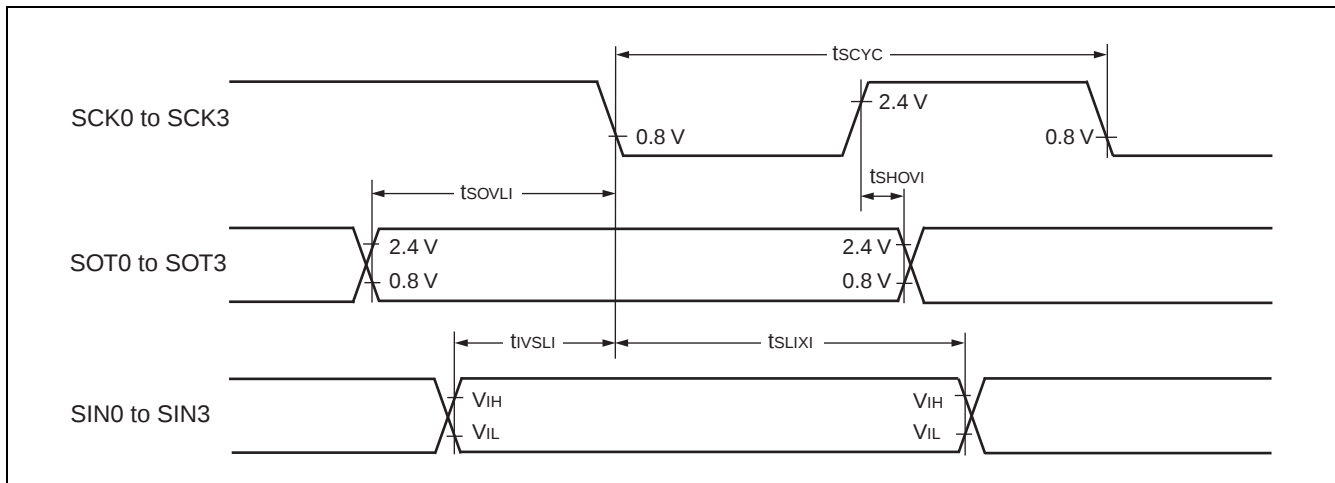
■ Bit setting: ESCR:SCES = 0, ECCR:SCDE = 1

($T_A = -40^\circ\text{C}$ to $+105^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = 0\text{ V}$)

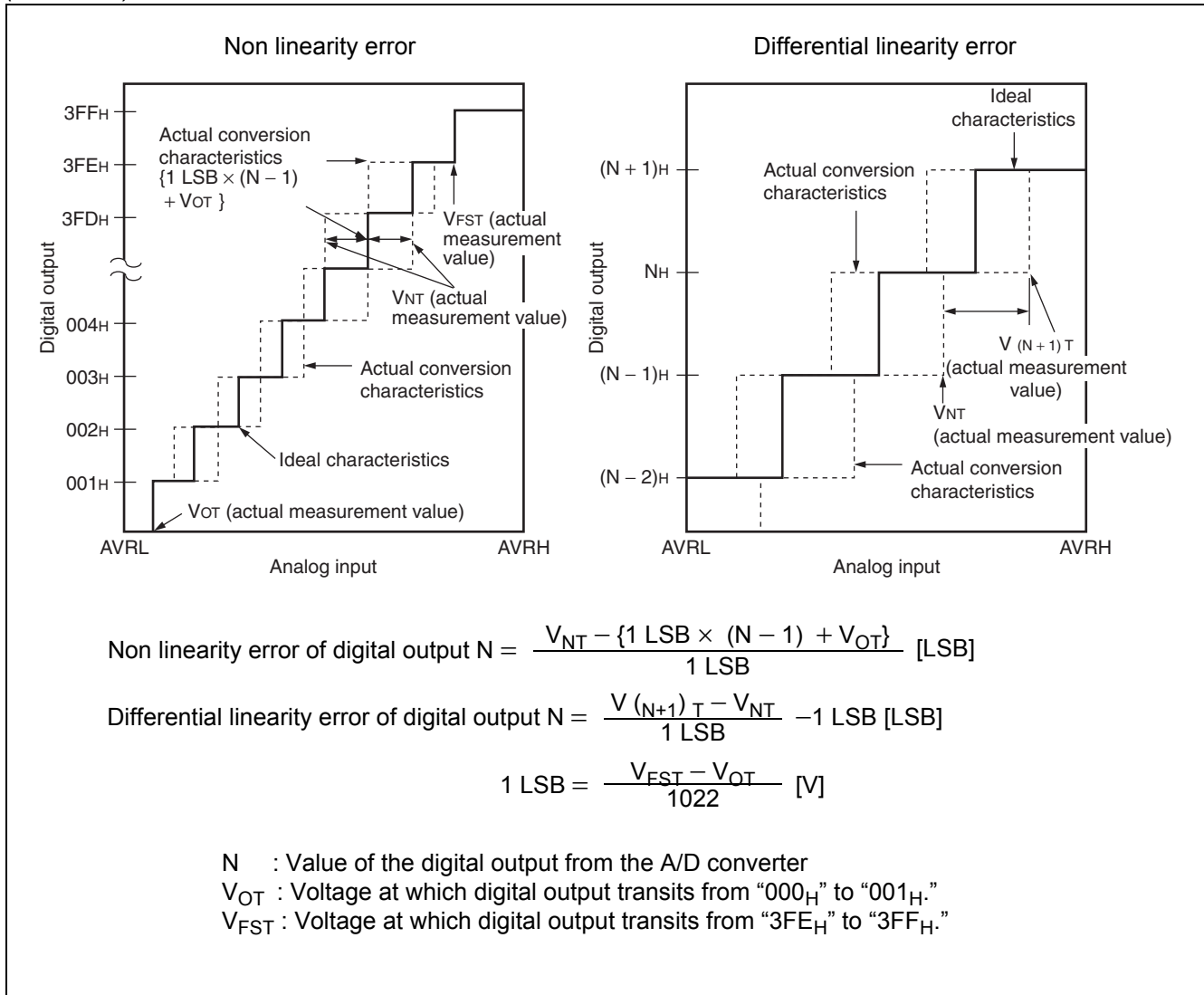
Parameter	Symbol	Pin	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$5 t_{CP}$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVI}	SCK0 to SCK3, SOT0 to SOT3		-50	+50	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	t_{IVSLI}	SCK0 to SCK3, SIN0 to SIN3		$t_{CP} + 80$	—	ns
SCK $\downarrow \rightarrow$ Valid SIN hold time	t_{SLIXI}	SCK0 to SCK3, SIN0 to SIN3		0	—	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	t_{SOVLI}	SCK0 to SCK3, SOT0 to SOT3		$3 t_{CP} - 70$	—	ns

Note:

- C_L is load capacity value of pins when testing.
- t_{CP} is internal operating clock cycle time (machine clock) . Refer to “Clock Timing”.



(Continued)



11.7 Notes on A/D Converter Section

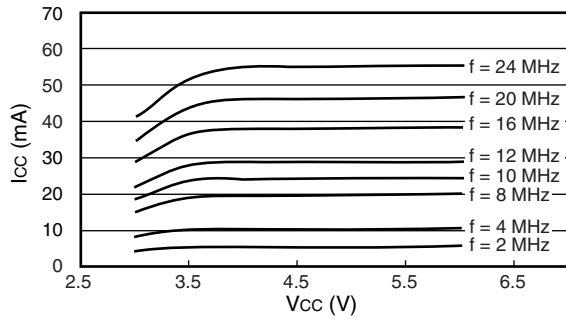
Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 1.5 kΩ or lower (4.0 V ≤ AV_{CC} ≤ 5.5 V,
sampling period = 0.5 μs)

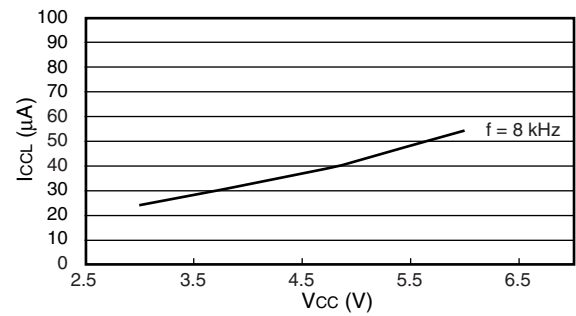
If an external capacitor is used, in consideration of the capacitive voltage dividing effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor be several thousand times greater than the capacitance of the internal capacitor.

■ MB90346E, MB90346ES, MB90346CE, MB90346CES

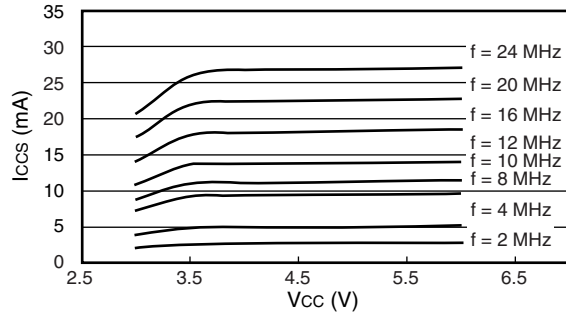
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



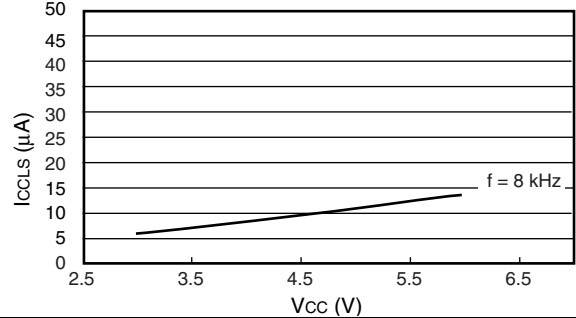
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



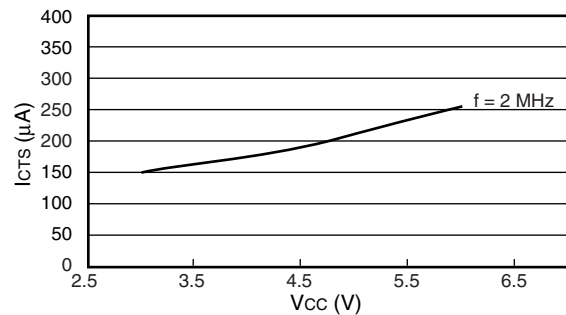
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



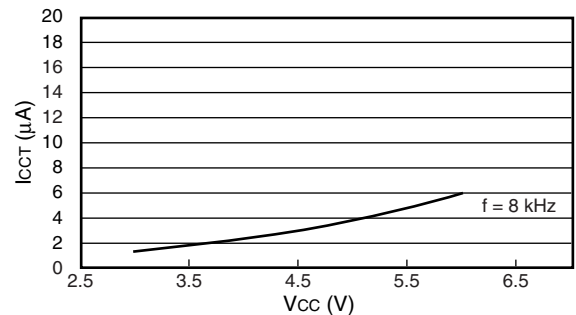
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



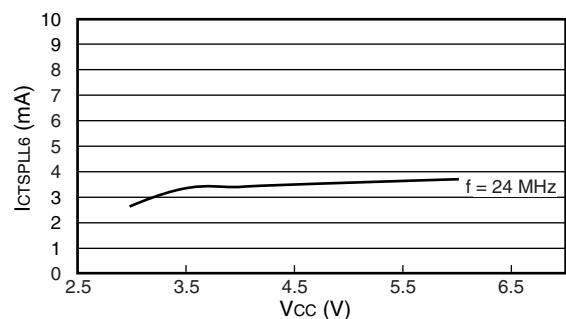
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



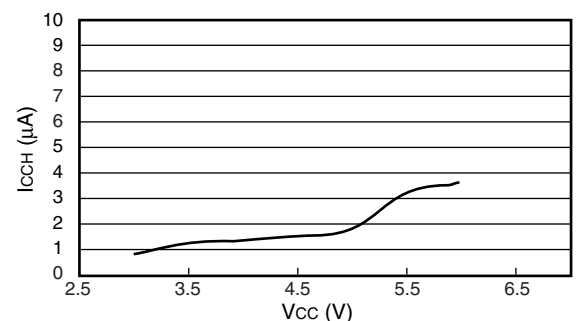
$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency

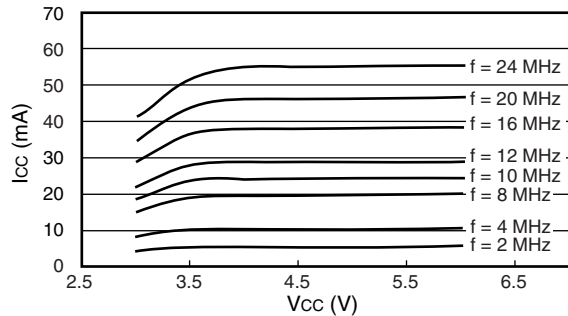


$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped

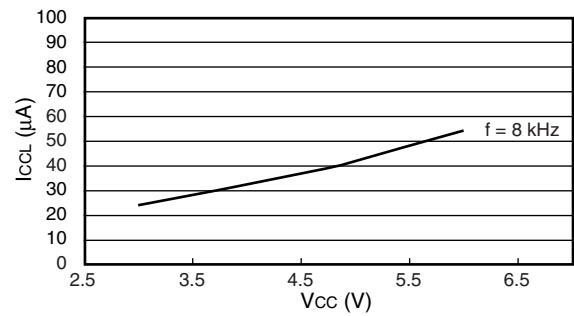


■ MB90347E, MB90347ES, MB90347CE, MB90347CES

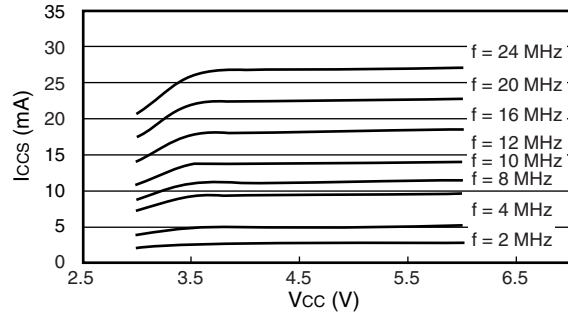
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



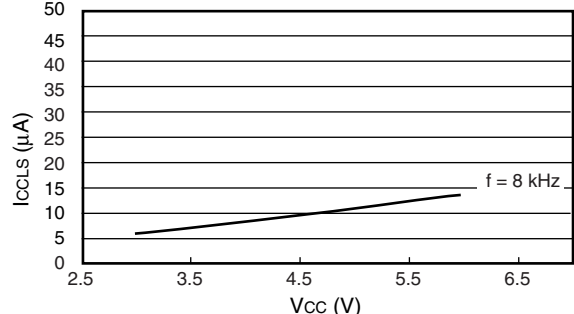
$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



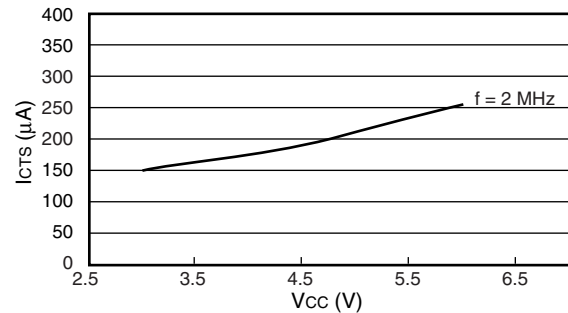
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



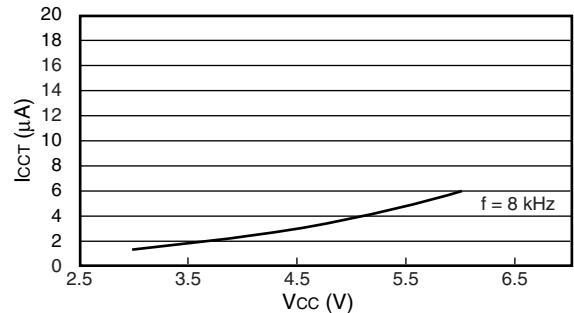
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



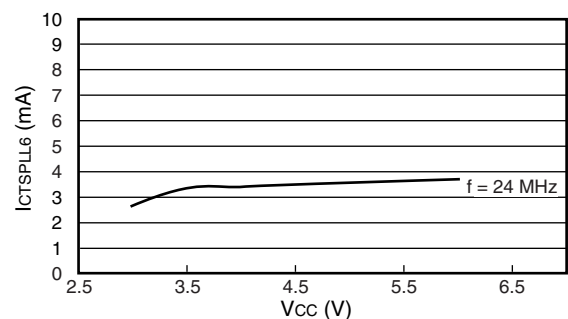
$I_{CTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CTSPLL6} - V_{CC}$
 $T_A = +25^\circ\text{C}$, external clock operation f = Internal operation frequency



$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, stopped

