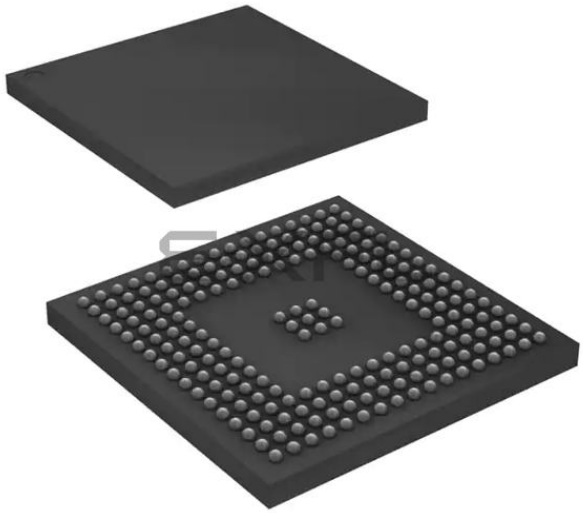
Microchip Technology - AT91SAM9XE512B-CU Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	180MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM, SRAM
Graphics Acceleration	No
Display & Interface Controllers	LCD, Touchscreen
Ethernet	10/100Mbps
SATA	-
USB	USB 2.0 (3)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	217-LFBGA
Supplier Device Package	217-LFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam9xe512b-cu

In all modes and due to a software agreement, register r13 is used as stack pointer.

The use and the function of all the registers described above should obey ARM Procedure Call Standard (APCS) which defines:

- constraints on the use of registers
- stack conventions
- argument passing and result return

For more details, refer to ARM Software Development Kit.

The Thumb state register set is a subset of the ARM state set. The programmer has direct access to:

- Eight general-purpose registers r0–r7
- Stack pointer, SP
- Link register, LR (ARM r14)
- PC
- CPSR

There are banked registers SPs, LRs and SPSRs for each privileged mode (for more details see the ARM9EJ-S Technical Reference Manual, revision r1p2 page 2-12).

10.3.7.1 Status Registers

The ARM9EJ-S core contains one CPSR, and five SPSRs for exception handlers to use. The program status registers:

- hold information about the most recently performed ALU operation
- control the enabling and disabling of interrupts
- set the processor operation mode

Figure 10-2. Status Register Format

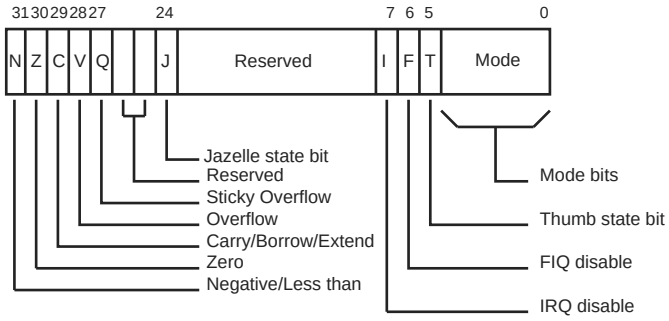


Figure 10-2 shows the status register format, where:

- N: Negative, Z: Zero, C: Carry, and V: Overflow are the four ALU flags
- The Sticky Overflow (Q) flag can be set by certain multiply and fractional arithmetic instructions like QADD, QDADD, QSUB, QDSUB, SMLAxy, and SMLAWy needed to achieve DSP operations.
  The Q flag is sticky in that, when set by an instruction, it remains set until explicitly cleared by an MSR instruction writing to the CPSR. Instructions cannot execute conditionally on the status of the Q flag.
- The J bit in the CPSR indicates when the ARM9EJ-S core is in Jazelle state, where:
  - J = 0: The processor is in ARM or Thumb state, depending on the T bit
  - J = 1: The processor is in Jazelle state.
- Mode: five bits to encode the current processor mode

GP NVM bits can be read using **Get GPNVM Bit** command **(GGPB)**. When a bit set in the Bit Mask is returned, then the corresponding GPNVM bit is set.

Table 13-25. Get General-purpose NVM Bit Command

Read/Write	DR Data
Write	GGPB
Read	Bit Mask

13.3.4.6 Flash Security Bit Command

Security bits can be set using **Set Security Bit** command (SSE). Once the security bit is active, the Fast Flash programming is disabled. No other command can be run. Only an event on the Erase pin can erase the security bit once the contents of the Flash have been erased.

Table 13-26. Set Security Bit Command

Read/Write	DR Data
Write	SSE

Once the security bit is set, it is not possible to access FFPI. The only way to erase the security bit is to erase the Flash.

In order to erase the Flash, the user must perform the following:

- Power-off the chip
- Power-on the chip with TST = 0
- Assert Erase during a period of more than 220 ms
- Power-off the chip

Then it is possible to return to FFPI mode and check that Flash is erased.

13.3.4.7 Memory Write Command

This command is used to perform a write access to any memory location.

The **Memory Write** command **(WRAM)** is optimized for consecutive writes. An internal address buffer is automatically increased.

Table 13-27. Write Command

Read/Write	DR Data
Write	(Number of Words to Write) << 16 | (WRAM)
Write	Address
Write	Memory [address]
Write	Memory [address+4]
Write	Memory [address+8]
Write	Memory [address+(Number of Words to Write - 1)* 4]

Figure 22-3. Memory Connection for an 8-bit Data Bus

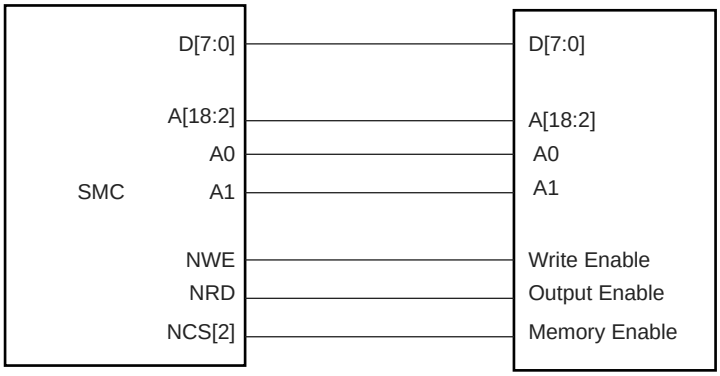


Figure 22-4. Memory Connection for a 16-bit Data Bus

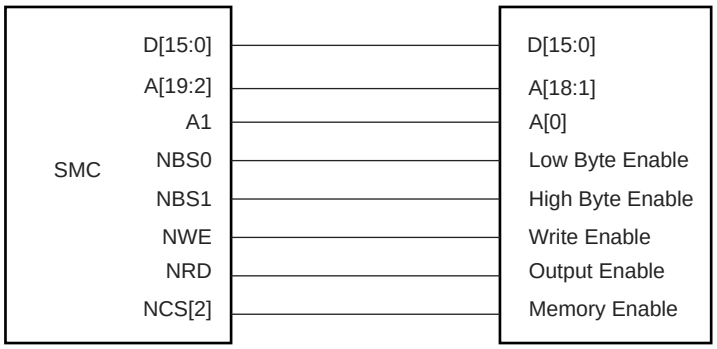
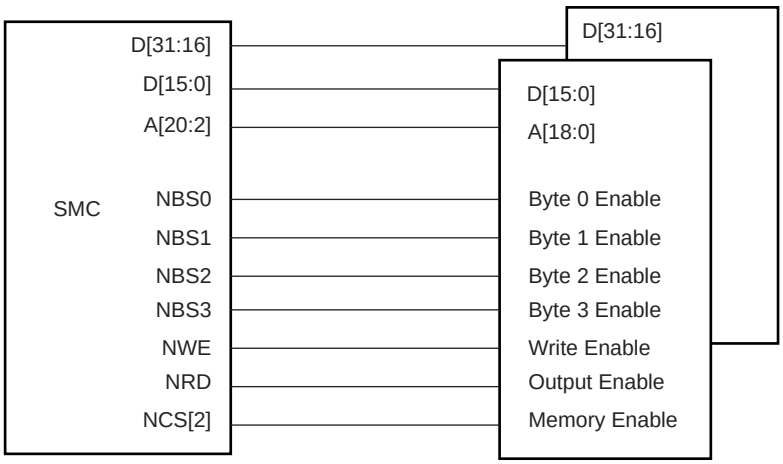


Figure 22-5. Memory Connection for a 32-bit Data Bus



22.8.5 Coding Timing Parameters

All timing parameters are defined for one chip select and are grouped together in one SMC_REGISTER according to their type.

The SMC_SETUP register groups the definition of all setup parameters:

- NRD_SETUP, NCS_RD_SETUP, NWE_SETUP, NCS_WR_SETUP

The SMC_PULSE register groups the definition of all pulse parameters:

- NRD_PULSE, NCS_RD_PULSE, NWE_PULSE, NCS_WR_PULSE

The SMC_CYCLE register groups the definition of all cycle parameters:

- NRD_CYCLE, NWE_CYCLE

Table 22-4 shows how the timing parameters are coded and their permitted range.

Table 22-4. Coding and Range of Timing Parameters

Coded Value	Number of Bits	Effective Value	Permitted Range	
			Coded Value	Effective Value
setup [5:0]	6	128 x setup[5] + setup[4:0]	0 ≤ 31	0 ≤ 128+31
pulse [6:0]	7	256 x pulse[6] + pulse[5:0]	0 ≤ 63	0 ≤ 256+63
cycle [8:0]	9	256 x cycle[8:7] + cycle[6:0]	0 ≤ 127	0 ≤ 256+127 0 ≤ 512+127 0 ≤ 768+127

22.8.6 Reset Values of Timing Parameters

Table 22-8, “Register Mapping,” gives the default value of timing parameters at reset.

22.8.7 Usage Restriction

The SMC does not check the validity of the user-programmed parameters. If the sum of SETUP and PULSE parameters is larger than the corresponding CYCLE parameter, this leads to unpredictable behavior of the SMC.

For read operations:

Null but positive setup and hold of address and NRD and/or NCS can not be guaranteed at the memory interface because of the propagation delay of theses signals through external logic and pads. If positive setup and hold values must be verified, then it is strictly recommended to program non-null values so as to cover possible skews between address, NCS and NRD signals.

For write operations:

If a null hold value is programmed on NWE, the SMC can guarantee a positive hold of address, byte select lines, and NCS signal after the rising edge of NWE. This is true for WRITE_MODE = 1 only. See “Early Read Wait State” on page 207.

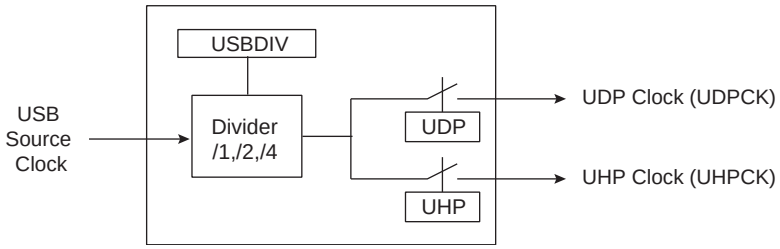
For read and write operations: a null value for pulse parameters is forbidden and may lead to unpredictable behavior.

In read and write cycles, the setup and hold time parameters are defined in reference to the address bus. For external devices that require setup and hold time between NCS and NRD signals (read), or between NCS and NWE signals (write), these setup and hold times must be converted into setup and hold times in reference to the address bus.

When the PLL B output is stable, i.e., the LOCKB is set:

- The USB host clock can be enabled by setting the UHP bit in PMC_SCER. To save power on this peripheral when it is not used, the user can set the UHP bit in PMC_SCDR. The UHP bit in PMC_SCSR gives the activity of this clock. The USB host port require both the 12/48 MHz signal and the Master Clock. The Master Clock may be controlled via the Master Clock Controller.

Figure 27-3. USB Clock Controller



27.5 Peripheral Clock Controller

The Power Management Controller controls the clocks of each embedded peripheral by the way of the Peripheral Clock Controller. The user can individually enable and disable the Master Clock on the peripherals by writing into the Peripheral Clock Enable (PMC_PCER) and Peripheral Clock Disable (PMC_PCDR) registers. The status of the peripheral clock activity can be read in the Peripheral Clock Status Register (PMC_PCSR).

When a peripheral clock is disabled, the clock is immediately stopped. The peripheral clocks are automatically disabled after a reset.

In order to stop a peripheral, it is recommended that the system software wait until the peripheral has executed its last programmed operation before disabling the clock. This is to avoid data corruption or erroneous behavior of the system.

The bit number within the Peripheral Clock Control registers (PMC_PCER, PMC_PCDR, and PMC_PCSR) is the Peripheral Identifier defined at the product level. Generally, the bit number corresponds to the interrupt source number assigned to the peripheral.

27.6 Programmable Clock Output Controller

The PMC controls two signals to be output on external pins PCKx. Each signal can be independently programmed via the PMC_PCKx registers.

PCKx can be independently selected between the Slow clock, the PLL A output, the PLL B output and the main clock by writing the CSS field in PMC_PCKx. Each output signal can also be divided by a power of 2 between 1 and 64 by writing the PRES (Prescaler) field in PMC_PCKx.

Each output signal can be enabled and disabled by writing 1 in the corresponding bit, PCKx of PMC_SCER and PMC_SCDR, respectively. Status of the active programmable output clocks are given in the PCKx bits of PMC_SCSR (System Clock Status Register).

Moreover, like the PCK, a status bit in PMC_SR indicates that the Programmable Clock is actually what has been programmed in the Programmable Clock registers.

As the Programmable Clock Controller does not manage with glitch prevention when switching clocks, it is strongly recommended to disable the Programmable Clock before any configuration change and to re-enable it after the change is actually performed.

27.9.8 PMC Clock Generator Main Clock Frequency Register

Name: CKGR_MCFR

Address: 0xFFFFFC24

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	MAINRDY

15	14	13	12	11	10	9	8
MAINF							

7	6	5	4	3	2	1	0
MAINF							

- **MAINF: Main Clock Frequency**

Gives the number of Main Clock cycles within 16 Slow Clock periods.

- **MAINRDY: Main Clock Ready**

0: MAINF value is not valid or the Main Oscillator is disabled.

1: The Main Oscillator has been enabled previously and MAINF value is available.

28.8.14 AIC End of Interrupt Command Register

Name: AIC_EOICR

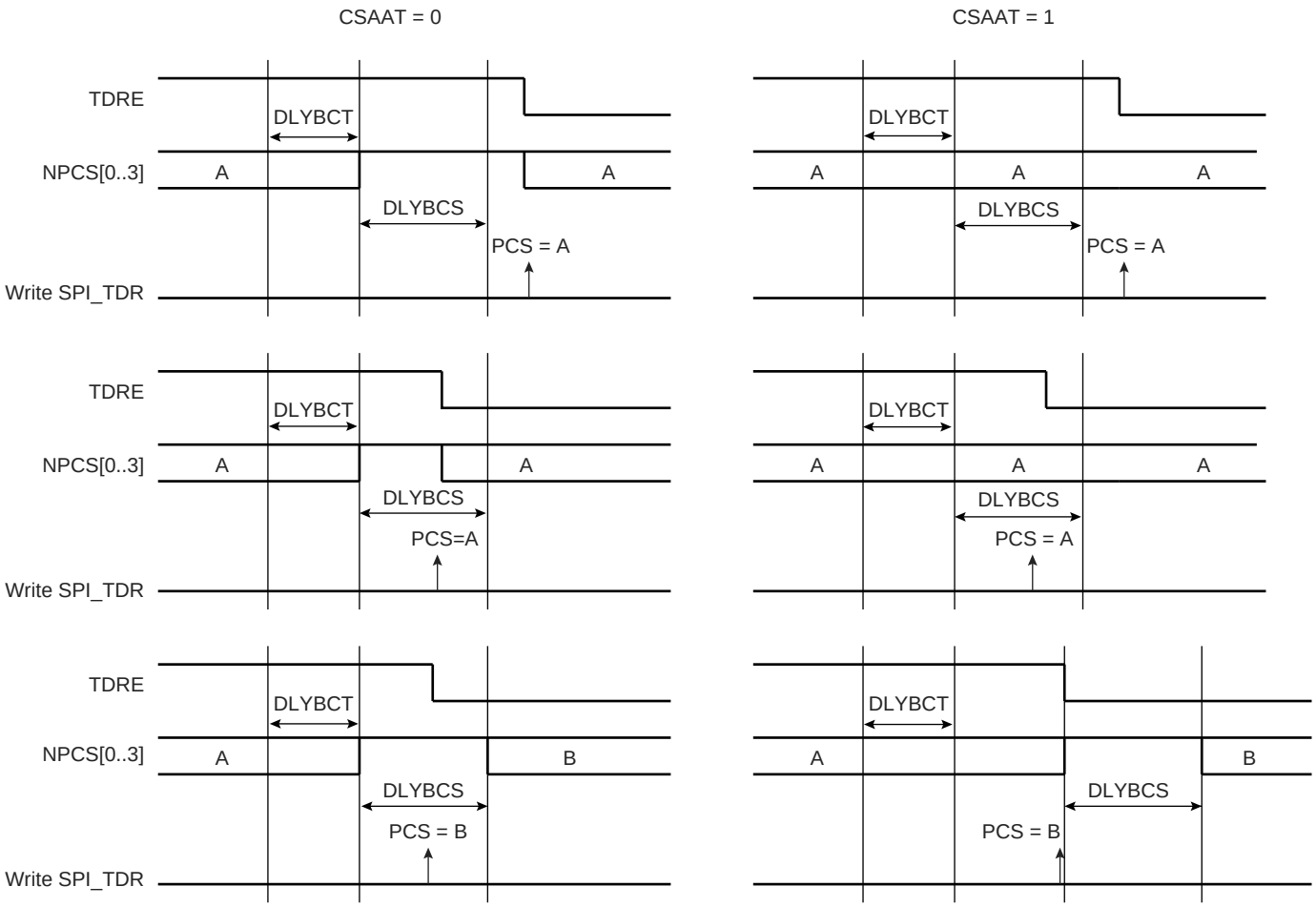
Address: 0xFFFFF130

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

The End of Interrupt Command Register is used by the interrupt routine to indicate that the interrupt treatment is complete. Any value can be written because it is only necessary to make a write to this register location to signal the end of interrupt treatment.

Figure 31-8. Peripheral Deselection



31.6.3.8 Mode Fault Detection

A mode fault is detected when the SPI is programmed in Master Mode and a low level is driven by an external master on the NPCS0/NSS signal. NPCS0, MOSI, MISO and SPCK must be configured in open drain through the PIO controller, so that external pull up resistors are needed to guarantee high level.

When a mode fault is detected, the MODF bit in the SPI_SR is set until the SPI_SR is read and the SPI is automatically disabled until re-enabled by writing the SPIEN bit in the SPI_CR (Control Register) at 1.

By default, the Mode Fault detection circuitry is enabled. The user can disable Mode Fault detection by setting the MODFDIS bit in the SPI Mode Register (SPI_MR).

31.6.4 SPI Slave Mode

When operating in Slave Mode, the SPI processes data bits on the clock provided on the SPI clock pin (SPCK).

The SPI waits for NSS to go active before receiving the serial clock from an external master. When NSS falls, the clock is validated on the serializer, which processes the number of bits defined by the BITS field of the Chip Select Register 0 (SPI_CSR0). These bits are processed following a phase and a polarity defined respectively by the NCPHA and CPOL bits of the SPI_CSR0. Note that BITS, CPOL and NCPHA of the other Chip Select Registers have no effect when the SPI is programmed in Slave Mode.

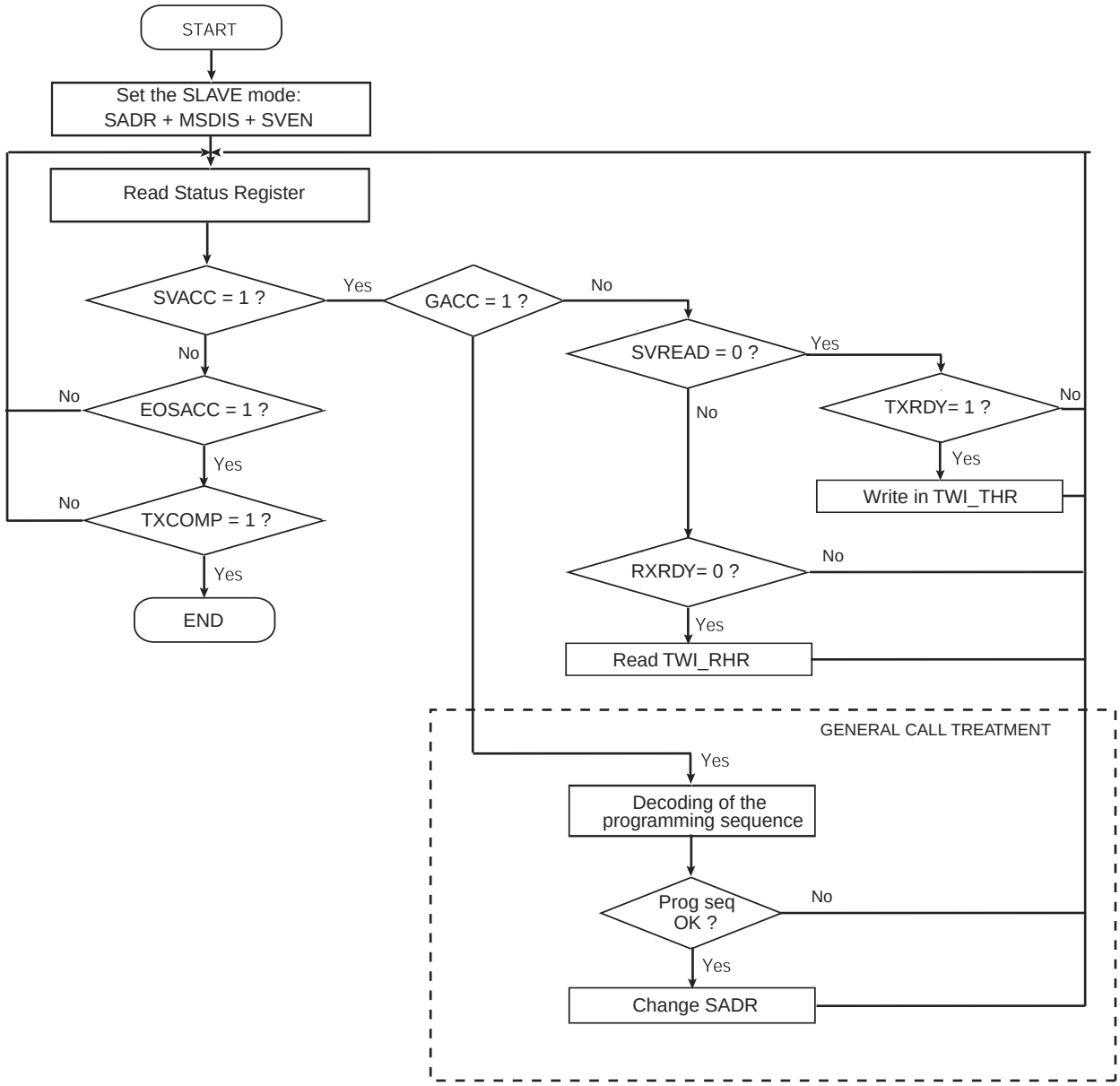
The bits are shifted out on the MISO line and sampled on the MOSI line.

(For more information on BITS field, see also the note below the register bitmap in Section 31.7.9 “SPI Chip Select Register” on page 464.)

32.6.5.6 Read/Write Flowcharts

The flowchart shown in Figure 32-32 gives an example of read and write operations in Slave mode. A polling or interrupt method can be used to check the status bits. The interrupt method requires that the interrupt enable register (TWI_IER) be configured first.

Figure 32-32. Read/Write Flowchart in Slave Mode



33.6.4.7 Protocol T = 1

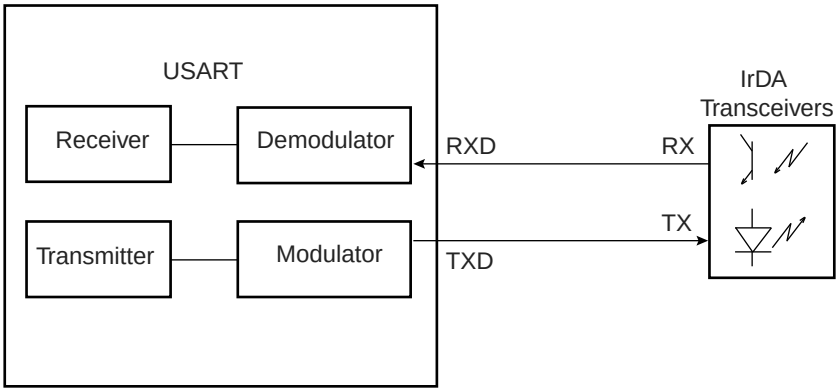
When operating in ISO7816 protocol T = 1, the transmission is similar to an asynchronous format with only one stop bit. The parity is generated when transmitting and checked when receiving. Parity error detection sets the PARE bit in the Channel Status Register (US_CSR).

33.6.5 IrDA Mode

The USART features an IrDA mode supplying half-duplex point-to-point wireless communication. It embeds the modulator and demodulator which allows a glueless connection to the infrared transceivers, as shown in Figure 33-23. The modulator and demodulator are compliant with the IrDA specification version 1.1 and support data transfer speeds ranging from 2.4 Kb/s to 115.2 Kb/s.

The USART IrDA mode is enabled by setting the USART_MODE field in the Mode Register (US_MR) to the value 0x8. The IrDA Filter Register (US_IF) allows configuring the demodulator filter. The USART transmitter and receiver operate in a normal asynchronous mode and all parameters are accessible. Note that the modulator and the demodulator are activated.

Figure 33-23. Connection to IrDA Transceivers



The receiver and the transmitter must be enabled or disabled according to the direction of the transmission to be managed.

To receive IrDA signals, the following needs to be done:

- Disable TX and Enable RX
- Configure the TXD pin as PIO and set it as an output at 0 (to avoid LED emission). Disable the internal pull-up (better for power consumption).
- Receive data

33.7.7 USART Receive Holding Register

Name: US_RHR

Address: 0xFFFB0018 (0), 0xFFFB4018 (1), 0xFFFB8018 (2), 0xFFFD0018 (3), 0xFFFD4018 (4)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
RXSYNH	–	–	–	–	–	–	RXCHR

7	6	5	4	3	2	1	0
RXCHR							

- **RXCHR: Received Character**

Last character received if RXRDY is set.

- **RXSYNH: Received Sync**

0: Last Character received is a Data.

1: Last Character received is a Command.

34.8.1 SSC Control Register

Name: SSC_CR

Address: 0xFFFBC000

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
SWRST	–	–	–	–	–	TXDIS	TXEN
7	6	5	4	3	2	1	0
–	–	–	–	–	–	RXDIS	RXEN

- **RXEN: Receive Enable**

0: No effect.

1: Enables Receive if RXDIS is not set.

- **RXDIS: Receive Disable**

0: No effect.

1: Disables Receive. If a character is currently being received, disables at end of current character reception.

- **TXEN: Transmit Enable**

0: No effect.

1: Enables Transmit if TXDIS is not set.

- **TXDIS: Transmit Disable**

0: No effect.

1: Disables Transmit. If a character is currently being transmitted, disables at end of current character transmission.

- **SWRST: Software Reset**

0: No effect.

1: Performs a software reset. Has priority on any other bit in SSC_CR.

36.9.1 MCI Control Register

Name: MCI_CR

Address: 0xFFFA8000

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
SWRST	–	–	–	PWSDIS	PWSEN	MCIDIS	MCIEN

- **MCIEN: Multi-Media Interface Enable**

0: No effect.

1: Enables the Multi-Media Interface if MCDIS is 0.

- **MCIDIS: Multi-Media Interface Disable**

0: No effect.

1: Disables the Multi-Media Interface.

- **PWSEN: Power Save Mode Enable**

0: No effect.

1: Enables the Power Saving Mode if PWSDIS is 0.

Warning: Before enabling this mode, the user must set a value different from 0 in the PWSDIV field (Mode Register MCI_MR).

- **PWSDIS: Power Save Mode Disable**

0: No effect.

1: Disables the Power Saving Mode.

- **SWRST: Software Reset**

0: No effect.

1: Resets the MCI. A software triggered hardware reset of the MCI interface is performed.

38.6.12 UDP Transceiver Control Register

Name: UDP_TXVC

Address: 0xFFFA4074

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	PUON	TXVDIS
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

WARNING: The UDP peripheral clock in the Power Management Controller (PMC) must be enabled before any read/write operations to the UDP registers including the UDP_TXVC register.

- **TXVDIS: Transceiver Disable**

When UDP is disabled, power consumption can be reduced significantly by disabling the embedded transceiver. This can be done by setting TXVDIS field.

To enable the transceiver, TXVDIS must be cleared.

- **PUON: Pull-up On**

0: The 1.5KΩ integrated pull-up on DP is disconnected.

1: The 1.5 KΩ integrated pull-up on DP is connected.

Note: If the USB pull-up is not connected on DP, the user should not write in any UDP register other than the UDP_TXVC register. This is because if DP and DM are floating at 0, or pulled down, then SE0 is received by the device with the consequence of a USB Reset.

40.3.3 Clocks

The sensor master clock (ISI_MCK) can be generated either by the Advanced Power Management Controller (APMC) through a Programmable Clock output or by an external oscillator connected to the sensor.

None of the sensors embeds a power management controller, so providing the clock by the APMC is a simple and efficient way to control power consumption of the system.

Care must be taken when programming the system clock. The ISI has two clock domains, the system bus clock and the pixel clock provided by sensor. The two clock domains are not synchronized, but the system clock must be faster than pixel clock.

40.3.4 Preview Path

40.3.4.1 Scaling, Decimation (Subsampling)

This module resizes captured 8-bit color sensor images to fit the LCD display format. The resize module performs only downscaling. The same ratio is applied for both horizontal and vertical resize, then a fractional decimation algorithm is applied.

The decimation factor is a multiple of 1/16 and values 0 to 15 are forbidden.

Table 40-6. Decimation Factor

Dec value	0->15	16	17	18	19	...	124	125	126	127
Dec Factor	X	1	1.063	1.125	1.188	...	7.750	7.813	7.875	7.938

Table 40-7. Decimation and Scaler Offset Values

INPUT OUTPUT		352*288	640*480	800*600	1280*1024	1600*1200	2048*1536
VGA 640*480	F	NA	16	20	32	40	51
QVGA 320*240	F	16	32	40	64	80	102
CIF 352*288	F	16	26	33	56	66	85
QCIF 176*144	F	16	53	66	113	133	170

Example:

Input 1280*1024 Output = 640*480

Hratio = 1280/640 = 2

Vratio = 1024/480 = 2.1333

The decimation factor is 2 so 32/16.

41.6.3 ADC Channel Enable Register

Name: ADC_CHER

Address: 0xFFFE0010

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	CH3	CH2	CH1	CH0

- **CHx: Channel x Enable**

0: No effect.

1: Enables the corresponding channel.

Table 42-2. DC Characteristics (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{PULLUP}	Pull-up Resistance	PA0–PA31 PB0–PB31 PC0–PC3 NRTST and NRST		50	100	180	kΩ
		PC4–PC31 V_{DDIOM} in 1.8V range		240		1000	kΩ
		PC4–PC31 V_{DDIOM} in 3.3V range		50		350	kΩ
I_O	Output Current	PA0–PA31 PB0–PB31 PC0–PC3				8	mA
		PC4–PC31 in 3.3V range				2	mA
		PC4–PC31 in 1.8V range				4	mA
I_{SC}	Static Current	On V_{DDCORE} = 1.8V, MCK = 0 Hz, excluding POR All inputs driven TMS, TDI, TCK, NRST = 1	T_A = 25°C		500		µA
			T_A = 85°C			5000	
		On V_{DDBU} = 1.8V, Logic cells consumption, excluding POR All inputs driven WKUP = 0	T_A = 25°C		2		µA
			T_A = 85°C			20	

Table 42-3. Brownout Detector Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOT-}	Threshold Level		1.52	1.55	1.58	V
V_{hys}	Hysteresis	$V_{hys} = V_{BOT+} - V_{BOT-}$		50	65	mV
I_{DD}	Current Consumption	BOD on (GPNVMbit[1] is set)		12	18	µA
		BOD off (GPNVMbit[1] is cleared)			1	µA
t_{START}	Startup Time			100	200	µs

Table 42-4. DC Flash Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{PU}	Power-up delay			30	µs
I_{STDBY}	Standby current			20	µA
I_{CC}	Active current	Read at maximum frequency (access time = 60 ns) VDDCORE = 1.8V		13.0	mA
		Write VDDCORE = 1.8V		7.0	mA

42.6.5 Crystal Characteristics

Table 42-16. Crystal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistor Rs	Fundamental @ 3 MHz			200	Ω
		Fundamental @ 8 MHz			100	
		Fundamental @ 16 MHz			80	
		Fundamental @ 20 MHz			50	
C_m	Motional Capacitance				8	fF
C_{SHUNT}	Shunt Capacitance				7	pF

42.6.6 PLL Characteristics

Table 42-17. PLLA Characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output Frequency	Field CKGR_PLL.OUTA = 00	80		160	MHz
		Field CKGR_PLL.OUTA = 10	150		220	MHz
f_{IN}	Input Frequency		1		32	MHz
I_{PLL}	Current Consumption	Active mode @ 240 MHz		3.6	4.5	mA
		Standby mode			1	µA

Note: 1. Startup time depends on PLL RC filter. A calculation tool is provided by Atmel.

Table 42-18. PLLB Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output Frequency	Field CKGR_PLL.OUTA = 01	70		130	MHz
f_{IN}	Input Frequency		1		5(1)	MHz
I_{PLL}	Current Consumption	Active mode @ 130 MHz			1.2	mA
		Standby mode			1	µA
t_{START}	Startup TIme				1	ms

Note: 1. The embedded filter is optimized for a 2 MHz input frequency. DIVB must be selected to meet this requirement.

46.1.3.2 MCI: SDIO Interrupt does not work with slots other than A

If there is 1-bit data bus width on slots other than slot A, the SDIO interrupt can not be captured. The sample is made on the wrong data line.

Problem Fix/Workaround

None

46.1.3.3 MCI: Data Write Operation and number of bytes

The Data Write operation with a number of bytes less than 12 is impossible.

Problem Fix/Workaround

The PDC counters must always be equal to 12 bytes for data transfers lower than 12 bytes. The BLKLEN or BCNT field are used to specify the real count number.

46.1.3.4 MCI: Flag Reset is not correct in half duplex mode

In half duplex mode, the reset of the flags ENDRX, RXBUFF, ENDTX and TXBUFE can be incorrect. These flags are reset correctly after a PDC channel enable.

Problem Fix/Workaround

Enable the interrupts related to ENDRX, ENDTX, RXBUFF and TXBUFE only after enabling the PDC channel by writing PDC_TXTEN or PDC_RXTEN.

46.1.3.5 MCI: Small Block Reading

In case of a read of a small block (i.e., 5 bytes) by the READ_SINGLE_BLOCK command (CMD17), the DATA FSM may not perform correctly. This occurs if the read transfer is done before the response start bit is sent by the card. It leads to erratic behavior of the NOTBUSY flag and to a false data time-out error, DTOE.

Problem Fix/Workaround

None.

46.1.3.6 MCI: old SDCard Compatibility

Busy line is sampled 2 clock cycles after the command End Bit when the R1B response type is expected. This timing is not strictly defined in SD mode.

This timing is defined with MMC specification 4.1. (R1b Busy Timing)

Problem Fix/Workaround

None.

46.1.4 Reset Controller (RSTC)

46.1.4.1 RSTC: Reset Type Status is wrong at power-up

RSTTYP status in the Reset Controller Status Register is wrong at power-up.

It should be “0” (General Reset) but it is “5” (Brownout Reset). The value is the same if Brownout and Brownout Reset are enabled or not. The BODSTS bit remains correct.

Problem Fix/Workaround

None.

Doc. Rev 6254B	Comments (Continued)	Change Request Ref. (1)
	Section 5.3 “Shutdown Logic Pins”, updated with external pull-up requirement.	rfo
	Debug and Test Section 11.5 “JTAG Port Pins”, added to Debug and Test.	rfo
	Boot Program: Section 12.4.4 “In-Application Programming (IAP) Feature”, added to datasheet.	6190
	AIC: Section 28.6.3 “Interrupt Sources”, Interrupt Source 1, OR-wiring description updated. Section 28.7.5 “Protect Mode”, enabling Debug Control Protect Mode in AIC_DCR register updated. Qualified/Internal on ATP	5191 5193
	DBGU: Section 29.1 “Description”, added to second paragraph; “...two-pin UART can be used as stand-alone...”	5846
	ECC: Section 24.4.3 “ECC Status Register 1” and Section 24.4.4 “ECC Status Register 2”, ECCERRx renamed as MULERRx on bitfields, 2, 18, 22, 26, 30. Section 24.4.1 “ECC Control Register”, added new bitfield: SRST	5542 5543
	EEFC: Section 19.4.2 “EEFC Flash Command Register”, updated FARG bit field description	5302
	ISI: Section 40.4.7 “ISI Preview Register”, updated PREV_VSIZE and PREV_HSIZE with RGB only comments	
	PMC: Section 27.7 “Programming Sequence”, steps 5 and 6: “By default PRES parameter is set to 0.....”	5596
	RSTC: Section 14.3.4.5 “Software Reset” PERRST must be used with PROCRST, except for debug purposes.	5436
	SMC: Section 22.8.5 “Coding Timing Parameters”, “Effective Value” column under “Permitted Range” updated in Table 22-4 on page 206. Section 22.9.3.1 “User Procedure”, instructions regarding configuration parameters of SMC Chip Select added.	5604 5621
	TWI: Section 32.5.1 “I/O Lines”, TWD and TWCK open drain status and condition updated. Programmer interdiction added to TWD and TWCK. Section 32.7.6 “TWI Status Register”, GACC bit description updated.	5343 rfo 5773
	USART: Manchester Encoding/Decoding is available in this implementation of the USART (not visible in 6254A).	5930