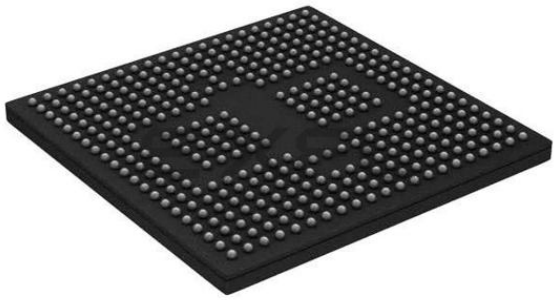

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	XCore
Core Size	32-Bit 32-Core
Speed	4000MIPS
Connectivity	RGMII, USB
Peripherals	-
Number of I/O	176
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	0.95V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	374-LFBGA
Supplier Device Package	374-FBGA (18x18)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xef232-1024-fb374-i40

Table of Contents

Signal	Function					Type	Properties
X2D00		$1A^0$				I/O	IOL, PD
X2D02			$4A^0$	$8A^0$	$16A^0$ $32A^{20}$	I/O	IOL, PD
X2D03			$4A^1$	$8A^1$	$16A^1$ $32A^{21}$	I/O	IOL, PD
X2D04			$4B^0$	$8A^2$	$16A^2$ $32A^{22}$	I/O	IOL, PD
X2D05			$4B^1$	$8A^3$	$16A^3$ $32A^{23}$	I/O	IOL, PD
X2D06			$4B^2$	$8A^4$	$16A^4$ $32A^{24}$	I/O	IOL, PD
X2D07			$4B^3$	$8A^5$	$16A^5$ $32A^{25}$	I/O	IOL, PD
X2D08			$4A^2$	$8A^6$	$16A^6$ $32A^{26}$	I/O	IOL, PD
X2D09			$4A^3$	$8A^7$	$16A^7$ $32A^{27}$	I/O	IOL, PD
X2D11		$1D^0$				I/O	IOL, PD
X2D12		$1E^0$				I/O	IOR, PD
X2D13		$1F^0$				I/O	IOR, PD
X2D14			$4C^0$	$8B^0$	$16A^8$ $32A^{28}$	I/O	IOR, PD
X2D15			$4C^1$	$8B^1$	$16A^9$ $32A^{29}$	I/O	IOR, PD
X2D16	$XL4^4_{in}$		$4D^0$	$8B^2$	$16A^{10}$	I/O	IOR, PD
X2D17	$XL4^3_{in}$		$4D^1$	$8B^3$	$16A^{11}$	I/O	IOR, PD
X2D18	$XL4^2_{in}$		$4D^2$	$8B^4$	$16A^{12}$	I/O	IOR, PD
X2D19	$XL4^1_{in}$		$4D^3$	$8B^5$	$16A^{13}$	I/O	IOR, PD
X2D20			$4C^2$	$8B^6$	$16A^{14}$ $32A^{30}$	I/O	IOR, PD
X2D21			$4C^3$	$8B^7$	$16A^{15}$ $32A^{31}$	I/O	IOR, PD
X2D22		$1G^0$				I/O	IOR, PD
X2D23		$1H^0$				I/O	IOR, PD
X2D24	$XL7^0_{in}$	$1I^0$				I/O	IOR, PD
X2D25	$XL7^0_{out}$	$1J^0$				I/O	IOR, PD
X2D26	$XL7^3_{out}$		$4E^0$	$8C^0$	$16B^0$	I/O	IOR, PD
X2D27	$XL7^4_{out}$		$4E^1$	$8C^1$	$16B^1$	I/O	IOR, PD
X2D28			$4F^0$	$8C^2$	$16B^2$	I/O	IOR, PD
X2D29			$4F^1$	$8C^3$	$16B^3$	I/O	IOR, PD
X2D30			$4F^2$	$8C^4$	$16B^4$	I/O	IOR, PD
X2D31			$4F^3$	$8C^5$	$16B^5$	I/O	IOR, PD
X2D32			$4E^2$	$8C^6$	$16B^6$	I/O	IOR, PD
X2D33			$4E^3$	$8C^7$	$16B^7$	I/O	IOR, PD
X2D34	$XL7^1_{out}$	$1K^0$				I/O	IOR, PD
X2D35	$XL7^2_{out}$	$1L^0$				I/O	IOR, PD
X2D36		$1M^0$		$8D^0$	$16B^8$	I/O	IOL, PD
X2D49	$XL5^4_{in}$				$32A^0$	I/O	IOR, PD
X2D50	$XL5^3_{in}$				$32A^1$	I/O	IOR, PD
X2D51	$XL5^2_{in}$				$32A^2$	I/O	IOR, PD
X2D52	$XL5^1_{in}$				$32A^3$	I/O	IOR, PD
X2D53	$XL5^0_{in}$				$32A^4$	I/O	IOR, PD
X2D54	$XL5^0_{out}$				$32A^5$	I/O	IOR, PD
X2D55	$XL5^1_{out}$				$32A^6$	I/O	IOR, PD
X2D56	$XL5^2_{out}$				$32A^7$	I/O	IOR, PD

(continued)

Signal	Function					Type	Properties
X2D57	$XL5^{3}_{out}$				$32A^{8}$	I/O	IOR, PD
X2D58	$XL5^{4}_{out}$				$32A^{9}$	I/O	IOR, PD
X2D61	$XL6^{4}_{in}$				$32A^{10}$	I/O	IOR, PD
X2D62	$XL6^{3}_{in}$				$32A^{11}$	I/O	IOR, PD
X2D63	$XL6^{2}_{in}$				$32A^{12}$	I/O	IOR, PD
X2D64	$XL6^{1}_{in}$				$32A^{13}$	I/O	IOR, PD
X2D65	$XL6^{0}_{in}$				$32A^{14}$	I/O	IOR, PD
X2D66	$XL6^{0}_{out}$				$32A^{15}$	I/O	IOR, PD
X2D67	$XL6^{1}_{out}$				$32A^{16}$	I/O	IOR, PD
X2D68	$XL6^{2}_{out}$				$32A^{17}$	I/O	IOR, PD
X2D69	$XL6^{3}_{out}$				$32A^{18}$	I/O	IOR, PD
X2D70	$XL6^{4}_{out}$				$32A^{19}$	I/O	IOR, PD
X3D00	$XL7^{2}_{in}$	$1A^{0}$				I/O	IOR, PD
X3D01	$XL7^{1}_{in}$	$1B^{0}$				I/O	IOR, PD
X3D02	$XL4^{0}_{in}$		$4A^{0}$	$8A^{0}$	$16A^{0}$ $32A^{20}$	I/O	IOR, PD
X3D03	$XL4^{0}_{out}$		$4A^{1}$	$8A^{1}$	$16A^{1}$ $32A^{21}$	I/O	IOR, PD
X3D04	$XL4^{1}_{out}$		$4B^{0}$	$8A^{2}$	$16A^{2}$ $32A^{22}$	I/O	IOR, PD
X3D05	$XL4^{2}_{out}$		$4B^{1}$	$8A^{3}$	$16A^{3}$ $32A^{23}$	I/O	IOR, PD
X3D06	$XL4^{3}_{out}$		$4B^{2}$	$8A^{4}$	$16A^{4}$ $32A^{24}$	I/O	IOR, PD
X3D07	$XL4^{4}_{out}$		$4B^{3}$	$8A^{5}$	$16A^{5}$ $32A^{25}$	I/O	IOR, PD
X3D08	$XL7^{4}_{in}$		$4A^{2}$	$8A^{6}$	$16A^{6}$ $32A^{26}$	I/O	IOR, PD
X3D09	$XL7^{3}_{in}$		$4A^{3}$	$8A^{7}$	$16A^{7}$ $32A^{27}$	I/O	IOR, PD
X3D10		$1C^{0}$				I/O	IOT, PD
X3D11		$1D^{0}$				I/O	IOT, PD
X3D12		$1E^{0}$				I/O	IOL, PD
X3D13		$1F^{0}$				I/O	IOL, PD
X3D14			$4C^{0}$	$8B^{0}$	$16A^{8}$ $32A^{28}$	I/O	IOR, PD
X3D15			$4C^{1}$	$8B^{1}$	$16A^{9}$ $32A^{29}$	I/O	IOR, PD
X3D20			$4C^{2}$	$8B^{6}$	$16A^{14}$ $32A^{30}$	I/O	IOR, PD
X3D21			$4C^{3}$	$8B^{7}$	$16A^{15}$ $32A^{31}$	I/O	IOR, PD
X3D23		$1H^{0}$				I/O	IOL, PD
X3D24		$1I^{0}$				I/O	IOR, PD
X3D25		$1J^{0}$				I/O	IOR, PD
X3D26	tx_clk (rgmii)		$4E^{0}$	$8C^{0}$	$16B^{0}$	I/O	IOT, PD
X3D27	tx_ctl (rgmii)		$4E^{1}$	$8C^{1}$	$16B^{1}$	I/O	IOT, PD
X3D28	rx_clk (rgmii)		$4F^{0}$	$8C^{2}$	$16B^{2}$	I/O	IOT, PD
X3D29	rx_ctl (rgmii)		$4F^{1}$	$8C^{3}$	$16B^{3}$	I/O	IOT, PD
X3D30	rx0 (rgmii)		$4F^{2}$	$8C^{4}$	$16B^{4}$	I/O	IOT, PD
X3D31	rx1 (rgmii)		$4F^{3}$	$8C^{5}$	$16B^{5}$	I/O	IOT, PD
X3D32	rx2 (rgmii)		$4E^{2}$	$8C^{6}$	$16B^{6}$	I/O	IOT, PD
X3D33	rx3 (rgmii)		$4E^{3}$	$8C^{7}$	$16B^{7}$	I/O	IOT, PD
X3D40	tx3 (rgmii)			$8D^{4}$	$16B^{12}$	I/O	IOT, PD
X3D41	tx2 (rgmii)			$8D^{5}$	$16B^{13}$	I/O	IOT, PD

(continued)

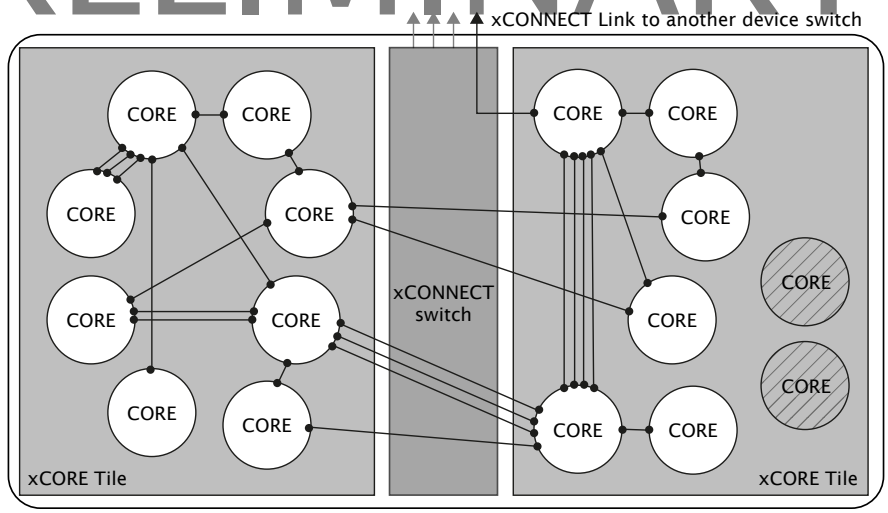


Figure 6: Switch, links and channel ends

and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between xCORE Tiles (up to 250 MBit/s), but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-UEF Link Performance and Design Guide, X2999.

7 PLL

The PLL creates a high-speed clock that is used for the switch, tile, and reference clock. The PLL multiplication value is selected through the two MODE pins, and can be changed by software to speed up the tile or use less power. The MODE pins are set as shown in Figure 7:

Figure 7: PLL multiplier values and MODE pins

Oscillator Frequency	MODE 1	MODE 0	Tile Frequency	PLL Ratio	PLL settings OD	F	R
3.25-10 MHz	0	0	130-400 MHz	40	1	159	0
9-25 MHz	1	1	144-400 MHz	16	1	63	0
25-50 MHz	1	0	167-400 MHz	8	1	31	0
50-100 MHz	0	1	196-400 MHz	4	1	15	0

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified in Figure 16. The OTP User ID field is read from bits [22:31] of the security register on xCORE Tile 0, *see* §9.1 (all zero on unprogrammed devices).

Figure 16: USERCODE return value

Bit31										Usercode Register																				Bit0
OTP User ID										Unused				Silicon Revision																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0				0				0				2				8				0				0						

13 Board Integration

The device has the following power supply pins:

- VDD pins for the xCORE Tile
- VDDIO pins for the I/O lines
- PLL_AVDD pins for the PLL
- OTP_VCC pins for the OTP

Several pins of each type are provided to minimize the effect of inductance within the package, all of which must be connected. The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

The VDD supply must ramp from 0 V to its final value within 10 ms to ensure correct startup.

The VDDIO and OTP_VCC supply must ramp to its final value before VDD reaches 0.4 V.

The PLLVDD supply should be separated from the other noisier supplies on the board. The PLL requires a very clean power supply, and a low pass filter (for example, a 4.7 Ω resistor and multi-layer ceramic capacitor) is recommended on this pin.

The following ground pins are provided:

- PLL_AGND for PLL_AVDD
- GND for all other supplies

All ground pins must be connected directly to the board ground.

The VDD and VDDIO supplies should be decoupled close to the chip by several 100 nF low inductance multi-layer ceramic capacitors between the supplies and GND (for example, 4x100nF 0402 low inductance MLCCs per supply rail). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least 10 uF should be placed on each of these supplies.

RST_N is an active-low asynchronous-assertion global reset signal. Following a reset, the PLL re-establishes lock after which the device boots up according to the boot mode (*see* §8). RST_N and must be asserted low during and after power up for 100 ns.

13.1 USB connections

USB_VBUS should be connected to the VBUS pin of the USB connector. A 2.2 uF capacitor to ground is required on the VBUS pin. A ferrite bead may be used to reduce HF noise.

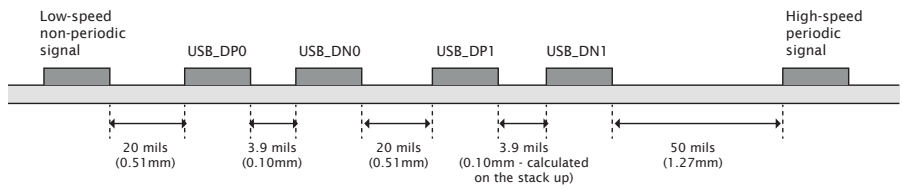
For self-powered systems, a bleeder resistor may be required to stop VBUS from floating when no USB cable is attached.

USB_DP and USB_DN should be connected to the USB connector. USB_ID does not need to be connected.

13.2 USB signal routing and placement

The USB_DP and USB_DN lines are the positive and negative data polarities of a high speed USB signal respectively. Their high-speed differential nature implies that they must be coupled and properly isolated. The board design must ensure that the board traces for USB_DP and USB_DN are tightly matched. In addition, according to the USB 2.0 specification, the USB_DP and USB_DN differential impedance must be 90 Ω.

Figure 17: USB trace separation showing a low speed signal, two differential pairs and a high-speed clock



13.2.1 General routing and placement guidelines

The following guidelines will help to avoid signal quality and EMI problems on high speed USB designs. They relate to a four-layer (Signal, GND, Power, Signal) PCB.

For best results, most of the routing should be done on the top layer (assuming the USB connector and XS2-UEF32A-1024-FB374 are on the top layer) closest to GND. Reference planes should be below the transmission lines in order to maintain control of the trace impedance.

14.9 JTAG Timing

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f(TCK_D)	TCK frequency (debug)			18	MHz	
f(TCK_B)	TCK frequency (boundary scan)			10	MHz	
T(SETUP)	TDO to TCK setup time	5			ns	A
T(HOLD)	TDO to TCK hold time	5			ns	A
T(DELAY)	TCK to output delay			15	ns	B

Figure 27: JTAG timing

A Timing applies to TMS and TDI inputs.

B Timing applies to TDO output from negative edge of TCK.

All JTAG operations are synchronous to TCK.

B.1 RAM base address: 0x00

This register contains the base address of the RAM. It is initialized to 0x00040000.

0x00: RAM base address

Bits	Perm	Init	Description
31:2	RW		Most significant 16 bits of all addresses.
1:0	RO	-	Reserved

B.2 Vector base address: 0x01

Base address of event vectors in each resource. On an interrupt or event, the 16 most significant bits of the destination address are provided by this register; the least significant 16 bits come from the event vector.

0x01: Vector base address

Bits	Perm	Init	Description
31:18	RW		The event and interrupt vectors.
17:0	RO	-	Reserved

B.3 xCORE Tile control: 0x02

Register to control features in the xCORE tile

0x02: xCORE Tile control

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:18	RW	0	RGMII TX data delay value (in PLL output cycle increments)
17:9	RW	0	RGMII TX clock divider value. TX clk rises when counter (clocked by PLL output) reaches this value and falls when counter reaches (value»1). Value programmed into this field should be actual divide value required minus 1
8	RW	0	Enable RGMII interface periph ports
7:6	RO	-	Reserved
5	RW	0	Select the dynamic mode (1) for the clock divider when the clock divider is enabled. In dynamic mode the clock divider is only activated when all active threads are paused. In static mode the clock divider is always enabled.
4	RW	0	Enable the clock divider. This divides the output of the PLL to facilitate one of the low power modes.
3	RO	-	Reserved
2	RW		Select between UTMI (1) and ULPI (0) mode.
1	RW		Enable the ULPI Hardware support module
0	RO	-	Reserved

B.4 xCORE Tile boot status: 0x03

This read-only register describes the boot status of the xCORE tile.

0x03: xCORE Tile boot status

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	RO		Processor number.
15:9	RO	-	Reserved
8	RO		Overwrite BOOT_MODE.
7:6	RO	-	Reserved
5	RO		Indicates if core1 has been powered off
4	RO		Cause the ROM to not poll the OTP for correct read levels
3	RO		Boot ROM boots from RAM
2	RO		Boot ROM boots from JTAG
1:0	RO		The boot PLL mode pin value.

0x9C .. 0x9F: Resources breakpoint control register

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	DRW	0	A bit for each thread in the machine allowing the breakpoint to be enabled individually for each thread.
15:2	RO	-	Reserved
1	DRW	0	When 0 break when condition A is met. When 1 = break when condition B is met.
0	DRW	0	When 1 the instruction breakpoint is enabled.

C Tile Configuration

The xCORE Tile control registers can be accessed using configuration reads and writes (use `write_tile_config_reg(tileref, ...)` and `read_tile_config_reg(tileref, ...)` for reads and writes).

Number	Perm	Description
0x00	CRO	Device identification
0x01	CRO	xCORE Tile description 1
0x02	CRO	xCORE Tile description 2
0x04	CRW	Control PSwitch permissions to debug registers
0x05	CRW	Cause debug interrupts
0x06	CRW	xCORE Tile clock divider
0x07	CRO	Security configuration
0x20 .. 0x27	CRW	Debug scratch
0x40	CRO	PC of logical core 0
0x41	CRO	PC of logical core 1
0x42	CRO	PC of logical core 2
0x43	CRO	PC of logical core 3
0x44	CRO	PC of logical core 4
0x45	CRO	PC of logical core 5
0x46	CRO	PC of logical core 6
0x47	CRO	PC of logical core 7
0x60	CRO	SR of logical core 0
0x61	CRO	SR of logical core 1
0x62	CRO	SR of logical core 2
0x63	CRO	SR of logical core 3
0x64	CRO	SR of logical core 4
0x65	CRO	SR of logical core 5
0x66	CRO	SR of logical core 6
0x67	CRO	SR of logical core 7

Figure 32: Summary

C.1 Device identification: 0x00

This register identifies the xCORE Tile

0x00: Device identification

Bits	Perm	Init	Description
31:24	CRO		Processor ID of this XCore.
23:16	CRO		Number of the node in which this XCore is located.
15:8	CRO		XCore revision.
7:0	CRO		XCore version.

C.2 xCORE Tile description 1: 0x01

This register describes the number of logical cores, synchronisers, locks and channel ends available on this xCORE tile.

0x01: xCORE Tile description 1

Bits	Perm	Init	Description
31:24	CRO		Number of channel ends.
23:16	CRO		Number of the locks.
15:8	CRO		Number of synchronisers.
7:0	RO	-	Reserved

C.3 xCORE Tile description 2: 0x02

This register describes the number of timers and clock blocks available on this xCORE tile.

0x02: xCORE Tile description 2

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:8	CRO		Number of clock blocks.
7:0	CRO		Number of timers.

C.4 Control PSwitch permissions to debug registers: 0x04

This register can be used to control whether the debug registers (marked with permission CRW) are accessible through the tile configuration registers. When this bit is set, write -access to those registers is disabled, preventing debugging of the xCORE tile over the interconnect.

0x07: Security configuration

Bits	Perm	Init	Description
31	CRO		Disables write permission on this register
30:15	RO	-	Reserved
14	CRO		Disable access to XCore's global debug
13	RO	-	Reserved
12	CRO		lock all OTP sectors
11:8	CRO		lock bit for each OTP sector
7	CRO		Enable OTP reduanacy
6	RO	-	Reserved
5	CRO		Override boot mode and read boot image from OTP
4	CRO		Disable JTAG access to the PLL/BOOT configuration registers
3:1	RO	-	Reserved
0	CRO		Disable access to XCore's JTAG debug TAP

C.8 Debug scratch: 0x20 .. 0x27

A set of registers used by the debug ROM to communicate with an external debugger, for example over the switch. This is the same set of registers as the Debug Scratch registers in the processor status.

0x20 .. 0x27: Debug scratch

Bits	Perm	Init	Description
31:0	CRW		Value.

C.9 PC of logical core 0: 0x40

Value of the PC of logical core 0.

0x40: PC of logical core 0

Bits	Perm	Init	Description
31:0	CRO		Value.

C.10 PC of logical core 1: 0x41

Value of the PC of logical core 1.

C.15 PC of logical core 6: 0x46

Value of the PC of logical core 6.

0x46: PC of logical core 6

Bits	Perm	Init	Description
31:0	CRO		Value.

C.16 PC of logical core 7: 0x47

Value of the PC of logical core 7.

0x47: PC of logical core 7

Bits	Perm	Init	Description
31:0	CRO		Value.

C.17 SR of logical core 0: 0x60

Value of the SR of logical core 0

0x60: SR of logical core 0

Bits	Perm	Init	Description
31:0	CRO		Value.

C.18 SR of logical core 1: 0x61

Value of the SR of logical core 1

0x61: SR of logical core 1

Bits	Perm	Init	Description
31:0	CRO		Value.

C.19 SR of logical core 2: 0x62

Value of the SR of logical core 2

D Node Configuration

The digital node control registers can be accessed using configuration reads and writes (use `write_node_config_reg(device, ...)` and `read_node_config_reg(device, ...)` for reads and writes).

Number	Perm	Description
0x00	RO	Device identification
0x01	RO	System switch description
0x04	RW	Switch configuration
0x05	RW	Switch node identifier
0x06	RW	PLL settings
0x07	RW	System switch clock divider
0x08	RW	Reference clock
0x09	R	System JTAG device ID register
0x0A	R	System USERCODE register
0x0C	RW	Directions 0-7
0x0D	RW	Directions 8-15
0x10	RW	Reserved
0x11	RW	Reserved.
0x1F	RO	Debug source
0x20 .. 0x28	RW	Link status, direction, and network
0x40 .. 0x47	RO	PLink status and network
0x80 .. 0x88	RW	Link configuration and initialization
0xA0 .. 0xA7	RW	Static link configuration

Figure 33: Summary

D.1 Device identification: 0x00

This register contains version and revision identifiers and the mode-pins as sampled at boot-time.

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	RO		Sampled values of BootCtl pins on Power On Reset.
15:8	RO		SSwitch revision.
7:0	RO		SSwitch version.

0x00: Device identification

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:24	RO		Identify the SRC_TARGET type 0 - SLink, 1 - PLink, 2 - SSCTL, 3 - Undefine.
23:16	RO		When the link is in use, this is the destination link number to which all packets are sent.
15:6	RO	-	Reserved
5:4	RW	0	Determines the network to which this link belongs, reset as 0.
3	RO	-	Reserved
2	RO		1 when the current packet is considered junk and will be thrown away.
1	RO		1 when the dest side of the link is in use.
0	RO		1 when the source side of the link is in use.

0x40 .. 0x47: PLink status and network

D.17 Link configuration and initialization: 0x80 .. 0x88

These registers contain configuration and debugging information specific to external links. The link speed and width can be set, the link can be initialized, and the link status can be monitored. The registers control links 0..7.

Bits	Perm	Init	Description
31	RW		Write to this bit with '1' will enable the XLink, writing '0' will disable it. This bit controls the muxing of ports with overlapping xlinks.
30	RW	0	0: operate in 2 wire mode; 1: operate in 5 wire mode
29:28	RO	-	Reserved
27	RO		Rx buffer overflow or illegal token encoding received.
26	RO	0	This end of the xlink has issued credit to allow the remote end to transmit
25	RO	0	This end of the xlink has credit to allow it to transmit.
24	WO		Clear this end of the xlink's credit and issue a HELLO token.
23	WO		Reset the receiver. The next symbol that is detected will be the first symbol in a token.
22	RO	-	Reserved
21:11	RW	0	Specify min. number of idle system clocks between two continuous symbols witin a transmit token -1.
10:0	RW	0	Specify min. number of idle system clocks between two continuous transmit tokens -1.

0x80 .. 0x88: Link configuration and initialization

E USB Node Configuration

The USB node control registers can be accessed using configuration reads and writes (use `write_node_config_reg(device, ...)` and `read_node_config_reg(device, ...)` for reads and writes).

Figure 34: Summary

Number	Perm	Description
0x00	RO	Device identification register
0x04	RW	Node configuration register
0x05	RW	Node identifier
0x51	RW	System clock frequency
0x80	RW	Link Control and Status

E.1 Device identification register: 0x00

This register contains version information, and information on power-on behavior.

0x00: Device identification register

Bits	Perm	Init	Description
31:24	RO	0x0F	Chip identifier
23:16	RO	-	Reserved
15:8	RO	0x02	Revision number of the USB block
7:0	RO	0x00	Version number of the USB block

E.2 Node configuration register: 0x04

This register is used to set the communication model to use (1 or 3 byte headers), and to prevent any further updates.

0x04: Node configuration register

Bits	Perm	Init	Description
31	RW	0	Set to 1 to disable further updates to the node configuration and link control and status registers.
30:1	RO	-	Reserved
0	RW	0	Header mode. 0: 3-byte headers; 1: 1-byte headers.

E.3 Node identifier: 0x05

0x05: Node identifier

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RW	0	16-bit node identifier. This does not need to be set, and is present for compatibility with XS1-switches.

E.4 System clock frequency: 0x51

0x51: System clock frequency

Bits	Perm	Init	Description
31:7	RO	-	Reserved
6:0	RW	25	Oscillator clock frequency in MHz rounded up to the nearest integer value. Only values between 5 and 100 MHz are valid - writes outside this range are ignored and will be NACKed. This field must be set on start up of the device and any time that the input oscillator clock frequency is changed. It must contain the system clock frequency in MHz rounded up to the nearest integer value.

E.5 Link Control and Status: 0x80

0x80: Link Control and Status

Bits	Perm	Init	Description
31:28	RO	-	Reserved
27	RO		Rx buffer overflow or illegal token encoding received.
26	RO	0	This end of the xlink has issued credit to allow the remote end to transmit
25	RO	0	This end of the xlink has credit to allow it to transmit.
24	WO		Clear this end of the xlink's credit and issue a HELLO token.
23	WO		Reset the receiver. The next symbol that is detected will be the first symbol in a token.
22	RO	-	Reserved
21:11	RW	1	Specify min. number of idle system clocks between two continuous symbols witin a transmit token -1.
10:0	RW	1	Specify min. number of idle system clocks between two continuous transmit tokens -1.

0x2C: UIFM PID

Bits	Perm	Init	Description
31:4	RO	-	Reserved
3:0	RO	0	Value of the last received PID.

F.13 UIFM Endpoint: 0x30

The last endpoint seen

0x30: UIFM Endpoint

Bits	Perm	Init	Description
31:5	RO	-	Reserved
4	RO	0	1 if endpoint contains a valid value.
3:0	RO	0	A copy of the last received endpoint.

F.14 UIFM Endpoint match: 0x34

This register can be used to mark UIFM endpoints as special.

0x34: UIFM Endpoint match

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RW	0	This register contains a bit for each endpoint. If its bit is set, the endpoint will be supplied on the RX port when ORed with 0x10.

F.15 OTG Flags mask: 0x38

0x38: OTG Flags mask

Bits	Perm	Init	Description
31:0	RW	0	Data

F.16 UIFM power signalling: 0x3C

0x3C: UIFM power signalling

Bits	Perm	Init	Description
31:9	RO	-	Reserved
8	RW	0	Valid
7:0	RW	0	Data

- ☐ Pins MODE0 and MODE1 are set to the correct value for the chosen oscillator frequency. The MODE settings are shown in the Oscillator section, Section 7. If you have a choice between two values, choose the value with the highest multiplier ratio since that will boot faster.

I.5 RGMII interface

This section can be skipped if you do not have any device connected to the RGMII interface.

- ☐ RX_CLK will be low when the xCORE comes out of reset (see Section 11).
- ☐ VDDIOT has a 2.5V supply.
- ☐ RGMII signals are connected to the appropriate RGMII pins of the xCORE device.

I.6 Boot

- ☐ X0D01 has a 1K pull-up to VDDIOL (Section 8).
- ☐ The device is kept in reset for at least 1 ms after VDDIOL has reached its minimum level (Section 8).

I.7 JTAG, XScope, and debugging

- ☐ You have decided as to whether you need an XSYS header or not (Section H)
- ☐ If you have not included an XSYS header, you have devised a method to program the SPI-flash or OTP (Section H).

I.8 GPIO

- ☐ You have not mapped both inputs and outputs to the same multi-bit port.
- ☐ Pins X0D04, X0D05, X0D06, and X0D07 are output only and are, after reset, pulled low or not connected (Section 8)

I.9 Multi device designs

Skip this section if your design only includes a single XMOS device.

- ☐ One device is connected to a SPI flash for booting.