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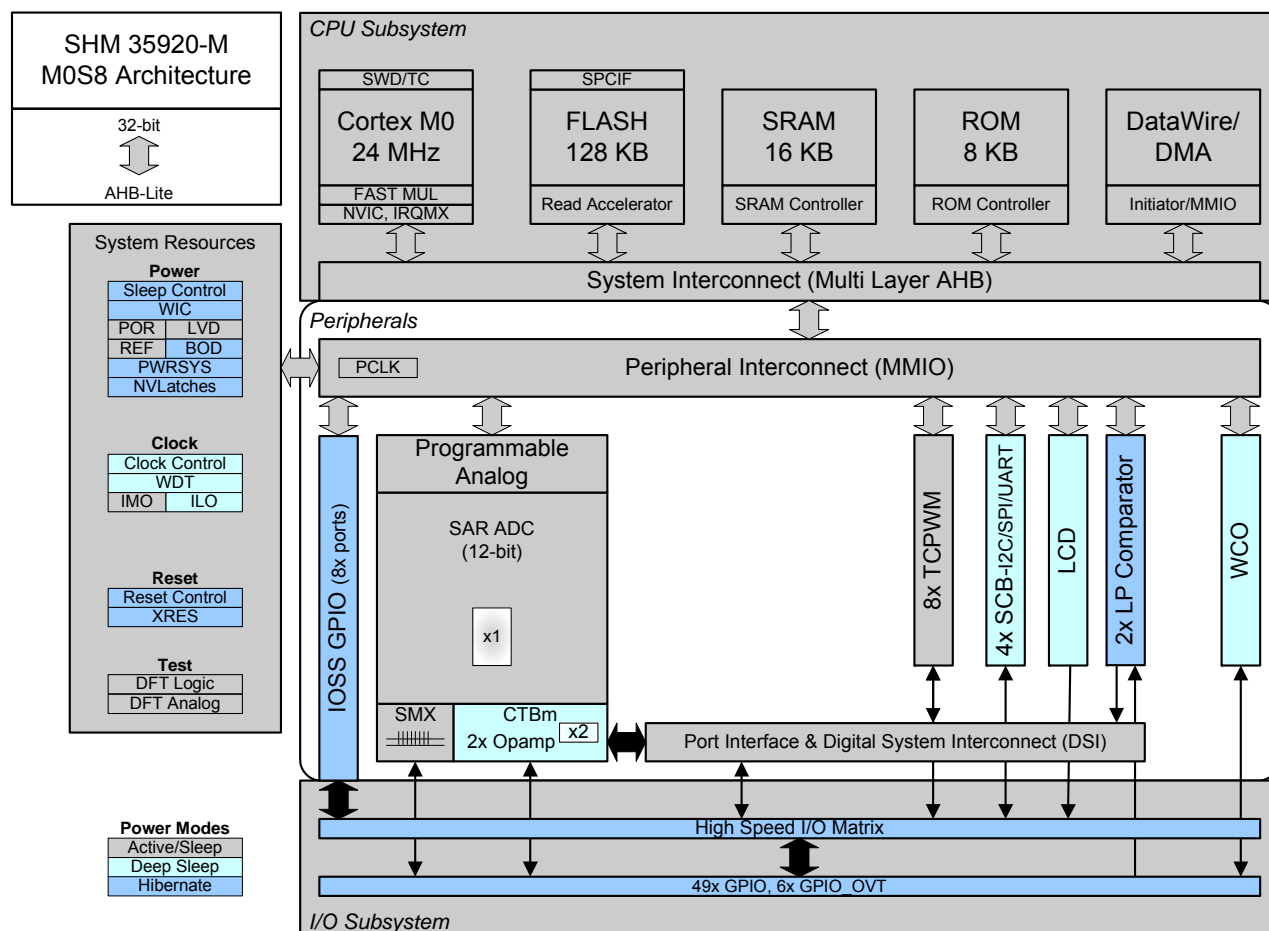
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyshm35925i-m068ltit

SHM 35920-M Block Diagram



The SHM35920-M devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for SHM35920-M devices. The SWD interface is fully compatible with industry-standard third-party tools. The SHM35920-M family provides a level of security not possible with multi-chip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and because

it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, SHM35920-M with device security enabled may not be returned for failure analysis. This is a trade-off the SHM35920-M allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in SHM35920-M is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for SHM35920-M has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The SHM35920-M has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

DMA

ADMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

System Resources

Power System

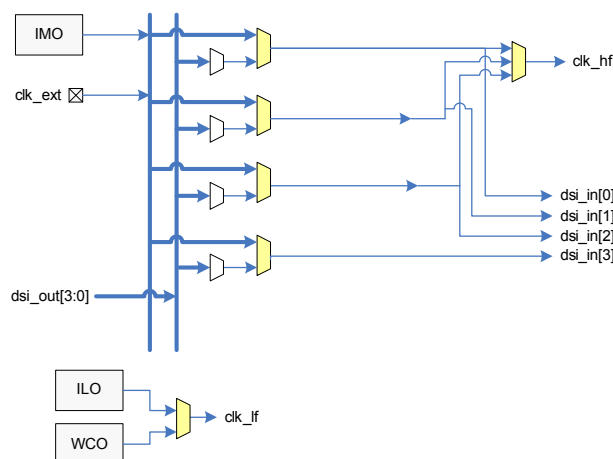
The power system is described in detail in the section [Power on page 11](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). SHM35920-M operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. SHM35920-M provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The SHM35920-M clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The SHM35920-M clock system consists of a Watch Crystal Oscillator (WCO) running at 32 kHz, the IMO (3 to 48 MHz) and the ILO (32-kHz nominal) internal oscillators, and provision for an external clock.

Figure 1. SHM35920-M MCU Clocking Architecture



The clk_hf signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are a total of 16 clock dividers for the SHM35920-M devices, each with 16-bit divide capability. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in SHM35920-M. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile memory. Trimming can also be done on the fly to allow in-field calibration. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is $\pm 2\%$.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Crystal Oscillator

The SHM35920-M clock subsystem also includes a low-frequency crystal oscillator (32-kHz WCO) that is available during the Deep Sleep mode and can be used for Real-Time Clock (RTC) and Watchdog Timer applications.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the low-frequency clock; this allows watchdog operation during Deep Sleep and generates a watchdog reset or an interrupt if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Reset

SHM35920-M can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

Voltage Reference

The SHM35920-M reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to add an external bypass capacitor to the internal reference using a GPIO pin or to use an external reference for the SAR.

Analog Blocks

12-bit SAR ADC

The 12-bit SAR ADC can operate at a maximum sample rate of 806 ksp/s.

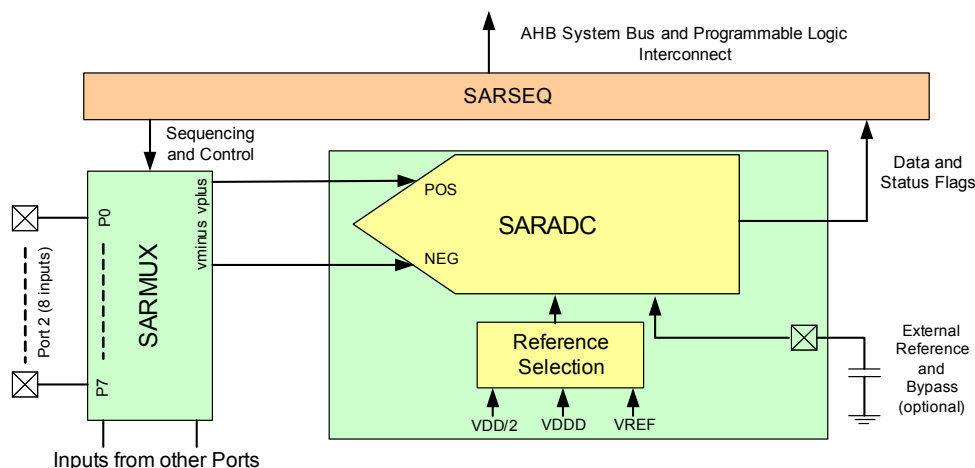
The block functionality is augmented for the user by adding a reference buffer to it (trimmable to $\pm 1\%$) and by providing the choice of three internal voltage references: V_{DD} , $V_{DD}/2$, and V_{REF} (nominally 1.024 V) as well as an external reference

through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. The system performance will be 65 dB for true 12-bit precision if appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer (expandable to 16 inputs). The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps, whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. In addition, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock. The SAR operating range is 1.71 to 5.5 V.

Figure 2. SAR ADC System Diagram



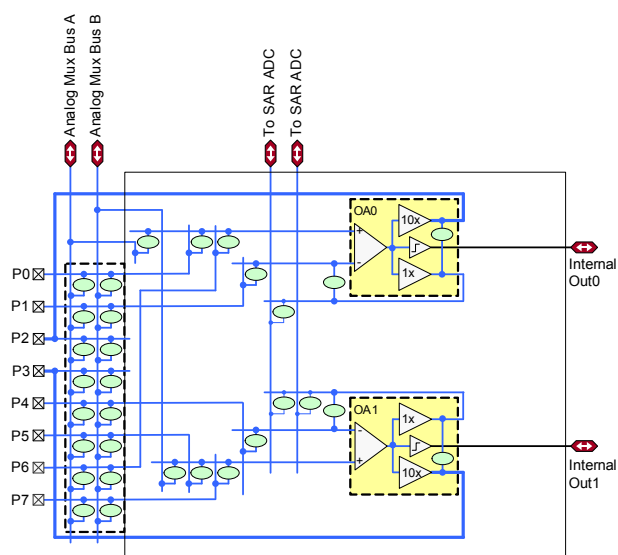
Analog Multiplex Bus

The SHM35920-M consists of two concentric analog buses (Analog Mux Bus A and Analog Mux Bus B) that circumnavigate the periphery of the chip. These buses can transport analog signals from any pin to various analog blocks (including the opamps) allowing, for example, the ADC to monitor any pin on the chip. These buses are independent and can also be split into three independent sections. This allows one section to be used for general analog signal processing, and another for general-purpose digital peripherals and GPIO.

Four Opamps

The SHM35920-M devices have four opamps with comparator modes, which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering. The opamps can operate in the Deep Sleep mode at very low power levels. The following diagram shows one of two identical opamp pairs of the opamp subsystem.

Figure 3. Identical Opamp Pairs in Opamp Subsystem



The ovals in Figure 3 represent analog switches, which may be controlled via user firmware, the SAR sequencer, or user-defined programmable logic. The opamps (OA0 and OA1) are configurable via these switches to perform all standard opamp functions with appropriate feedback components.

The opamps (OA0 and OA1) are programmable and reconfigurable to provide standard opamp functionality via switchable feedback components, unity gain functionality for driving pins directly, or for internal use (such as buffering SAR ADC inputs as indicated in the diagram), or as true comparators.

The opamp inputs provide highly flexible connectivity and can connect directly to dedicated pins or, via the analog mux buses, to any pin on the chip. Analog switch connectivity is controllable by user firmware.

The opamps operate in Deep Sleep mode at very low currents allowing analog circuits to remain operational during Deep Sleep.

Temperature Sensor

All SHM35920-M devices have one on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress-supplied software that includes calibration and linearization.

Low-power Comparators

The SHM35920-M devices have a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid meta-stability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block uses a 16-bit counter with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals, which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. The SHM35920-M has eight TCPWM blocks.

Serial Communication Blocks (SCB)

The SHM35920-M has four SCBs, which can each implement an I²C, UART, or SPI interface.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The I²C peripheral is also capable of supporting SMBus or PMBus interfaces. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I²C peripheral is compatible with the I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and also supports an EzSPI mode in which data interchange is reduced to reading and writing an array in memory.

GPIO

The SHM35920-M has 55 GPIOs in the 68-pin QFN package. The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (8 for SHM35920-M).

The Pins of Port 6 (up to 6 depending on the package) are overvoltage tolerant (V_{IN} can exceed V_{DD}). The overvoltage cells will not sink more than 10 μA when their inputs exceed V_{DDIO} in compliance with I²C specifications.

Special Function Peripherals

LCD Segment Drive

SHM35920-M has an LCD controller, which can drive up to four commons and up to 51 segments. Any pin can be either a common or a segment pin. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

Power

The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

The SHM35920-M family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

Unregulated External Supply

In this mode, the SHM35920-M is powered by an External Power Supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5V and works down to 1.8 V. In this mode, the internal regulator of the SHM35920-M supplies the internal logic and the VCCD output of the SHM35920-M must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6 μF ; X5R ceramic or better).

The grounds, VSSA and VSS, must be shorted together. Bypass capacitors must be used from VDDD and VDPA to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 μF range in parallel with a smaller capacitor (0.1 μF , for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power Supply	Bypass Capacitors
VDDD–VSS and VDDIO–VSS	0.1 μF ceramic at each pin plus bulk capacitor 1 to 10 μF .
VDPA–VSSA	0.1 μF ceramic at pin. Additional 1 μF to 10 μF bulk capacitor
VCCD–VSS	1 μF ceramic capacitor at the VCCD pin
VREF–VSSA (optional)	The internal bandgap may be bypassed with a 1 μF to 10 μF capacitor for better ADC performance.

Regulated External Supply

In this mode, the SHM35920-M is powered by an external power supply that must be within the range of 1.71 to 1.89 V ($1.8 \pm 5\%$); note that this range needs to include power supply ripple. VCCD and VDDD pins are shorted together and bypassed. The internal regulator is disabled in firmware.

Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings^[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID1	V _{DD_ABS}	Analog or digital supply relative to V _{SS} (V _{SSD} = V _{SSA})	−0.5	−	6	V	Absolute maximum
SID2	V _{CCD_ABS}	Direct digital core voltage input relative to V _{SSD}	−0.5	−	1.95	V	Absolute maximum
SID3	V _{GPIO_ABS}	GPIO voltage; V _{DDD} or V _{DDA}	−0.5	−	V _{DD} +0.5	V	Absolute maximum
SID4	I _{GPIO_ABS}	Current per GPIO	−25	−	25	mA	Absolute maximum
SID5	I _{G-PIO_injection}	GPIO injection current per pin	−0.5	−	0.5	mA	Absolute maximum
BID44	ESD_HBM	Electrostatic discharge human body model	2200	−	−	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	−	−	V	
BID46	LU	Pin current for latch-up	−140	−	140	mA	

Device Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$ and $T_J \leq 125\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID53	V _{DD}	Power Supply Input Voltage (V _{DDA} = V _{DDD} = V _{DD})	1.8	−	5.5	V	With regulator enabled
SID255	V _{DDD}	Power Supply Input Voltage unregulated	1.71	1.8	1.89	V	Internally unregulated Supply
SID54	V _{CCD}	Output voltage (for core logic)	−	1.8	−	V	
SID55	C _{EFC}	External Regulator voltage bypass	1	1.3	1.6	μF	X5R ceramic or better
SID56	C _{EXC}	Power supply decoupling capacitor	−	1	−	μF	X5R ceramic or better
Active Mode, V_{DD} = 1.71 V to 5.5 V, −40 °C to +105 °C							
SID6	I _{DD1}	Execute from Flash; CPU at 6 MHz	−	2.2	2.8	mA	
SID7	I _{DD2}	Execute from Flash; CPU at 12 MHz	−	3.7	4.2	mA	
SID8	I _{DD3}	Execute from Flash; CPU at 24 MHz	−	6.7	7.2	mA	
Sleep Mode, −40 °C to +105 °C							
SID21	I _{DD16}	I ² C wakeup, WDT, and Comparators on. Regulator Off.	−	1.75	2.1	mA	V _{DD} = 1.71 to 1.89, 6 MHz
SID22	I _{DD17}	I ² C wakeup, WDT, and Comparators on.	−	1.7	2.1	mA	V _{DD} = 1.8 to 5.5, 6 MHz
SID23	I _{DD18}	I ² C wakeup, WDT, and Comparators on. Regulator Off.	−	2.35	2.8	mA	V _{DD} = 1.71 to 1.89, 12 MHz
SID24	I _{DD19}	I ² C wakeup, WDT, and Comparators on.	−	2.25	2.8	mA	V _{DD} = 1.8 to 5.5, 12 MHz

Note

- Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 2. DC Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
Deep Sleep Mode, -40 °C to + 60 °C							
SID30	I _{DD25}	I ² C wakeup and WDT on. Regulator Off.	–	1.55	20	μA	V _{DD} = 1.71 to 1.89
SID31	I _{DD26}	I ² C wakeup and WDT on.	–	1.35	15	μA	V _{DD} = 1.8 to 3.6
SID32	I _{DD27}	I ² C wakeup and WDT on.	–	1.5	15	μA	V _{DD} = 3.6 to 5.5
Deep Sleep Mode, +85 °C							
SID33	I _{DD28}	I ² C wakeup and WDT on. Regulator Off.	–	–	60	μA	V _{DD} = 1.71 to 1.89
SID34	I _{DD29}	I ² C wakeup and WDT on.	–	–	45	μA	V _{DD} = 1.8 to 3.6
SID35	I _{DD30}	I ² C wakeup and WDT on.	–	–	30	μA	V _{DD} = 3.6 to 5.5
Deep Sleep Mode, +105 °C							
SID33Q	I _{DD28Q}	I ² C wakeup and WDT on. Regulator Off.	–	–	135	μA	V _{DD} = 1.71 to 1.89
SID34Q	I _{DD29Q}	I ² C wakeup and WDT on.	–	–	180	μA	V _{DD} = 1.8 to 3.6
SID35Q	I _{DD30Q}	I ² C wakeup and WDT on.	–	–	140	μA	V _{DD} = 3.6 to 5.5
Hibernate Mode, -40 °C to + 60 °C							
SID39	I _{DD34}	Regulator Off.	–	150	3000	nA	V _{DD} = 1.71 to 1.89
SID40	I _{DD35}		–	150	1000	nA	V _{DD} = 1.8 to 3.6
SID41	I _{DD36}		–	150	1100	nA	V _{DD} = 3.6 to 5.5
Hibernate Mode, +85 °C							
SID42	I _{DD37}	Regulator Off.	–	–	4500	nA	V _{DD} = 1.71 to 1.89
SID43	I _{DD38}		–	–	3500	nA	V _{DD} = 1.8 to 3.6
SID44	I _{DD39}		–	–	3500	nA	V _{DD} = 3.6 to 5.5
Hibernate Mode, +105 °C							
SID42Q	I _{DD37Q}	Regulator Off.	–	–	19.4	μA	V _{DD} = 1.71 to 1.89
SID43Q	I _{DD38Q}		–	–	17	μA	V _{DD} = 1.8 to 3.6
SID44Q	I _{DD39Q}		–	–	16	μA	V _{DD} = 3.6 to 5.5
Stop Mode, +85 °C							
SID304	I _{DD43A}	Stop Mode current; V _{DD} = 3.6 V	–	35	85	nA	T = -40 °C to +60 °C
SID304A	I _{DD43B}	Stop Mode current; V _{DD} = 3.6 V	–	–	1450	nA	T = +85 °C
Stop Mode, +105 °C							
SID304Q	I _{DD43AQ}	Stop Mode current; V _{DD} = 3.6 V	–	–	5645	nA	
XRES current							
SID307	I _{DD_XR}	Supply current while XRES asserted	–	2	5	mA	

Table 4. GPIO DC Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	–	–	4	nA	Guaranteed by characterization
SID66	C_{IN}	Input capacitance	–	–	7	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTTL	25	40	–	mV	$V_{DD} \geq 2.7\text{ V}$
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	–	–	mV	
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

Table 5. GPIO AC Specifications

 (Guaranteed by Characterization)^[3]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DD} , Load = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DD} , Load = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3 V V_{DD} , Load = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3 V V_{DD} , Load = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout; 3.3 V $\leq V_{DD} \leq 5.5\text{ V}$. Fast strong mode.	–	–	24	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; 1.7 V $\leq V_{DD} \leq 3.3\text{ V}$. Fast strong mode.	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; 3.3 V $\leq V_{DD} \leq 5.5\text{ V}$. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout; 1.7 V $\leq V_{DD} \leq 3.3\text{ V}$. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V $\leq V_{DD} \leq 5.5\text{ V}$	–	–	48	MHz	90/10% V_{IO}

Note

- Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	μ s	Guaranteed by characterization

Analog Peripherals

Opamp

Table 8. Opamp Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I_{DD}	Opamp block current. No load.	–	–	–	–	
SID269	I_{DD_HI}	Power = high	–	1100	1850	μA	
SID270	I_{DD_MED}	Power = medium	–	550	950	μA	
SID271	I_{DD_LOW}	Power = low	–	150	350	μA	
	GBW	Load = 20 pF, 0.1 mA. $V_{DDA} = 2.7 V$	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	I_{OUT_MAX}	$V_{DDA} \geq 2.7 V$, 500 mV from rail	–	–	–	–	
SID275	$I_{OUT_MAX_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT_MAX_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT_MAX_LO}$	Power = low	–	5	–	mA	
	I_{OUT}	$V_{DDA} = 1.71 V$, 500 mV from rail	–	–	–	–	
SID278	$I_{OUT_MAX_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT_MAX_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT_MAX_LO}$	Power = low	–	2	–	mA	
SID281	V_{IN}	Input voltage range	–0.05	–	$V_{DDA} - 0.2$	V	Charge-pump on, $V_{DDA} \geq 2.7 V$
SID282	V_{CM}	Input common mode voltage	–0.05	–	$V_{DDA} - 0.2$	V	Charge-pump on, $V_{DDA} \geq 2.7 V$
	V_{OUT}	$V_{DDA} \geq 2.7 V$	–	–	–	–	
SID283	V_{OUT_1}	Power = high, $I_{load}=10 mA$	0.5	–	$V_{DDA} - 0.5$	V	
SID284	V_{OUT_2}	Power = high, $I_{load}=1 mA$	0.2	–	$V_{DDA} - 0.2$	V	
SID285	V_{OUT_3}	Power = medium, $I_{load}=1 mA$	0.2	–	$V_{DDA} - 0.2$	V	
SID286	V_{OUT_4}	Power = low, $I_{load}=0.1 mA$	0.2	–	$V_{DDA} - 0.2$	V	
SID288	V_{OS_TR}	Offset voltage, trimmed	1	± 0.5	1	mV	High mode
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	± 1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	± 2	–	mV	Low mode
SID290	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–10	± 3	10	$\mu V/^{\circ}C$	High mode. $T_A \leq 85^{\circ}C$.
SID290Q	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	15	± 3	15	$\mu V/^{\circ}C$	High mode. $T_A \leq 105^{\circ}C$
SID290A	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–	± 10	–	$\mu V/^{\circ}C$	Medium mode
SID290B	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–	± 10	–	$\mu V/^{\circ}C$	Low mode
SID291	CMRR	DC Common mode rejection ratio. High-power mode. Common Mode voltage range from 0.5 V to $V_{DDA} - 0.5 V$.	60	70	–	dB	$V_{DD} = 3.6 V$
SID292	PSRR	At 1 kHz, 100-mV ripple	70	85	–	dB	$V_{DD} = 3.6 V$
	Noise		–	–	–	–	

Table 8. Opamp Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID293	V_{N1}	Input referred, 1 Hz - 1GHz, power = high	–	94	–	μVrms	
SID294	V_{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	
SID295	V_{N3}	Input referred, 10kHz, power = high	–	28	–	nV/rtHz	
SID296	V_{N4}	Input referred, 100kHz, power = high	–	15	–	nV/rtHz	
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7\text{ V}$	6	–	–	V/ μs	
SID299	T_op_wake	From disable to enable, no external RC dominating	–	25	–	μs	
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	Comp_mode	Comparator mode; 50 mV drive, Trise = Tfall (approx.)	–	–	–		
SID300	T _{PD1}	Response time; power = high	–	150	–	ns	
SID301	T _{PD2}	Response time; power = medium	–	400	–	ns	
SID302	T _{PD3}	Response time; power = low	–	2000	–	ns	
SID303	Vhyst_op	Hysteresis	–	10	–	mV	
Deep Sleep Mode		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep mode. $V_{DDA} \geq 2.7\text{ V}$.
SID_DS_1	IDD_HI_M1	Mode 1, High current	–	1400	–	μA	25 °C
SID_DS_2	IDD_MED_M1	Mode 1, Medium current	–	700	–	μA	25 °C
SID_DS_3	IDD_LOW_M1	Mode 1, Low current	–	200	–	μA	25 °C
SID_DS_4	IDD_HI_M2	Mode 2, High current	–	120	–	μA	25 °C
SID_DS_5	IDD_MED_M2	Mode 2, Medium current	–	60	–	μA	25 °C
SID_DS_6	IDD_LOW_M2	Mode 2, Low current	–	15	–	μA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25 °C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25 °C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25 °C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} -1.5 V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} -1.5 V
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA} -1.5 V
SID_DS_13	VOS_HI_M1	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA} -1.5 V
SID_DS_14	VOS_MED_M1	Mode 1, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA} -1.5 V
SID_DS_15	VOS_LOW_M1	Mode 1, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA} -1.5 V
SID_DS_16	VOS_HI_M2	Mode 2, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA} -1.5 V
SID_DS_17	VOS_MED_M2	Mode 2, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA} -1.5 V

Table 8. Opamp Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_18	VOS_LOW_M2	Mode 2, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to $V_{DDA}-1.5$ V
SID_DS_19	IOUT_HI_M1	Mode 1, High current	–	10	–	mA	Output is 0.5 V to $V_{DDA}-0.5$ V
SID_DS_20	IOUT_MED_M1	Mode 1, Medium current	–	10	–	mA	Output is 0.5 V to $V_{DDA}-0.5$ V
SID_DS_21	IOUT_LOW_M1	Mode 1, Low current	–	4	–	mA	Output is 0.5 V to $V_{DDA}-0.5$ V
SID_DS_22	IOUT_HI_M2	Mode 2, High current	–	1	–	mA	Output is 0.5 V to $V_{DDA}-0.5$ V
SID_DS_23	IOUT_MED_M2	Mode 2, Medium current	–	1	–	mA	Output is 0.5 V to $V_{DDA}-0.5$ V
SID_DS_24	IOUT_LOW_M2	Mode 2, Low current	–	0.5	–	mA	Output is 0.5 V to $V_{DDA}-0.5$ V

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID85	$V_{\text{OFFSET}2}$	Input offset voltage, Common Mode voltage range from 0 to $V_{DD}-1$	–	–	± 4	mV	
SID85A	$V_{\text{OFFSET}3}$	Input offset voltage. Ultra low-power mode ($V_{DD} \geq 2.2$ V for Temp < 0 °C, $V_{DD} \geq 1.8$ V for Temp > 0 °C).	–	± 12	–	mV	
SID86	V_{HYST}	Hysteresis when enabled, Common Mode voltage range from 0 to $V_{DD}-1$.	–	10	35	mV	Guaranteed by characterization
SID87	$V_{\text{ICM}1}$	Input common mode voltage in normal mode	0	–	$V_{DD}-0.1$	V	Modes 1 and 2.
SID247	$V_{\text{ICM}2}$	Input common mode voltage in low power mode	0	–	V_{DD}	V	
SID247A	$V_{\text{ICM}3}$	Input common mode voltage in ultra low power mode ($V_{DD} \geq 2.2$ V for Temp < 0 °C, $V_{DD} \geq 1.8$ V for Temp > 0 °C)	0	–	$V_{DD}-1.15$	V	
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	$V_{DD} \geq 2.7$ V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	$V_{DD} < 2.7$ V. Guaranteed by characterization
SID89	$I_{\text{CMP}1}$	Block current, normal mode	–	–	400	μ A	Guaranteed by characterization
SID248	$I_{\text{CMP}2}$	Block current, low power mode	–	–	100	μ A	Guaranteed by characterization
SID259	$I_{\text{CMP}3}$	Block current, ultra low power mode ($V_{DD} \geq 2.2$ V for Temp < 0 °C, $V_{DD} \geq 1.8$ V for Temp > 0 °C)	–	6	28	μ A	Guaranteed by characterization
SID90	Z_{CMP}	DC input impedance of comparator	35	–	–	M Ω	Guaranteed by characterization

Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T _{RESP1}	Response time, normal mode	–	–	110	ns	50-mV overdrive
SID258	T _{RESP2}	Response time, low power mode	–	–	200	ns	50-mV overdrive
SID92	T _{RESP3}	Response time, ultra low power mode (V _{DDD} ≥ 2.2 V for Temp < 0 °C, V _{DDD} ≥ 1.8 V for Temp > 0 °C)	–	–	15	µs	200-mV overdrive

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	T _{SENSACC}	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	16		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	8		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V _{REF} .
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V _{SS}	–	V _{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V _{SS}	–	V _{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID106	A_PSR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	806	ksps	

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization) (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	500	ksps	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	ksps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	66	–	–	dB	$F_{IN} = 10 \text{ kHz}$
SID111	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DD} = 1.71 \text{ to } 5.5$, 806 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID111A	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DDD} = 1.71 \text{ to } 3.6$, 806 Ksps, $V_{ref} = 1.71 \text{ to } V_{DDD}$.
SID111B	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	$V_{DDD} = 1.71 \text{ to } 5.5$, 500 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID112	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71 \text{ to } 5.5$, 806 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID112A	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71 \text{ to } 3.6$, 806 Ksps, $V_{ref} = 1.71 \text{ to } V_{DDD}$.
SID112B	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	$V_{DDD} = 1.71 \text{ to } 5.5$, 500 Ksps, $V_{ref} = 1 \text{ to } 5.5$.
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	$F_{IN} = 10 \text{ kHz}$.

CSD

Table 14. IDAC Specification

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
CSD Specification							
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID314	IDAC1_CRT1	Output current of Idac1 (8-bits) in High range	–	612	–	μA	
SID314A	IDAC1_CRT2	Output current of Idac1(8-bits) in Low range	–	306	–	μA	
SID315	IDAC2_CRT1	Output current of Idac2 (7-bits) in High range	–	304.8	–	μA	
SID315A	IDAC2_CRT2	Output current of Idac2 (7-bits) in Low range	–	152.4	–	μA	

LCD Direct Drive

Table 18. LCD Direct Drive DC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I _{LCDLOW}	Operating current in low power mode	–	5	–	μA	16 × 4 small segment disp. at 50 Hz
SID155	C _{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	Guaranteed by Design
SID156	LCD _{OFFSET}	Long-term segment offset	–	20	–	mV	
SID157	I _{LCDOP1}	PWM Mode current. 5-V bias. 24-MHz IMO	–	0.6	–	mA	32 × 4 segments. 50 Hz, 25 °C
SID158	I _{LCDOP2}	PWM Mode current. 3.3-V bias. 24-MHz IMO.	–	0.5	–	mA	32 × 4 segments. 50 Hz, 25 °C

Table 19. LCD Direct Drive AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F _{LCD}	LCD frame rate	10	50	150	Hz	

Table 20. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I _{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	μA	
SID161	I _{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	μA	

Table 21. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F _{UART}	Bit rate	–	–	1	Mbps	

SPI Specifications

Table 22. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	I _{SPI1}	Block current consumption at 1 Mb/s/sec	–	–	360	μA	
SID164	I _{SPI2}	Block current consumption at 4 Mb/s/sec	–	–	560	μA	
SID165	I _{SPI3}	Block current consumption at 8 Mb/s/sec	–	–	600	μA	

Table 23. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F _{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	

SWD Interface

Table 32. SWD Interface Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID214	F_SWCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCLK \leq 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	$T = 1/f_{\text{SWDCLK}}$	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	$T = 1/f_{\text{SWDCLK}}$	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	$T = 1/f_{\text{SWDCLK}}$	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	$T = 1/f_{\text{SWDCLK}}$	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 33. IMO DC Specifications

(Guaranteed by Design)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I _{IMO1}	IMO operating current at 48 MHz	–	–	1000	μA	
SID219	I _{IMO2}	IMO operating current at 24 MHz	–	–	325	μA	
SID220	I _{IMO3}	IMO operating current at 12 MHz	–	–	225	μA	
SID221	I _{IMO4}	IMO operating current at 6 MHz	–	–	180	μA	
SID222	I _{IMO5}	IMO operating current at 3 MHz	–	–	150	μA	

Table 34. IMO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F _{IMOTOL1}	Frequency variation from 3 to 48 MHz	–	–	±2	%	±3% if T _A > 85 °C and IMO frequency < 24 MHz
SID226	T _{STARTIMO}	IMO startup time	–	–	12	μs	
SID227	T _{JITRMSIMO1}	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	T _{JITRMSIMO2}	RMS Jitter at 24 MHz	–	145	–	ps	
SID229	T _{JITRMSIMO3}	RMS Jitter at 48 MHz	–	139	–	ps	

Internal Low-Speed Oscillator

Table 35. ILO DC Specifications

(Guaranteed by Design)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I _{ILO1}	ILO operating current at 32 kHz	–	0.3	1.05	μA	Guaranteed by Characterization
SID233	I _{ILOLEAK}	ILO leakage current	–	2	15	nA	Guaranteed by Design

Table 36. ILO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	T _{STARTILO1}	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	T _{ILODUTY}	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	F _{ILOTRIM1}	32 kHz trimmed frequency	15	32	50	kHz	Max ILO frequency is 70 kHz if T _A > 85 °C

Table 37. External Clock Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at V _{DD/2}	45	–	55	%	Guaranteed by characterization

Table 38. Watch Crystal Oscillator (WCO) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
IMO WCO-PLL calibrated mode							
SID330	IMO _{WCO1}	Frequency variation with IMO set to 3 MHz	–0.6	–	0.6	%	Does not include WCO tolerance
SID331	IMO _{WCO2}	Frequency variation with IMO set to 5 MHz	–0.4	–	0.4	%	Does not include WCO tolerance
SID332	IMO _{WCO3}	Frequency variation with IMO set to 7 MHz or 9 MHz	–0.3	–	0.3	%	Does not include WCO tolerance
SID333	IMO _{WCO4}	All other IMO frequency settings	–0.2	–	0.2	%	Does not include WCO tolerance
WCO Specifications							
SID398	F _{WCO}	Crystal frequency	–	32.768		kHz	
SID399	F _{TOL}	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal.
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive level	–	–	1	μW	
SID402	T _{START}	Startup time	–	–	500	ms	
SID403	C _L	Crystal load capacitance	6	–	12.5	pF	
SID404	C ₀	Crystal shunt capacitance	–	1.35	–	pF	
SID405	I _{WCO1}	Operating current (high power mode)	–	–	8	uA	

Table 39. Block Specs

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID257	T _{WS24} *	Number of wait states at 24 MHz	1	–	–		CPU execution from Flash
SID260	V _{REFSAR}	Trimmed internal reference to SAR	–1	–	+1	%	Percentage of V _{bg} (1.024 V). Guaranteed by characterization
SID261	F _{SARINTREF}	SAR operating speed without external reference bypass	–	–	100	ksps	12-bit resolution. Guaranteed by characterization
SID262	T _{CLKSWITCH}	Clock switching from clk1 to clk2 in clk1 periods	3	–	4	Periods	Guaranteed by design

* T_{WS24} is guaranteed by design

Packaging

The description of the SHM35920-M package dimensions follows.

Table 40. Packaging Dimensions

Spec ID#	Package	Description	Package Dwg #
PKG_1	68-pin QFN	68 QFN, 8 mm x 8 mm x 1.0 mm height	001-09618

Table 41. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T _A	Operating ambient temperature		-40	25	85	°C
T _J	Operating junction temperature		-40	—	100	°C
T _{JA}	Package θ _{JA} (68-pin QFN)		—	16.8	—	°C/Watt
T _{JC}	Package θ _{JC} (68-pin QFN)		—	2.9	—	°C/Watt

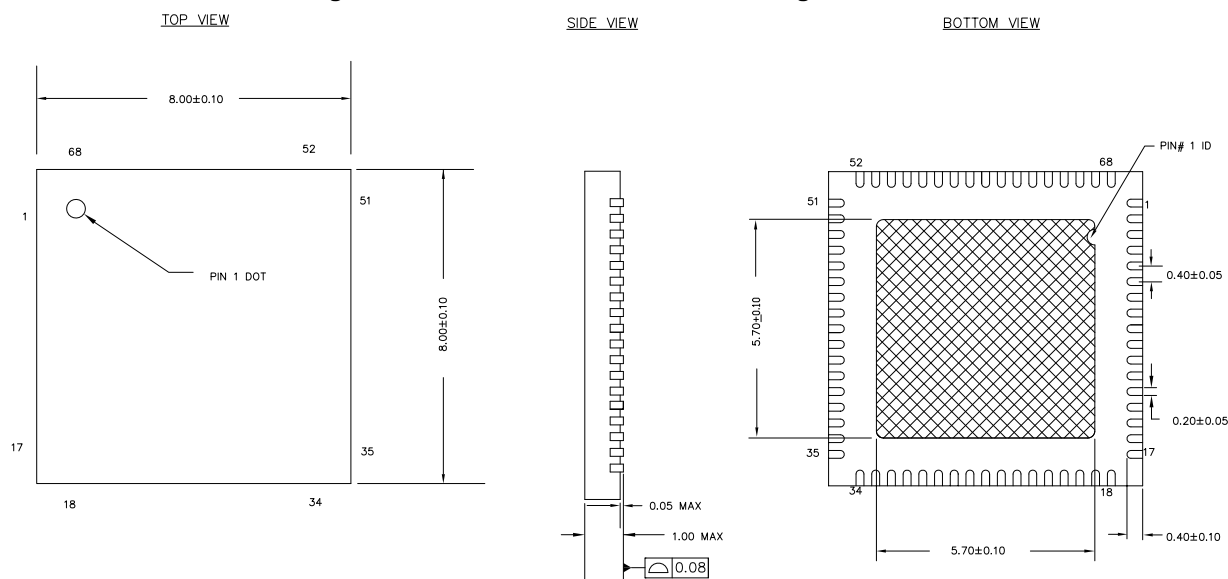
Table 42. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds


Table 43. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
All packages	MSL 3

Figure 4. 68-Pin 8 x 8 x 1.0 mm QFN Package Outline



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

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Table 44. Acronyms Used in this Document *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA

Table 44. Acronyms Used in this Document *(continued)*

Acronym	Description
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal