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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	20
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SOIC (0.295", 7.50mm Width)
Supplier Device Package	24-SOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f652lpf-g-sne2

MB95650L Series

New 8FX 8-bit Microcontrollers

The MB95650L Series is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral functions.

Features

F²MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

Clock

- Selectable main clock source
  - Main oscillation clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)
  - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
  - Main CR clock (4 MHz ±2%)
  - Main CR PLL clock
    - The main CR PLL clock frequency becomes 8 MHz ±2% when the PLL multiplication rate is 2.
    - The main CR PLL clock frequency becomes 10 MHz ±2% when the PLL multiplication rate is 2.5.
    - The main CR PLL clock frequency becomes 12 MHz ±2% when the PLL multiplication rate is 3.
    - The main CR PLL clock frequency becomes 16 MHz ±2% when the PLL multiplication rate is 4.
  - Main PLL clock (maximum machine clock frequency: 16 MHz)
- Selectable subclock source
  - Suboscillation clock (32.768 kHz)
  - External clock (32.768 kHz)
  - Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 150 kHz)

Timer

- 8/16-bit composite timer × 2 channels
- Time-base timer × 1 channel
- Watch prescaler × 1 channel

UART/SIO × 1 channel (The channel can be used either as a UART/SIO channel or as an I²C bus interface channel.)

- The function of this channel can be switched between UART/SIO and I²C bus interface.
- Full duplex double buffer
- Capable of clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer

I²C bus interface × 2 channels (One of the two channels can be used either as an I²C bus interface channel or as a UART/SIO channel.)

- Supports Standard-mode and Fast-mode (400 kHz).
- Built-in wake-up function

LIN-UART

- Full duplex double buffer
- Capable of clock asynchronous serial data transfer and clock synchronous serial data transfer

External interrupt × 6 channels

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

8/12-bit A/D converter × 6 channels

8-bit or 12-bit resolution can be selected.

Low power consumption (standby) modes

There are four standby modes as follows:

- Stop mode
- Sleep mode
- Watch mode
- Time-base timer mode

I/O port

- MB95F652E/F653E/F654E/F656E (number of I/O ports: 21)
  - General-purpose I/O ports (CMOS I/O) : 17
  - General-purpose I/O ports (N-ch open drain) : 4
- MB95F652L/F653L/F654L/F656L (number of I/O ports: 20)
  - General-purpose I/O ports (CMOS I/O) : 17
  - General-purpose I/O ports (N-ch open drain) : 3

On-chip debug

- 1-wire serial control
- Serial writing supported (asynchronous mode)

Hardware/software watchdog timer

- Built-in hardware watchdog timer
- Built-in software watchdog timer

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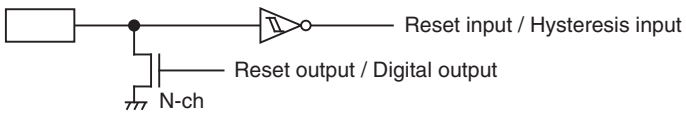
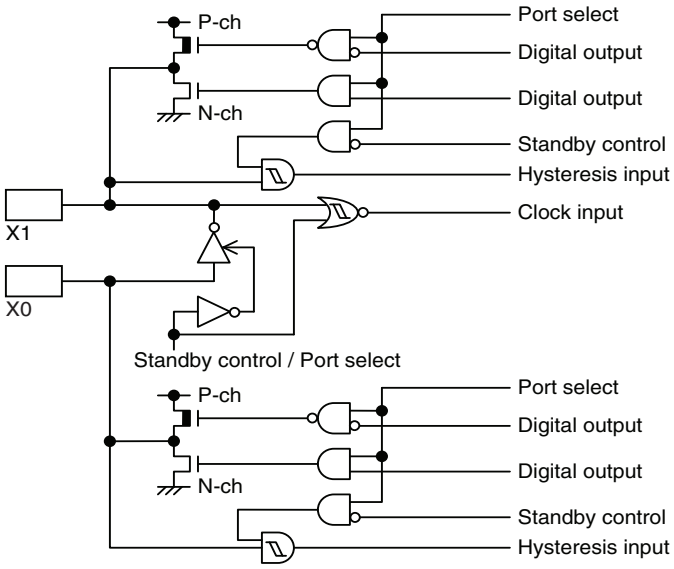
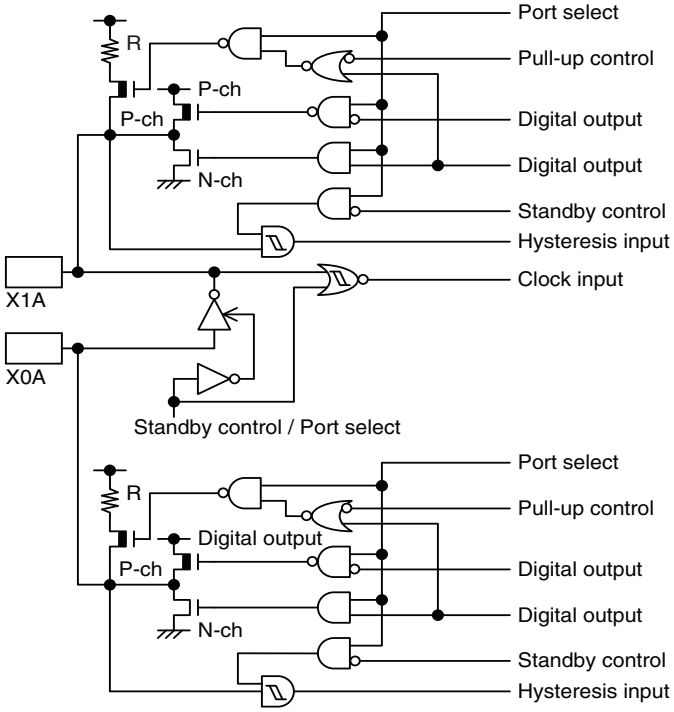
<table>
<tr><th>Part number
Parameter</th><th>MB95F652E</th><th>MB95F653E</th><th>MB95F654E</th><th>MB95F656E</th><th>MB95F652L</th><th>MB95F653L</th><th>MB95F654L</th><th>MB95F656L</th></tr>
<tr><td rowspan="2">UART/SIO</td><td colspan="8">1 channel (The channel can be used either as a UART/SIO channel or as an I²C bus interface channel.)</td></tr>
<tr><td colspan="8">• Data transfer with UART/SIO is enabled.
• It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function.
• It uses the NRZ type transfer format.
• LSB-first data transfer and MSB-first data transfer are available to use.
• Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.</td></tr>
<tr><td rowspan="2">I²C bus interface</td><td colspan="8">2 channels (One of the two channels can be used either as an I²C bus interface channel or as a UART/SIO channel.)</td></tr>
<tr><td colspan="8">• Master/slave transmission and reception
• It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.</td></tr>
<tr><td>Watch prescaler</td><td colspan="8">Eight different time intervals can be selected.</td></tr>
<tr><td>Flash memory</td><td colspan="8">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table>
<tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr>
<tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr>
</table></td></tr>
<tr><td>Standby mode</td><td colspan="8">There are four standby modes as follows:
• Stop mode
• Sleep mode
• Watch mode
• Time-base timer mode</td></tr>
<tr><td>Package</td><td colspan="8">FPT-24P-M10
FPT-24P-M34
LCC-32P-M19</td></tr>
</table>

6. I/O Circuit Type

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 5 MΩ • CMOS output • Hysteresis input • Pull-up control

(Continued)

9. Pin Connection

Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 1.0 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

DBG pin

Connect the DBG pin to an external pull-up resistor of 2 kΩ or above.

After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released.

The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

$\overline{\text{RST}}$ pin

Connect the $\overline{\text{RST}}$ pin to an external pull-up resistor of 2 kΩ or above.

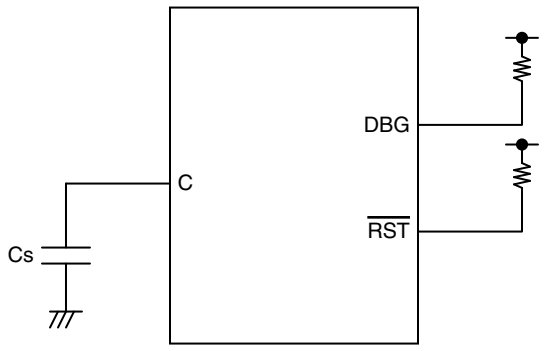
To prevent the device from unintentionally entering the reset mode due to noise, minimize the interconnection length between a pull-up resistor and the $\overline{\text{RST}}$ pin and that between a pull-up resistor and the V_{CC} pin when designing the layout of the printed circuit board.

The PF2/$\overline{\text{RST}}$ pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/$\overline{\text{RST}}$ pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

DBG/$\overline{\text{RST}}$/C pins connection diagram



Note on serial communication

In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, take measures such as adding a checksum to the end of data in order to detect errors. If an error is detected, retransmit the data.

13. Areas for Specific Applications

The general-purpose register area and vector table area are used for the specific applications.

General-purpose register area (Addresses: 0x0100 to 0x01FF*1)

- This area contains the auxiliary registers used for 8-bit arithmetic operations, transfer, etc.
- As this area forms part of the RAM area, it can also be used as conventional RAM.
- When the area is used as general-purpose registers, general-purpose register addressing enables high-speed access with short instructions.

Non-volatile register data area (Addresses: 0xFFBB to 0xFFBF)

- The area from 0xFFBB to 0xFFBF is used to store data of the non-volatile register. For details, refer to “Chapter 23 Non-volatile Register (NVR) Interface” in “New 8FX MB95650L Series Hardware Manual”.

Vector table area (Addresses: 0xFFC0 to 0xFFFF)

- This area is used as the vector table for vector call instructions (CALLV), interrupts, and resets.
- The top of the Flash memory area is allocated to the vector table area. The start address of a service routine is set to an address in the vector table in the form of data.

“16. Interrupt Source Table” lists the vector table addresses corresponding to vector call instructions, interrupts, and resets.

For details, refer to “Chapter 4 Reset”, “Chapter 5 Interrupts” and “A.2 Special Instruction Special Instruction CALLV #vct” in “New 8FX MB95650L Series Hardware Manual”.

Direct bank pointer and access area

Direct bank pointer (DP[2:0])	Operand-specified dir	Access area
0bXXX (It does not affect mapping.)	0x0000 to 0x007F	0x0000 to 0x007F
0b000 (Initial value)	0x0090 to 0x00FF	0x0090 to 0x00FF
0b001	0x0080 to 0x00FF	0x0100 to 0x017F
0b010		0x0180 to 0x01FF*1
0b011		0x0200 to 0x027F
0b100		0x0280 to 0x02FF*2
0b101		0x0300 to 0x037F
0b110		0x0380 to 0x03FF
0b111		0x0400 to 0x047F

*1: Due to the memory size limit, the available access area is up to “0x018F” in MB95F652E/F652L.

*2: Due to the memory size limit, the available access area is up to “0x028F” in MB95F653E/F653L.

15.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95650L Series Hardware Manual”.

15.1.1 Port 0 configuration

Port 0 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 0 data register (PDR0)
- Port 0 direction register (DDR0)
- Port 0 pull-up register (PUL0)
- A/D input disable register (lower) (AIDRL)

15.1.2 Block diagrams of port 0

P00/AN00 pin

This pin has the following peripheral function:

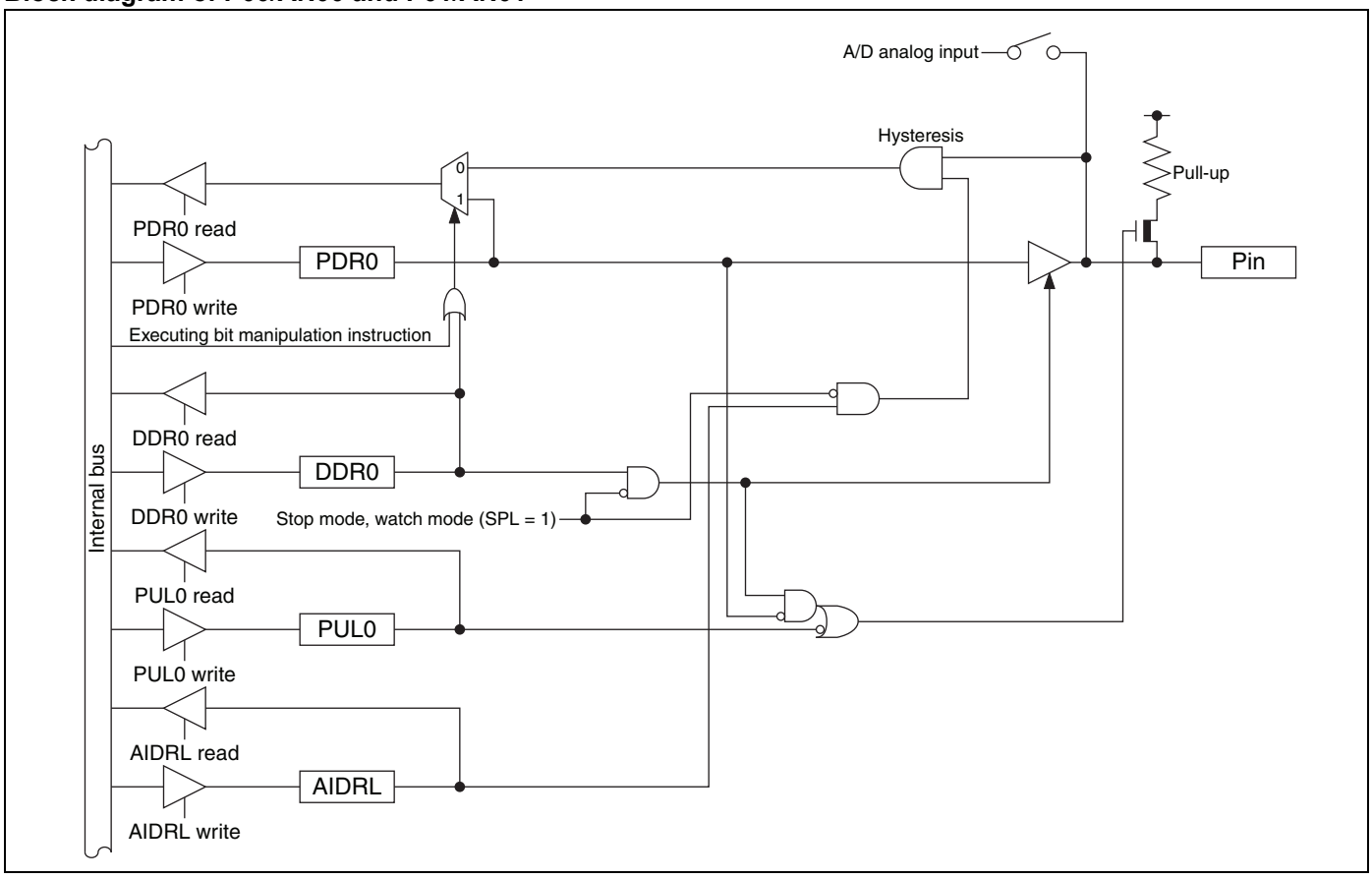
- 8/12-bit A/D converter analog input pin (AN00)

P01/AN01 pin

This pin has the following peripheral function:

- 8/12-bit A/D converter analog input pin (AN01)

Block diagram of P00/AN00 and P01/AN01



P02/INT02/AN02/SCK pin

This pin has the following peripheral functions:

- External interrupt input pin (INT02)
- 8/12-bit A/D converter analog input pin (AN02)
- LIN-UART clock I/O pin (SCK)

P03/INT03/AN03/SOT pin

This pin has the following peripheral functions:

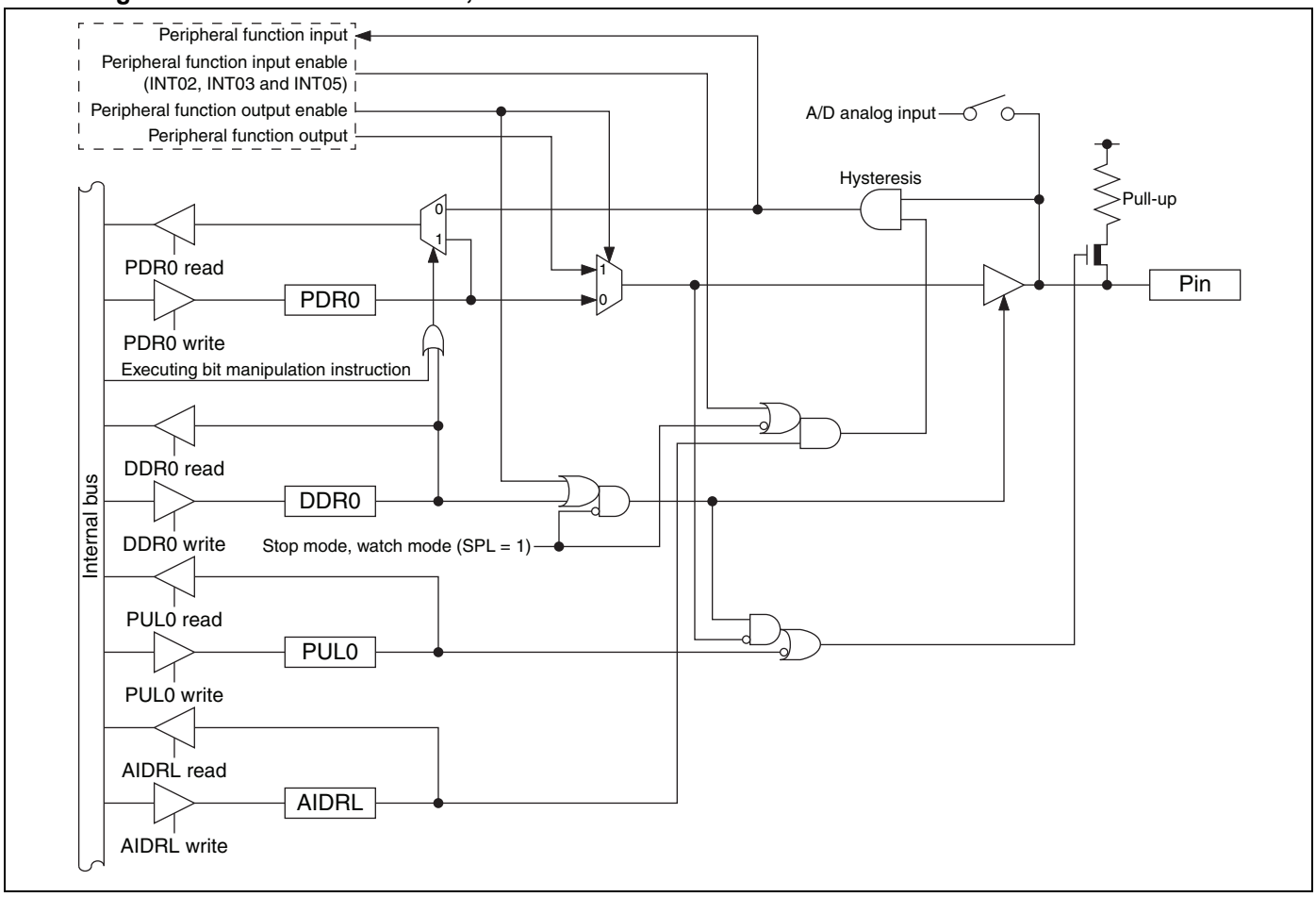
- External interrupt input pin (INT03)
- 8/12-bit A/D converter analog input pin (AN03)
- LIN-UART data output pin (SOT)

P05/INT05/AN05/TO00 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT05)
- 8/16-bit composite timer ch. 0 output pin (TO00)

Block diagram of P02/INT02/AN02/SCK, P03/INT03/AN03/SOT and P05/INT05/AN05/TO00

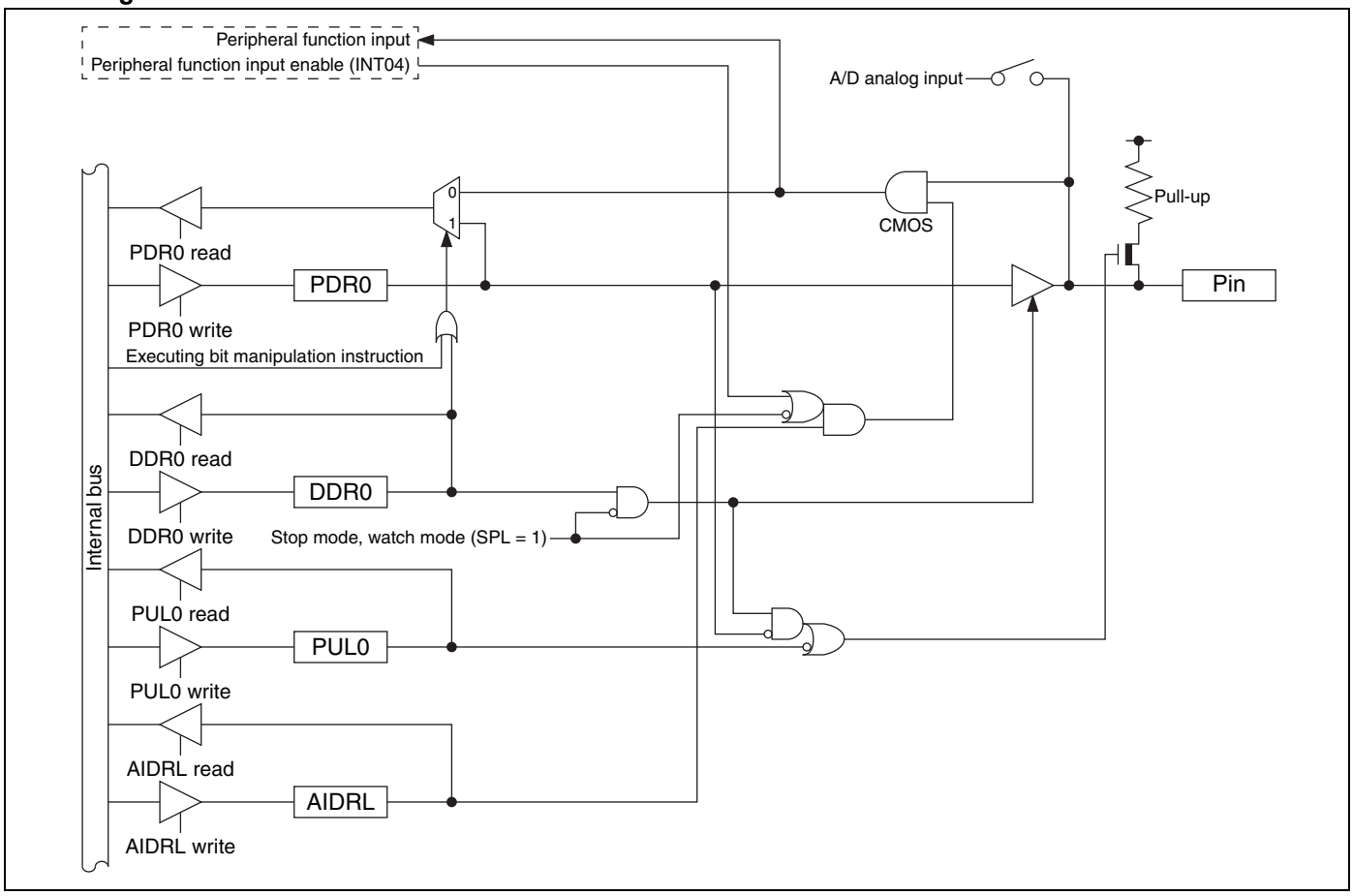


P04/INT04/AN04/SIN/EC0 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT04)
- 8/12-bit A/D converter analog input pin (AN04)
- LIN-UART data input pin (SIN)
- 8/16-bit composite timer ch. 0 clock input pin (EC0)

Block diagram of P04/INT04/AN04/SIN/EC0



15.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95650L Series Hardware Manual”.

15.2.1 Port 1 configuration

Port 1 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)

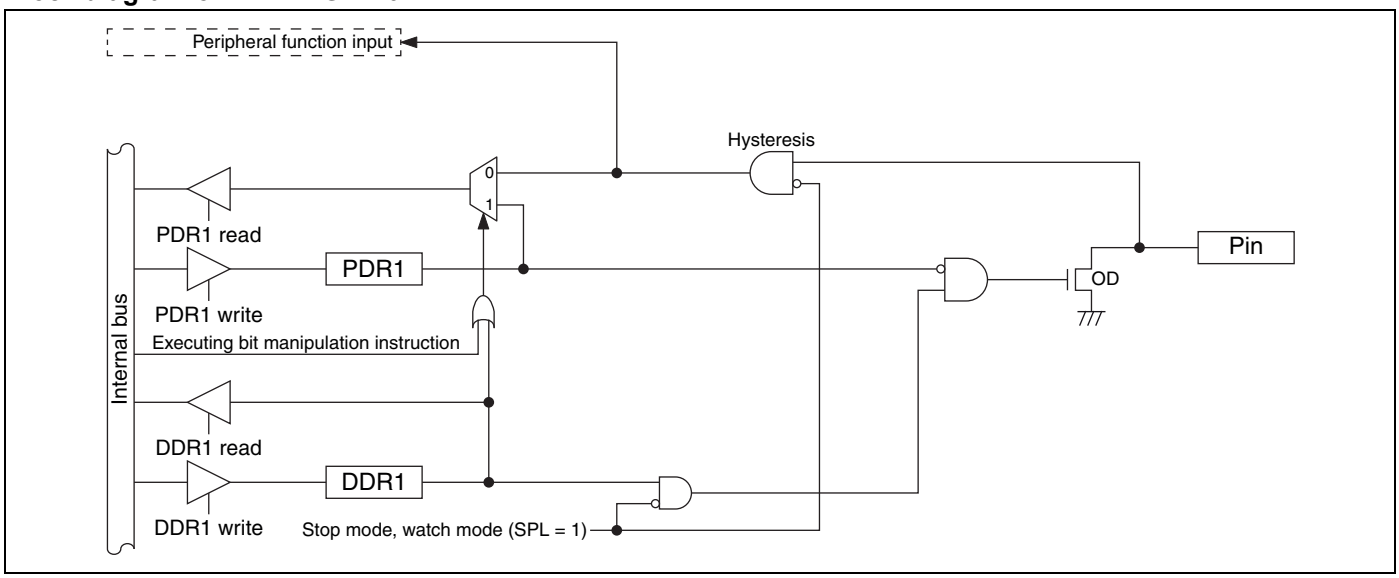
15.2.2 (2)Block diagrams of port 1

P12/DBG/EC0 pin

This pin has the following peripheral functions:

- DBG input pin (DBG)
- 8/16-bit composite timer ch. 0 clock input pin (EC0)

Block diagram of P12/DBG/EC0



P14/SDA0 pin

This pin has the following peripheral function:

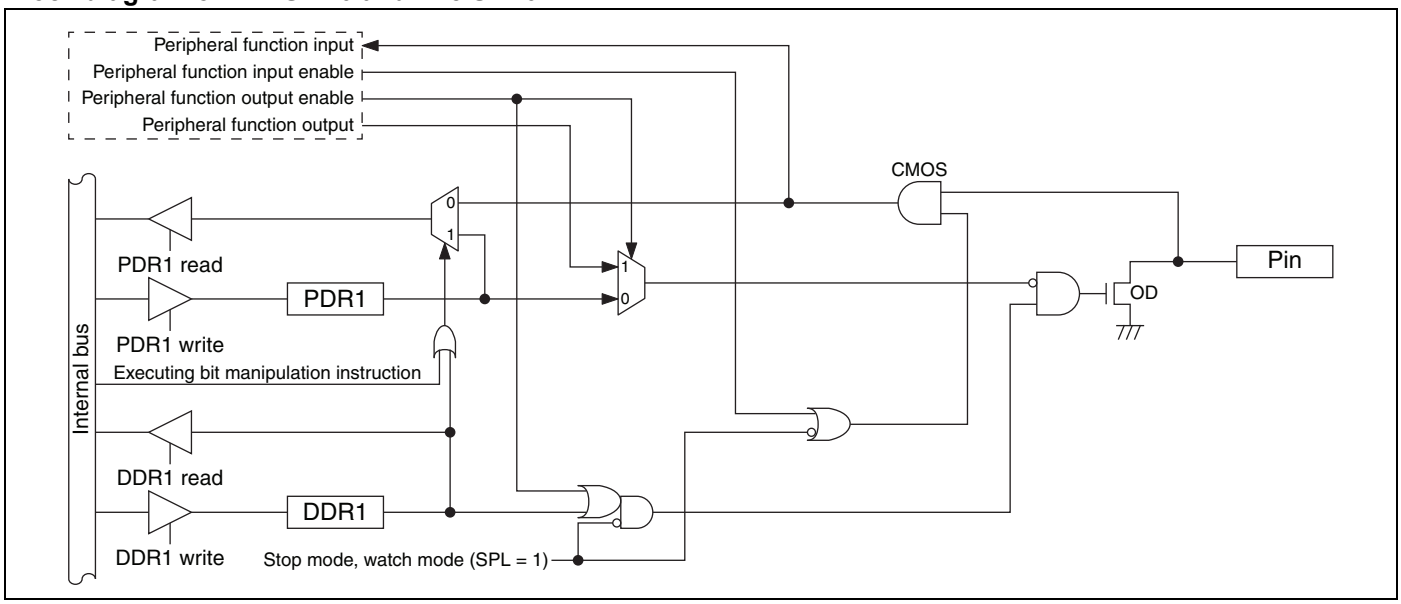
- I^2C bus interface ch. 0 data I/O pin (SDA0)

P15/SCL0 pin

This pin has the following peripheral function:

- I^2C bus interface ch. 0 clock I/O pin (SCL0)

Block diagram of P14/SDA0 and P15/SCL0



15.5.3 Port G registers

Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

Correspondence between registers and pins for port G

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PG2**	**PG1**	**-**
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

15.5.4 Port G operations

Operation as an output port

- A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
- If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- Reading the PDRG register returns the PDRG register value.

Operation as an input port

- A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

Operation at reset

If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

Operation of the pull-up register

Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

18.3 DC Characteristics

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI1}	P04, P16, P17	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input level
	V_{IHI2}	P14, P15	*1	0.7 V_{CC}	—	V_{CC} + 5.5	V	CMOS input level
	V_{IHS}	P00 to P03, P05 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{ILI}	P04, P14 to P17	*1	V_{SS} − 0.3	—	0.3 V_{CC}	V	CMOS input level
	V_{ILS}	P00 to P03, P05 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_{D1}	P12, PF2	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
	V_{D2}	P14, P15	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
	V_{D3}	P16, P17	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	In I^2C mode
"H" level output voltage	V_{OH1}	Output pins other than P05 to P07, P12, P62, P63	I_{OH} = −4 mA*2	V_{CC} − 0.5	—	—	V	
	V_{OH2}	P05 to P07, P62, P63	I_{OH} = −8 mA*3	V_{CC} − 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P05 to P07, P62, P63	I_{OL} = 4 mA*4	—	—	0.4	V	
	V_{OL2}	P05 to P07, P62, P63	I_{OL} = 12 mA*5	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	−5	—	+5	µA	When the internal pull-up resistor is disabled
Internal pull-up resistor	R_{PULL}	P00 to P07, P62 to P64, PG1, PG2	V_I = 0 V	75	100	150	kΩ	When the internal pull-up resistor is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

(Continued)

18.4 AC Characteristics

18.4.1 Clock Timing

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	—	1	—	32.5	MHz	When the main external clock is used
		X0, X1	—	—	4	—	MHz	When the main PLL clock is used
	F_{CRH}	—	—	3.92	4	4.08	MHz	Operating conditions • The main CR clock is used. • 0 °C ≤ T_A ≤ +70 °C
				3.8	4	4.2	MHz	Operating conditions • The main CR clock is used. • –40 °C ≤ T_A < 0 °C, +70 °C < T_A ≤ +85 °C
	F_{MCRPLL}	—	—	7.84	8	8.16	MHz	Operating conditions • PLL multiplication rate: 2 • 0 °C ≤ T_A ≤ +70 °C
				7.6	8	8.4	MHz	Operating conditions • PLL multiplication rate: 2 • –40 °C ≤ T_A < 0 °C, +70 °C < T_A ≤ +85 °C
				9.8	10	10.2	MHz	Operating conditions • PLL multiplication rate: 2.5 • 0 °C ≤ T_A ≤ +70 °C
				9.5	10	10.5	MHz	Operating conditions • PLL multiplication rate: 2.5 • –40 °C ≤ T_A < 0 °C, +70 °C < T_A ≤ +85 °C
				11.76	12	12.24	MHz	Operating conditions • PLL multiplication rate: 3 • 0 °C ≤ T_A ≤ +70 °C
				11.4	12	12.6	MHz	Operating conditions • PLL multiplication rate: 3 • –40 °C ≤ T_A < 0 °C, +70 °C < T_A ≤ +85 °C
				15.68	16	16.32	MHz	Operating conditions • PLL multiplication rate: 4 • 0 °C ≤ T_A ≤ +70 °C
				15.2	16	16.8	MHz	Operating conditions • PLL multiplication rate: 4 • –40 °C ≤ T_A < 0 °C, +70 °C < T_A ≤ +85 °C
	F_{MPLL}	—	—	8	—	16	MHz	When the main PLL clock is used

(Continued)

(Continued)

(V_{CC} = 1.8 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.25	—	4	MHz	When the main CR clock is used
			0.25	—	16	MHz	When the main PLL clock is used
			0.25	—	16	MHz	When the main CR PLL clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the suboscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

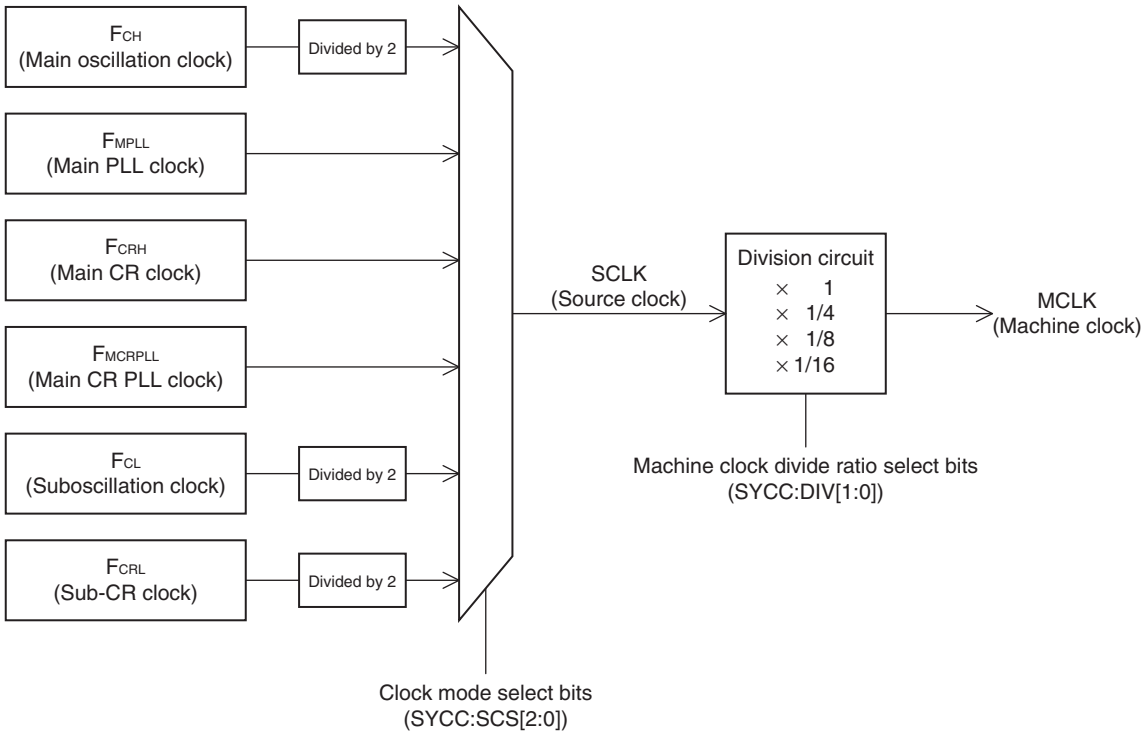
*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- PLL multiplication of main clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Main CR clock
- PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Subclock divided by 2
- Sub-CR clock divided by 2

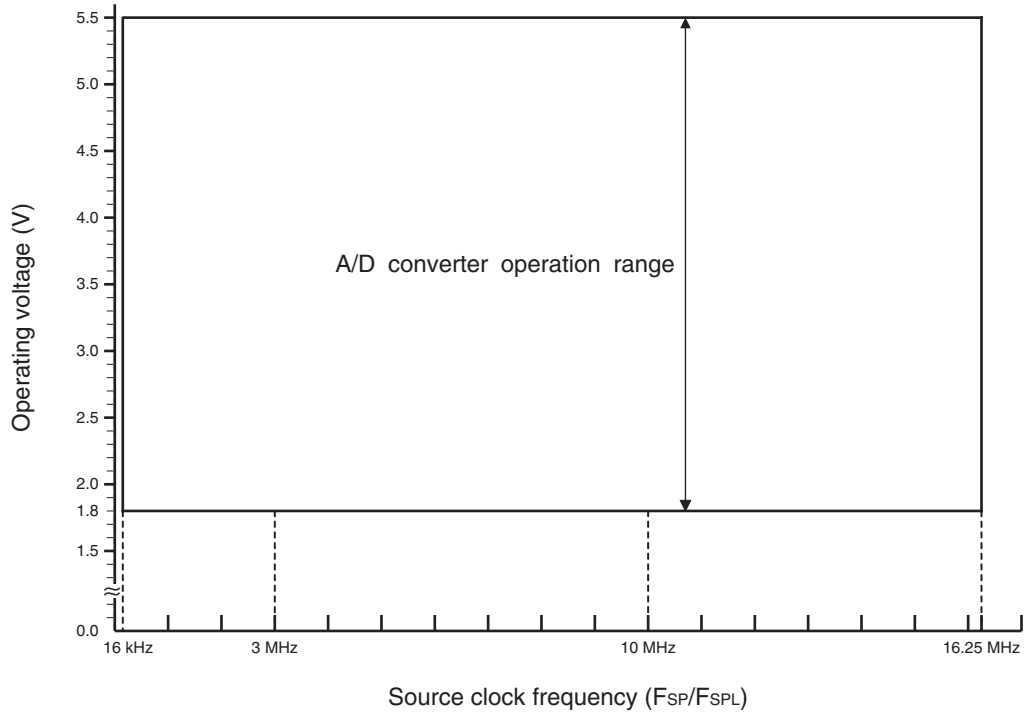
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

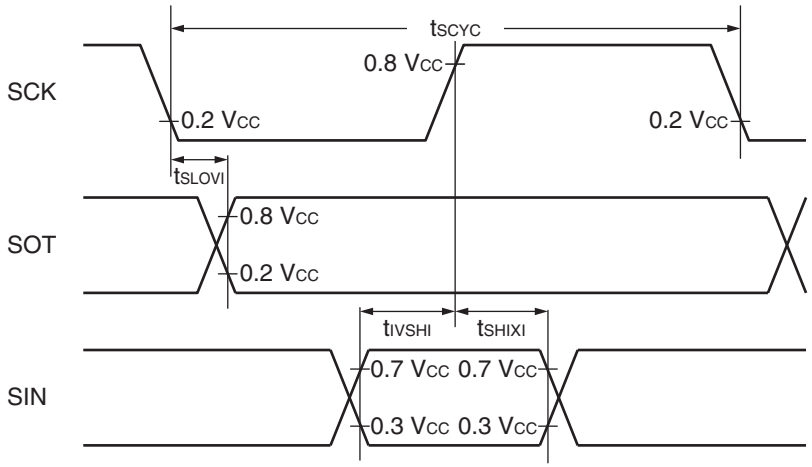
Schematic diagram of the clock generation block



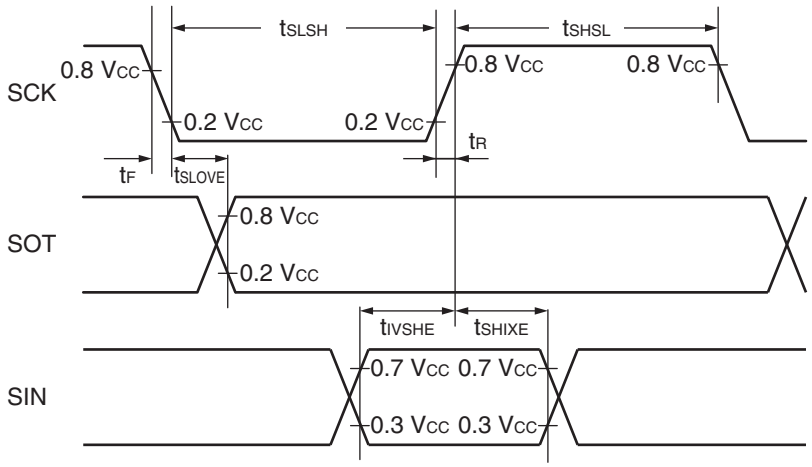
Operating voltage - Operating frequency (T_A = −40 °C to +85 °C)



Internal shift clock mode



External shift clock mode



*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 – t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 10	—	ns
SCK↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK↓	t_{IVSLE}	SCK, SIN		30	—	ns
SCK↓→ valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL0, SCL1	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL0, SCL1		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL0, SCL1, SDA0, SDA1		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL0, SCL1, SDA0, SDA1		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL0, SCL1, SDA0, SDA1		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t_{BUF}	SCL0, SCL1, SDA0, SDA1		$(2\ nm + 4)\ t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL0, SCL1, SDA0, SDA1		$3\ t_{MCLK} - 20$	—	ns	Master mode

(Continued)