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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	24-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f654epft-g-sne2

Power-on reset

A power-on reset is generated when the power is switched on.

Low-voltage detection reset circuit and low-voltage detection interrupt circuit (only available on MB95F652E/F653E/F654E/F656E)

Built-in low-voltage detection function

Clock supervisor counter

Built-in clock supervisor counter

Dual operation Flash memory

The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

Flash memory security function

Protects the content of the Flash memory.

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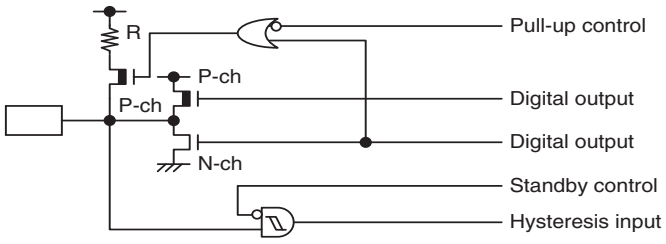
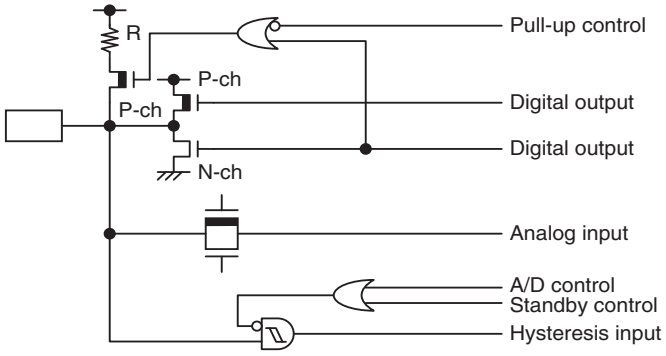
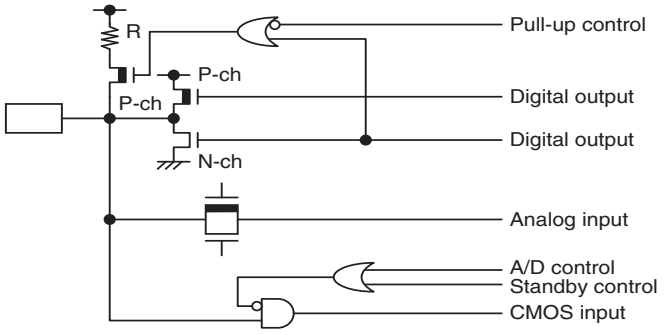
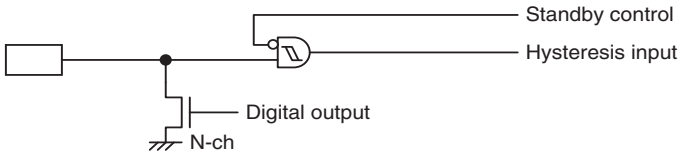
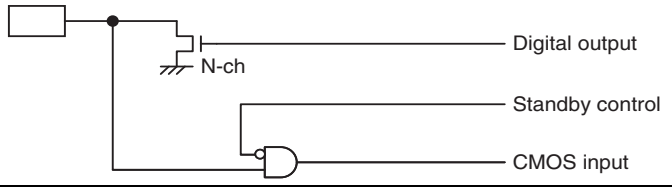
Type	Circuit	Remarks
D		• CMOS output • Hysteresis input • Pull-up control • High current output
E		• CMOS output • Hysteresis input • Pull-up control • Analog input
F		• CMOS output • CMOS input • Pull-up control • Analog input
H		• N-ch open drain output • Hysteresis input
I		• N-ch open drain output • CMOS input

(Continued)

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%.
   Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

7.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

14. I/O Map

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E to 0x0015	—	(Disabled)	—	—
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018 to 0x0027	—	(Disabled)	—	—
0x0028	PDRF	Port F data register	R/W	0b00000000
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	PUL0	Port 0 pull-up register	R/W	0b00000000
0x002D to 0x0032	—	(Disabled)	—	—
0x0033	PUL6	Port 6 pull-up register	R/W	0b00000000
0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A to 0x0048	—	(Disabled)	—	—

(Continued)

P06/INT06/TO01 pin

This pin has the following peripheral functions:

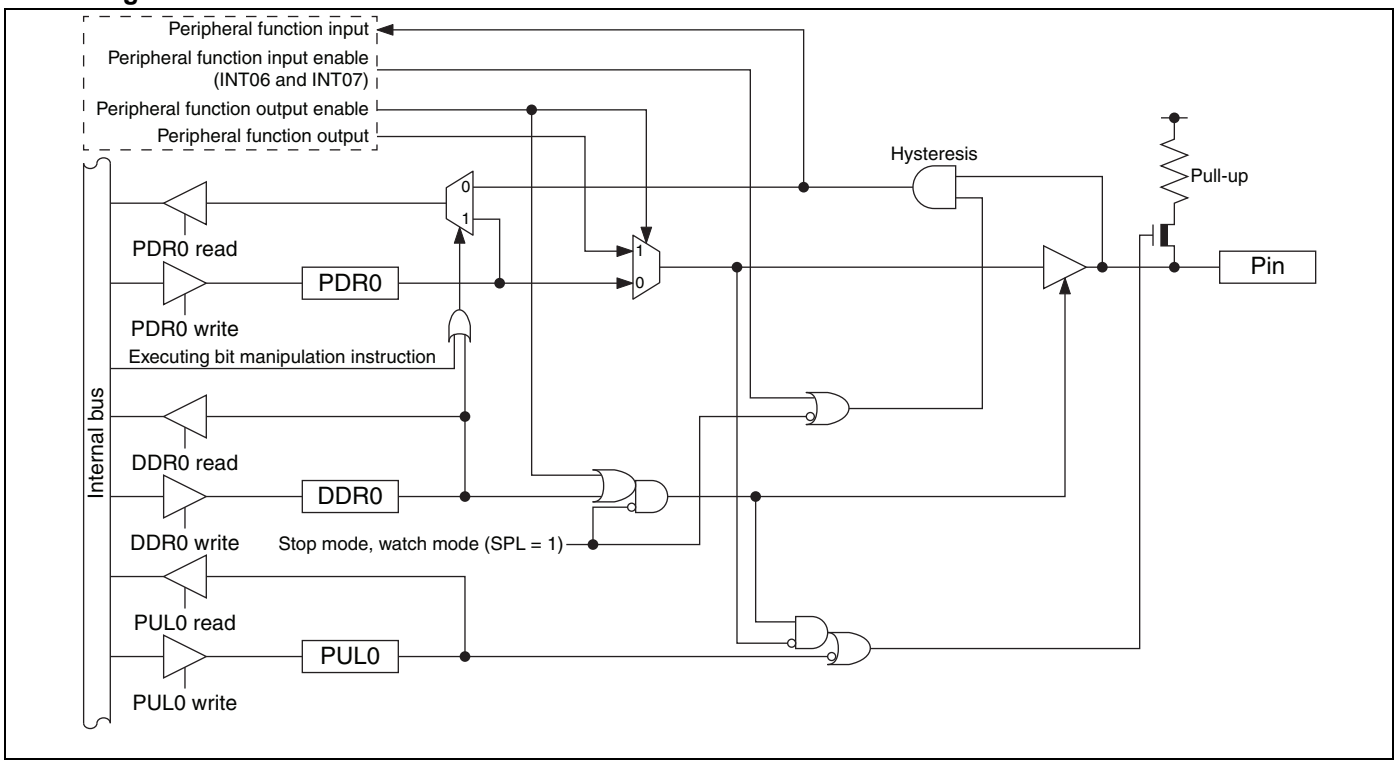
- External interrupt input pin (INT06)
- 8/16-bit composite timer ch. 0 output pin (TO01)

P07/INT07/TO10 pin

This pin has the following peripheral functions:

- External interrupt input pin (INT07)
- 8/16-bit composite timer ch. 1 output pin (TO10)

Block diagram of P06/INT06/TO01 and P07/INT07/TO10



15.1.3 Port 0 registers

Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR0	0	Pin state is “L” level.	PDR0 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR0 value is “1”.	As output port, outputs “H” level.
DDR0	0	Port input enabled		
	1	Port output enabled		
PUL0	0	Pull-up disabled		
	1	Pull-up enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

Correspondence between registers and pins for port 0

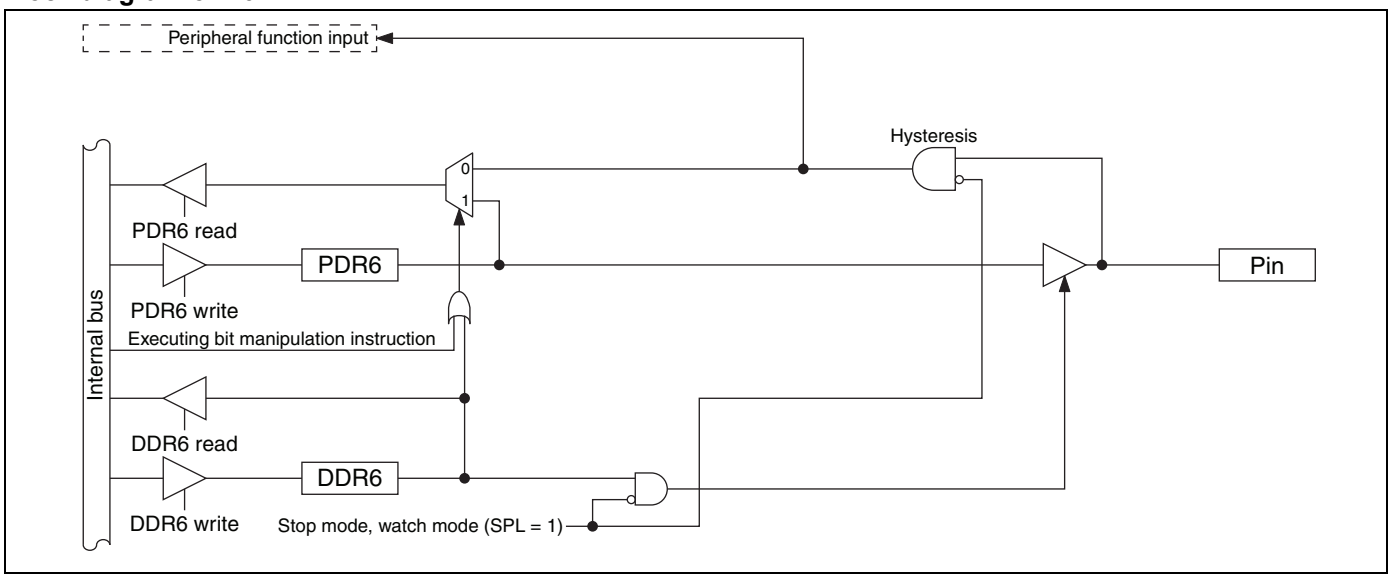
	Correspondence between related register bits and pins							
Pin name	**P07**	**P06**	**P05**	**P04**	**P03**	**P02**	**P01**	**P00**
PDR0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR0								
PUL0								
AIDRL	-	-						

P64/EC1 pin

This pin has the following peripheral function:

- 8/16-bit composite timer ch. 1 clock input pin (EC1)

Block diagram of P64/EC1



16. Interrupt Source Table

Interrupt source	Interrupt request number	Vector table address		Interrupt level setting register		Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower	Register	Bit	
External interrupt ch. 4	IRQ00	0xFFFA	0xFFFB	ILR0	L00 [1:0]	High
External interrupt ch. 5	IRQ01	0xFFF8	0xFFF9	ILR0	L01 [1:0]	
External interrupt ch. 2	IRQ02	0xFFF6	0xFFF7	ILR0	L02 [1:0]	
External interrupt ch. 6						
External interrupt ch. 3	IRQ03	0xFFF4	0xFFF5	ILR0	L03 [1:0]	
External interrupt ch. 7						
Low-voltage detection interrupt circuit	IRQ04	0xFFF2	0xFFF3	ILR1	L04 [1:0]	
UART/SIO ch. 0						
8/16-bit composite timer ch. 0 (lower)	IRQ05	0xFFF0	0xFFF1	ILR1	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	0xFFEE	0xFFEF	ILR1	L06 [1:0]	
LIN-UART (reception)	IRQ07	0xFFEC	0xFFED	ILR1	L07 [1:0]	
LIN-UART (transmission)	IRQ08	0xFFEA	0xFFEB	ILR2	L08 [1:0]	
—	IRQ09	0xFFE8	0xFFE9	ILR2	L09 [1:0]	
I^2C bus interface ch. 1	IRQ10	0xFFE6	0xFFE7	ILR2	L10 [1:0]	
—	IRQ11	0xFFE4	0xFFE5	ILR2	L11 [1:0]	
—	IRQ12	0xFFE2	0xFFE3	ILR3	L12 [1:0]	
—	IRQ13	0xFFE0	0xFFE1	ILR3	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	0xFFDE	0xFFDF	ILR3	L14 [1:0]	
—	IRQ15	0xFFDC	0xFFDD	ILR3	L15 [1:0]	
I^2C bus interface ch. 0	IRQ16	0xFFDA	0xFFDB	ILR4	L16 [1:0]	
—	IRQ17	0xFFD8	0xFFD9	ILR4	L17 [1:0]	
8/12-bit A/D converter	IRQ18	0xFFD6	0xFFD7	ILR4	L18 [1:0]	
Time-base timer	IRQ19	0xFFD4	0xFFD5	ILR4	L19 [1:0]	
Watch prescaler	IRQ20	0xFFD2	0xFFD3	ILR5	L20 [1:0]	
—	IRQ21	0xFFD0	0xFFD1	ILR5	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	0xFFCE	0xFFCF	ILR5	L22 [1:0]	
Flash memory	IRQ23	0xFFCC	0xFFCD	ILR5	L23 [1:0]	Low

17. Pin States in each Mode

Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
PF0/X0	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PF1/X1	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PF2/$\overline{\text{RST}}$	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input	Reset input*4
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PG1/X0A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
PG2/X1A	Oscillation input	Oscillation input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	—
	I/O port*1	I/O port*1	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Previous state kept - Input blocked*1, *2	- Hi-Z - Input blocked*1, *2	- Hi-Z - Input enabled*3 (However, it does not function.)
P00/AN00	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	- Previous state kept - Input blocked*2, *5	- Hi-Z*6 - Input blocked*2, *5	- Previous state kept - Input blocked*2, *5	- Hi-Z*6 - Input blocked*2, *5	- Hi-Z - Input blocked*2
P01/AN01							
P02/INT02/ AN02/SCK							
P03/INT03/ AN03/SOT							
P04/INT04/ AN04/SIN/ EC0							
P05/INT05/ AN05/TO00							

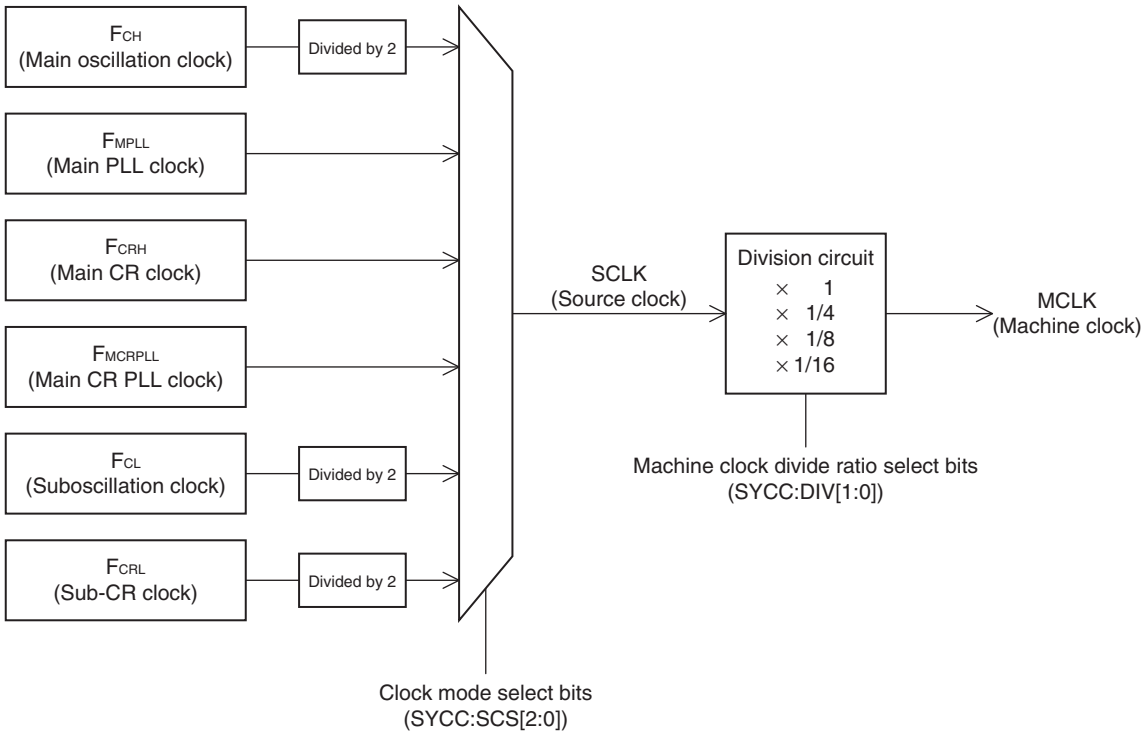
18.3 DC Characteristics

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

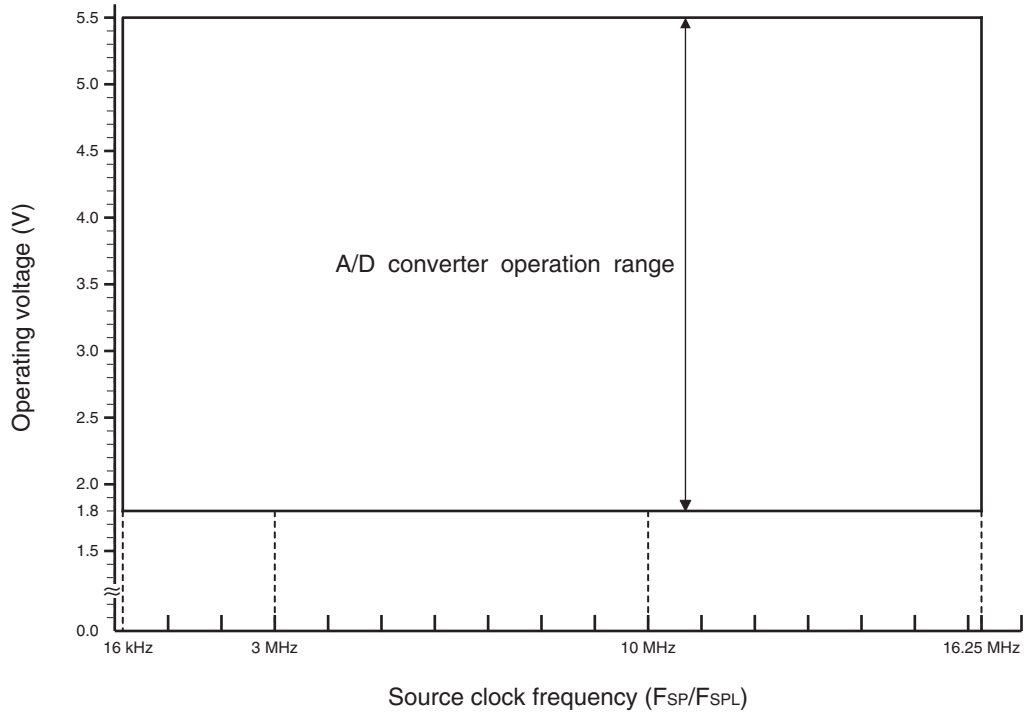
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI1}	P04, P16, P17	*1	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input level
	V_{IHI2}	P14, P15	*1	0.7 V_{CC}	—	V_{CC} + 5.5	V	CMOS input level
	V_{IHS}	P00 to P03, P05 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{ILI}	P04, P14 to P17	*1	V_{SS} − 0.3	—	0.3 V_{CC}	V	CMOS input level
	V_{ILS}	P00 to P03, P05 to P07, P12, P62 to P64, PF0, PF1, PG1, PG2	*1	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} − 0.3	—	0.2 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_{D1}	P12, PF2	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
	V_{D2}	P14, P15	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	
	V_{D3}	P16, P17	—	V_{SS} − 0.3	—	V_{SS} + 5.5	V	In I^2C mode
"H" level output voltage	V_{OH1}	Output pins other than P05 to P07, P12, P62, P63	I_{OH} = −4 mA*2	V_{CC} − 0.5	—	—	V	
	V_{OH2}	P05 to P07, P62, P63	I_{OH} = −8 mA*3	V_{CC} − 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P05 to P07, P62, P63	I_{OL} = 4 mA*4	—	—	0.4	V	
	V_{OL2}	P05 to P07, P62, P63	I_{OL} = 12 mA*5	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	−5	—	+5	µA	When the internal pull-up resistor is disabled
Internal pull-up resistor	R_{PULL}	P00 to P07, P62 to P64, PG1, PG2	V_I = 0 V	75	100	150	kΩ	When the internal pull-up resistor is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

(Continued)

Schematic diagram of the clock generation block



Operating voltage - Operating frequency (T_A = −40 °C to +85 °C)

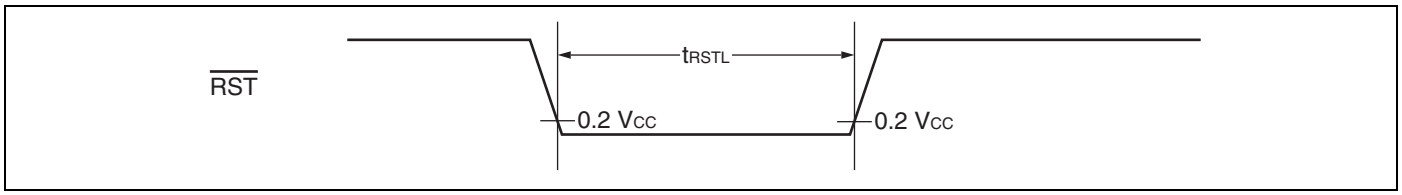


18.4.3 External Reset

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*	—	ns	

*: See "18.4.2. Source Clock/Machine Clock" for t_{MCLK}.



18.4.6 LIN-UART Timing

*Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

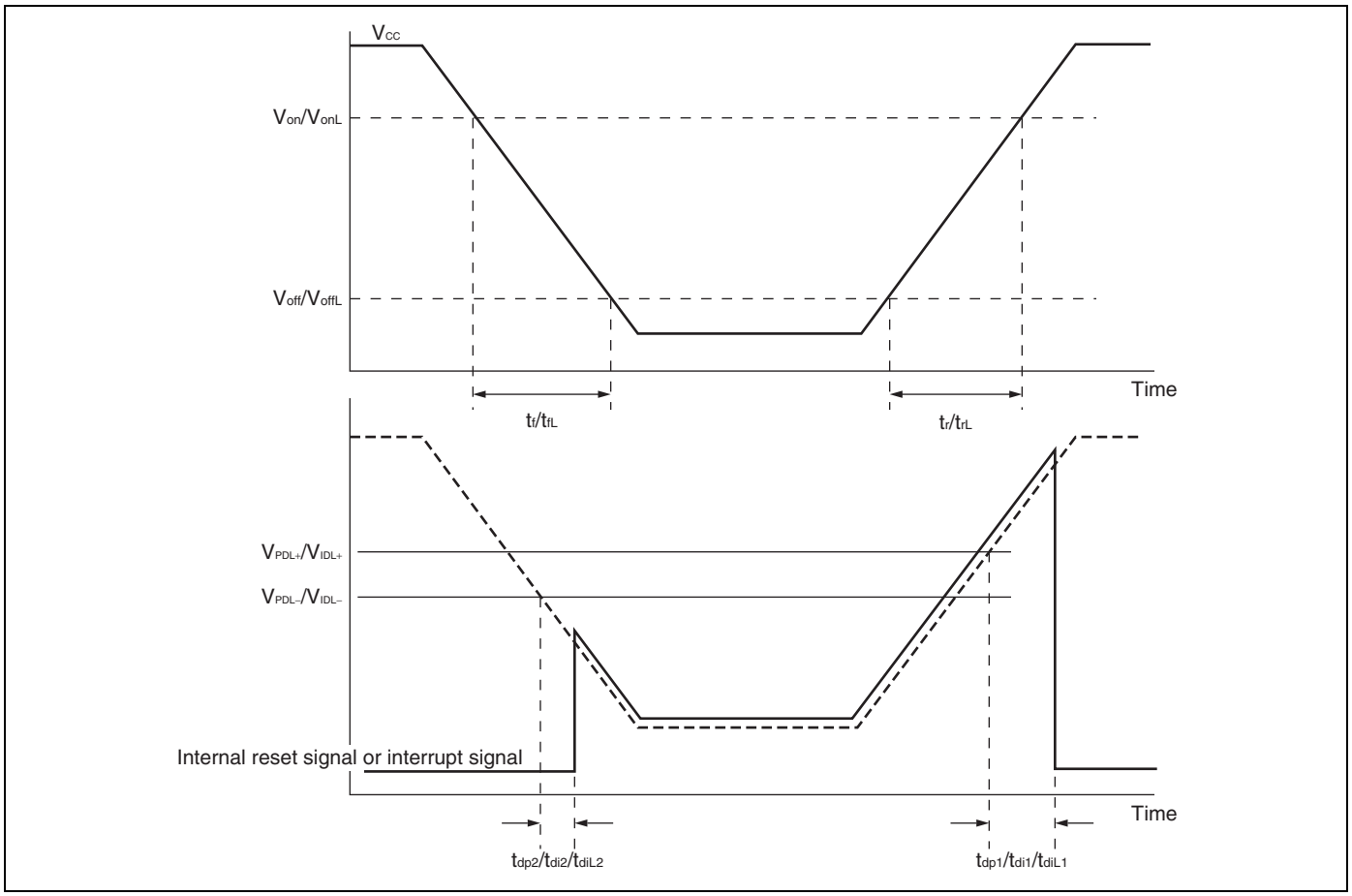
(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3–t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 10	—	ns
SCK↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK↑	t_{IVSHE}	SCK, SIN		30	—	ns
SCK↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.


V_{CC}
V_{on}/V_{onL}
V_{off}/V_{offL}
Time
t_f/t_{fL}
t_r/t_{rL}
V_{PDL+}/V_{IDL+}
V_{PDL-}/V_{IDL-}
Internal reset signal or interrupt signal
Time
$t_{dp2}/t_{di2}/t_{diL2}$
$t_{dp1}/t_{di1}/t_{diL1}$

18.5.3 Definitions of A/D Converter Terms

Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter.

When the number of bits is 12, analog voltage can be divided into 2^{12} = 4096.

Linearity error (unit: LSB)

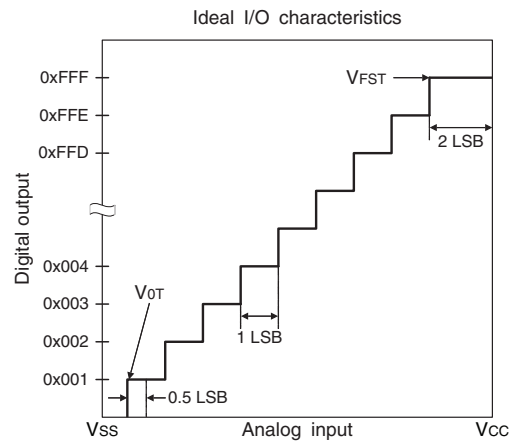
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“000000000000” ← → “000000000001”) of a device to the full-scale transition point (“111111111111” ← → “111111111110”) of the same device.

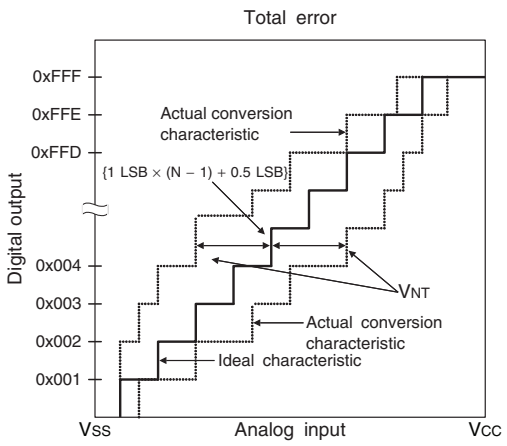
Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.





$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{4096}\ \text{V}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{LSB}$$

N : A/D converter digital output value

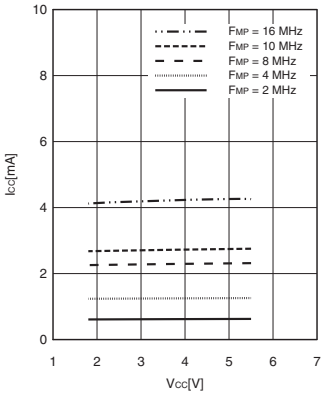
V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

(Continued)

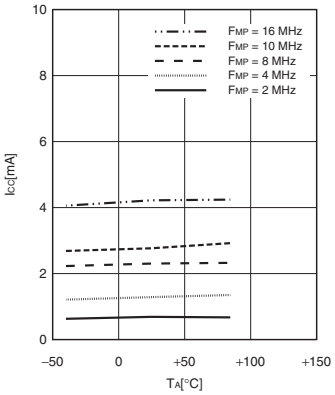
19. Sample Characteristics

Power supply current temperature characteristics

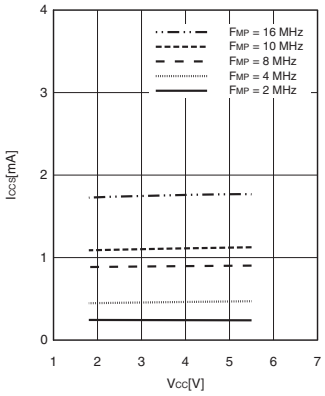
I_{CC} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



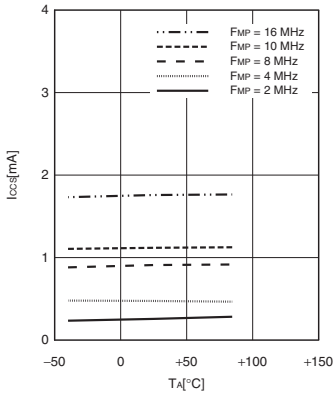
I_{CC} – T_A
V_{CC} = 3.3V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



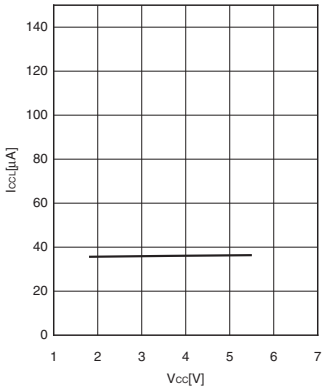
I_{CCS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



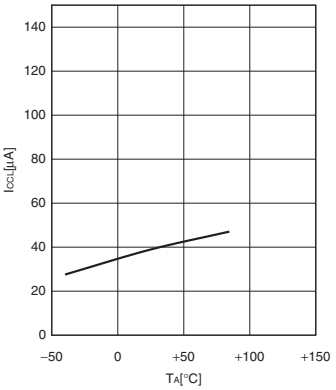
I_{CCS} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



I_{CCL} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating

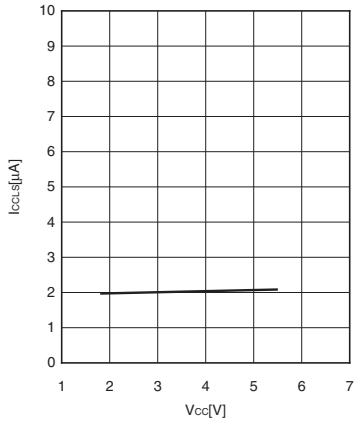


I_{CCL} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating

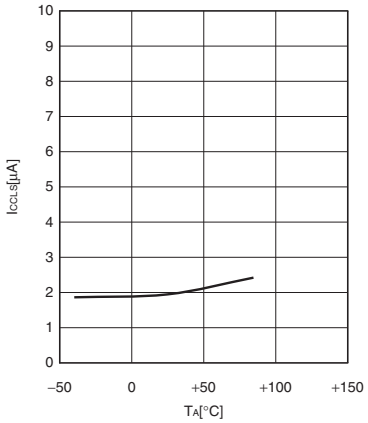


(Continued)

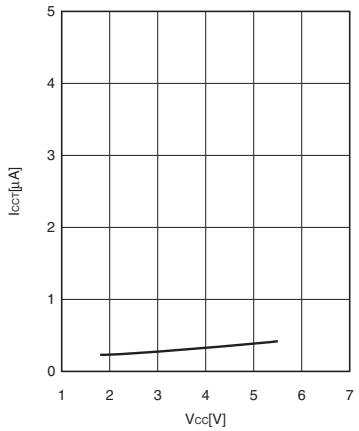
I_{CCLS} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



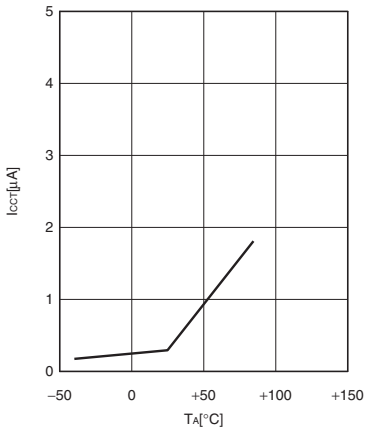
I_{CCLS} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



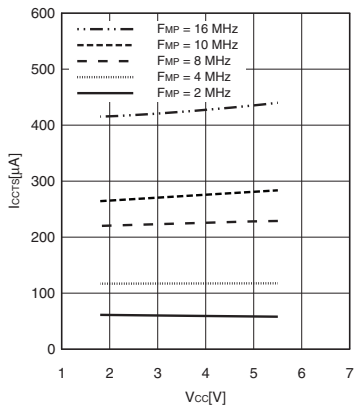
I_{CCT} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



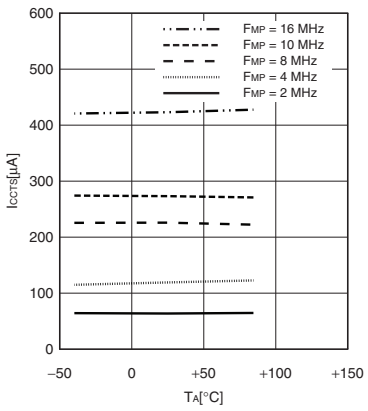
I_{CCT} – T_A
V_{CC} = 3.3 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



I_{CCTS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



I_{CCTS} – T_A
V_{CC} = 3.3 V, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating



21. Ordering Information

Part number	Package
MB95F652EPFT-G-SNE2 MB95F652LPFT-G-SNE2 MB95F653EPFT-G-SNE2 MB95F653LPFT-G-SNE2 MB95F654EPFT-G-SNE2 MB95F654LPFT-G-SNE2 MB95F656EPFT-G-SNE2 MB95F656LPFT-G-SNE2	24-pin plastic TSSOP (FPT-24P-M10)
MB95F652EPF-G-SNE2 MB95F652LPF-G-SNE2 MB95F653EPF-G-SNE2 MB95F653LPF-G-SNE2 MB95F654EPF-G-SNE2 MB95F654LPF-G-SNE2 MB95F656EPF-G-SNE2 MB95F656LPF-G-SNE2	24-pin plastic SOP (FPT-24P-M34)
MB95F652EWQN-G-SNE1 MB95F652EWQN-G-SNERE1 MB95F652LWQN-G-SNE1 MB95F652LWQN-G-SNERE1 MB95F653EWQN-G-SNE1 MB95F653EWQN-G-SNERE1 MB95F653LWQN-G-SNE1 MB95F653LWQN-G-SNERE1 MB95F654EWQN-G-SNE1 MB95F654EWQN-G-SNERE1 MB95F654LWQN-G-SNE1 MB95F654LWQN-G-SNERE1 MB95F656EWQN-G-SNE1 MB95F656EWQN-G-SNERE1 MB95F656LWQN-G-SNE1 MB95F656LWQN-G-SNERE1	32-pin plastic QFN (LCC-32P-M19)

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