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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, LINbus, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 6x8/12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SOIC (0.295", 7.50mm Width)
Supplier Device Package	24-SOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f656epf-g-sne2

(Continued)

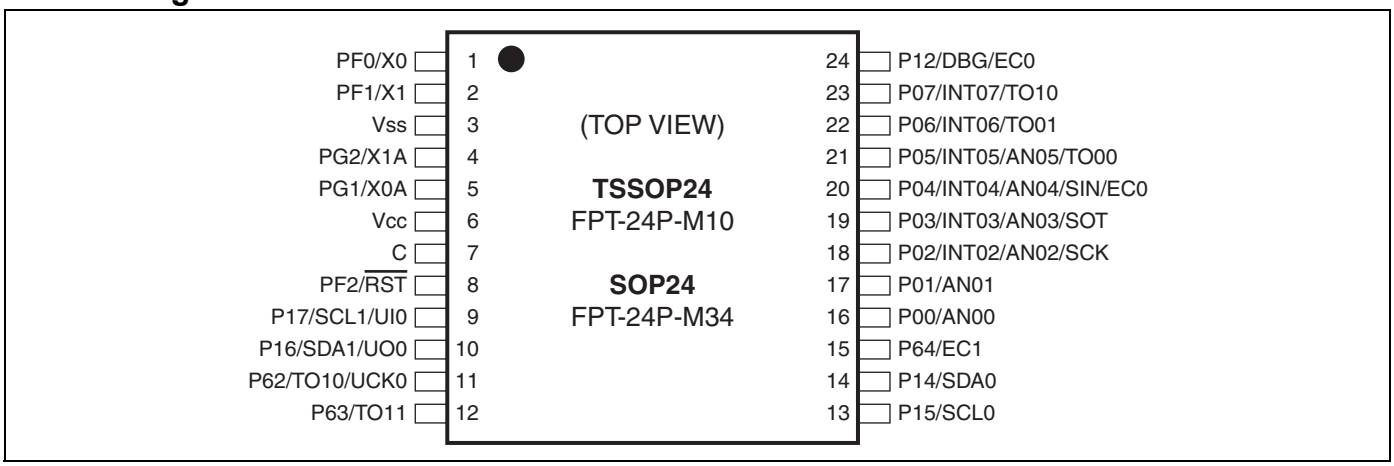
<table>
<tr><th>Part number
Parameter</th><th>MB95F652E</th><th>MB95F653E</th><th>MB95F654E</th><th>MB95F656E</th><th>MB95F652L</th><th>MB95F653L</th><th>MB95F654L</th><th>MB95F656L</th></tr>
<tr><td rowspan="2">UART/SIO</td><td colspan="8">1 channel (The channel can be used either as a UART/SIO channel or as an I²C bus interface channel.)</td></tr>
<tr><td colspan="8">• Data transfer with UART/SIO is enabled.
• It has a full duplex double buffer, variable data length (5/6/7/8 bits), an internal baud rate generator and an error detection function.
• It uses the NRZ type transfer format.
• LSB-first data transfer and MSB-first data transfer are available to use.
• Both clock asynchronous (UART) serial data transfer and clock synchronous (SIO) serial data transfer are enabled.</td></tr>
<tr><td rowspan="2">I²C bus interface</td><td colspan="8">2 channels (One of the two channels can be used either as an I²C bus interface channel or as a UART/SIO channel.)</td></tr>
<tr><td colspan="8">• Master/slave transmission and reception
• It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.</td></tr>
<tr><td>Watch prescaler</td><td colspan="8">Eight different time intervals can be selected.</td></tr>
<tr><td>Flash memory</td><td colspan="8">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table>
<tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr>
<tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr>
</table></td></tr>
<tr><td>Standby mode</td><td colspan="8">There are four standby modes as follows:
• Stop mode
• Sleep mode
• Watch mode
• Time-base timer mode</td></tr>
<tr><td>Package</td><td colspan="8">FPT-24P-M10
FPT-24P-M34
LCC-32P-M19</td></tr>
</table>

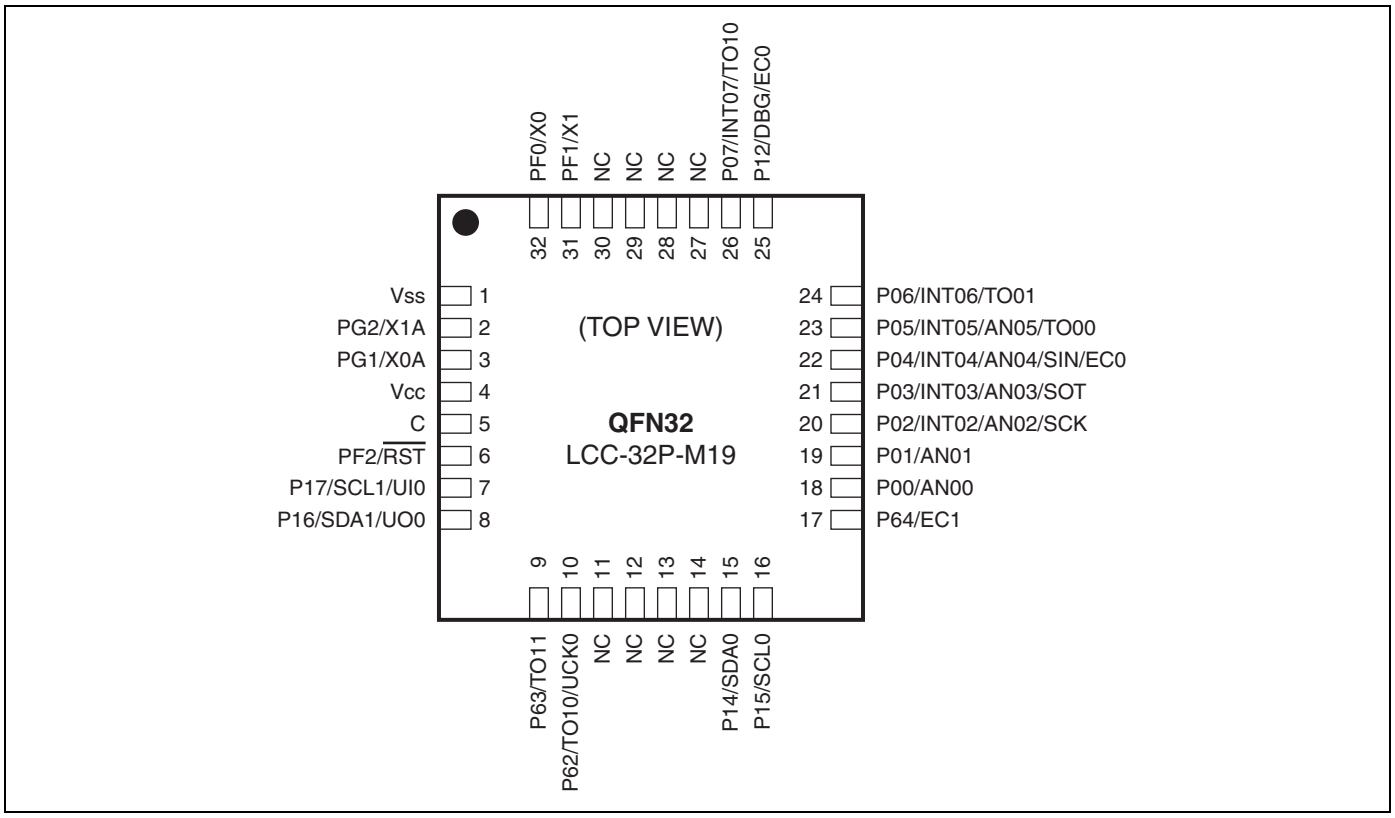
2. Packages and Corresponding Products

Part number / Package	MB95F652E	MB95F653E	MB95F654E	MB95F656E	MB95F652L	MB95F653L	MB95F654L	MB95F656L
FPT-24P-M10	O	O	O	O	O	O	O	O
FPT-24P-M34	O	O	O	O	O	O	O	O
LCC-32P-M19	O	O	O	O	O	O	O	O

O: Available

4. Pin Assignment





Pin no.		Pin name	I/O circuit type*4	Function	I/O type			
SOP24*1, TSSOP24*2	QFN32*3				Input	Output	OD*5	PU*6
16	18	P00	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		AN00		8/12-bit A/D converter analog input pin				
17	18	P01	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		AN01		8/12-bit A/D converter analog input pin				
18	20	P02	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT02		External interrupt input pin				
		AN02		8/12-bit A/D converter analog input pin				
		SCK		LIN-UART clock I/O pin				
19	21	P03	E	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		INT03		External interrupt input pin				
		AN03		8/12-bit A/D converter analog input pin				
		SOT		LIN-UART data output pin				
20	22	P04	F	General-purpose I/O port	CMOS/ analog	CMOS	—	O
		INT04		External interrupt input pin				
		AN04		8/12-bit A/D converter analog input pin				
		SIN		LIN-UART data input pin				
		EC0		8/16-bit composite timer ch. 0 clock input pin				
21	23	P05	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
		INT05		External interrupt input pin				
		AN05		8/12-bit A/D converter analog input pin				
		TO00		8/16-bit composite timer ch. 0 output pin				
22	24	P06	D	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		INT06		External interrupt input pin				
		TO01		8/16-bit composite timer ch. 0 output pin				
23	26	P07	K	General-purpose I/O port High-current pin	Hysteresis	CMOS	—	O
		INT07		External interrupt input pin				
		TO10		8/16-bit composite timer ch. 1 output pin				

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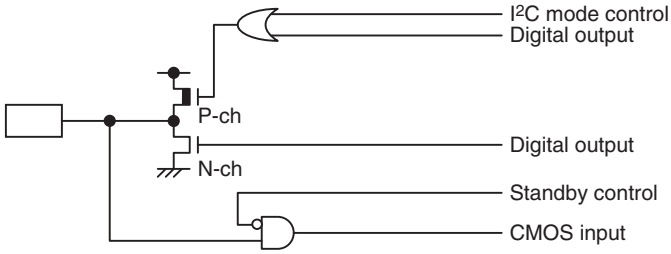
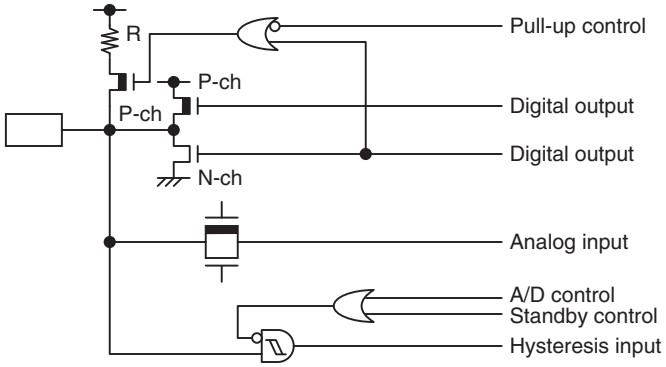
Type	Circuit	Remarks
J		• CMOS output • CMOS input • N-ch open drain output in I2C mode
K		• CMOS output • Hysteresis input • Pull-up control • Analog input • High current output

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%.
   Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

7.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

8. Notes On Device Handling

Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in “18.1 Absolute Maximum Ratings” of “18. Electrical Characteristics” is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

Stabilizing supply voltage

Supply voltage must be stabilized.

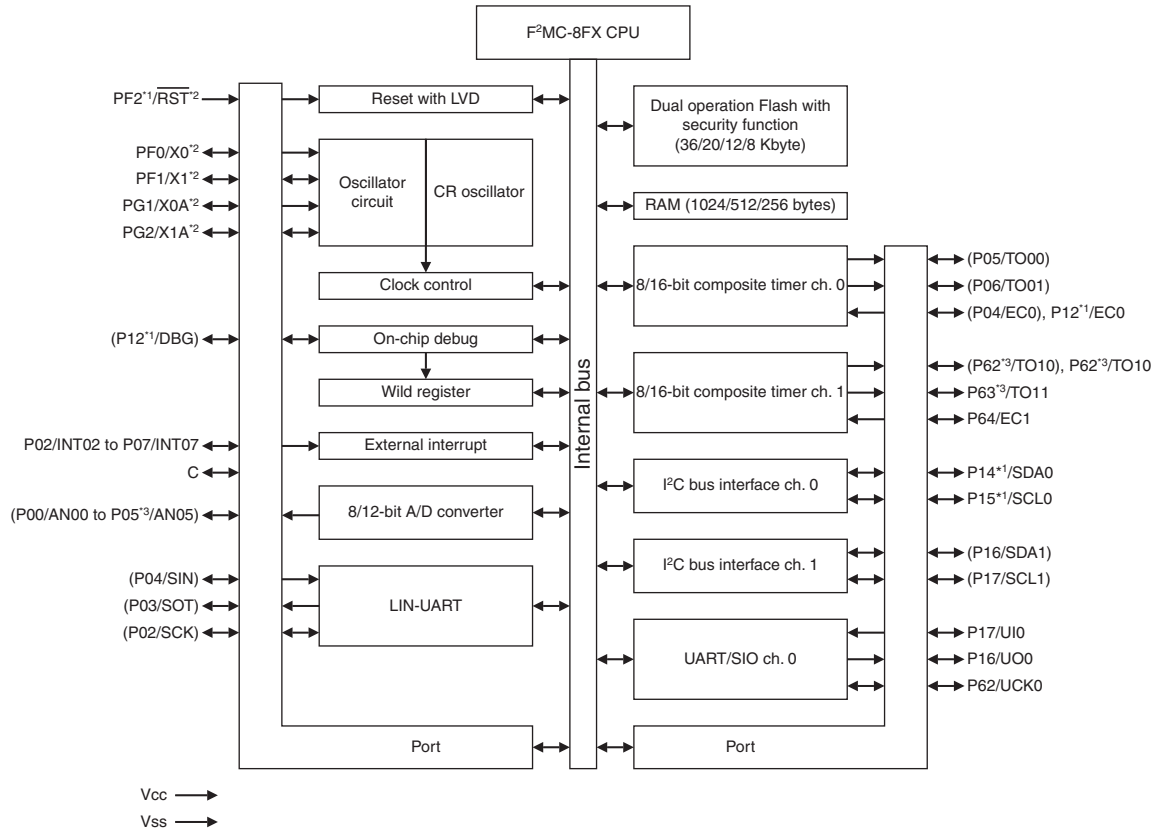
A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

10. Block Diagram



*1: P12, P14, P15 and PF2 are N-ch open drain pins.
*2: Software select
*3: P05 to P07, P62 and P63 are high-current pins.

Note: Pins in parentheses indicate that those pins are shared among different peripheral functions.

15.1.3 Port 0 registers

Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR0	0	Pin state is “L” level.	PDR0 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR0 value is “1”.	As output port, outputs “H” level.
DDR0	0	Port input enabled		
	1	Port output enabled		
PUL0	0	Pull-up disabled		
	1	Pull-up enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

Correspondence between registers and pins for port 0

	Correspondence between related register bits and pins							
Pin name	**P07**	**P06**	**P05**	**P04**	**P03**	**P02**	**P01**	**P00**
PDR0	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DDR0								
PUL0								
AIDRL	-	-						

15.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95650L Series Hardware Manual”.

15.2.1 Port 1 configuration

Port 1 is made up of the following elements.

- General-purpose I/O pins/peripheral function I/O pins
- Port 1 data register (PDR1)
- Port 1 direction register (DDR1)

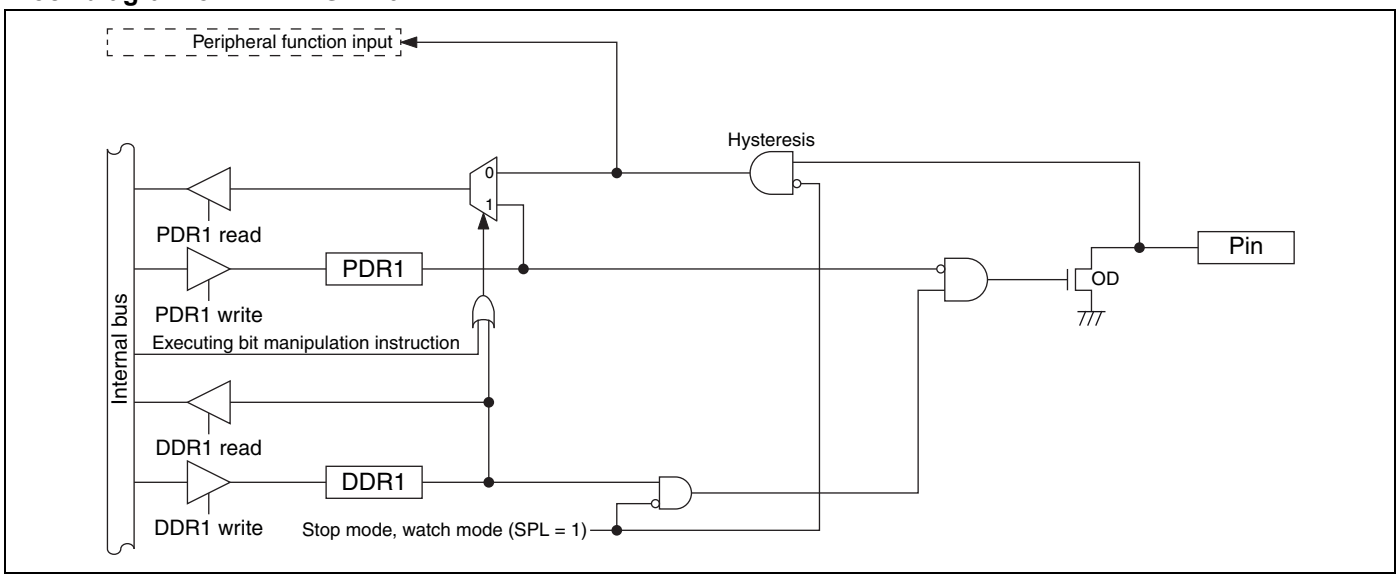
15.2.2 (2)Block diagrams of port 1

P12/DBG/EC0 pin

This pin has the following peripheral functions:

- DBG input pin (DBG)
- 8/16-bit composite timer ch. 0 clock input pin (EC0)

Block diagram of P12/DBG/EC0



15.2.4 Port 1 operations

Operation as an output port

- A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to “1”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
- If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- Reading the PDR1 register returns the PDR1 register value.

Operation as an input port

- A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to “0”.
- For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
- Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

Operation as a peripheral function output pin

- A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

Operation as a peripheral function input pin

- To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to “0”.
- Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

Operation at reset

If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

Operation in stop mode and watch mode

- If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR1 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

15.5.3 Port G registers

Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

Correspondence between registers and pins for port G

	Correspondence between related register bits and pins							
Pin name	**-**	**-**	**-**	**-**	**-**	**PG2**	**PG1**	**-**
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

(V_{CC} = 3.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

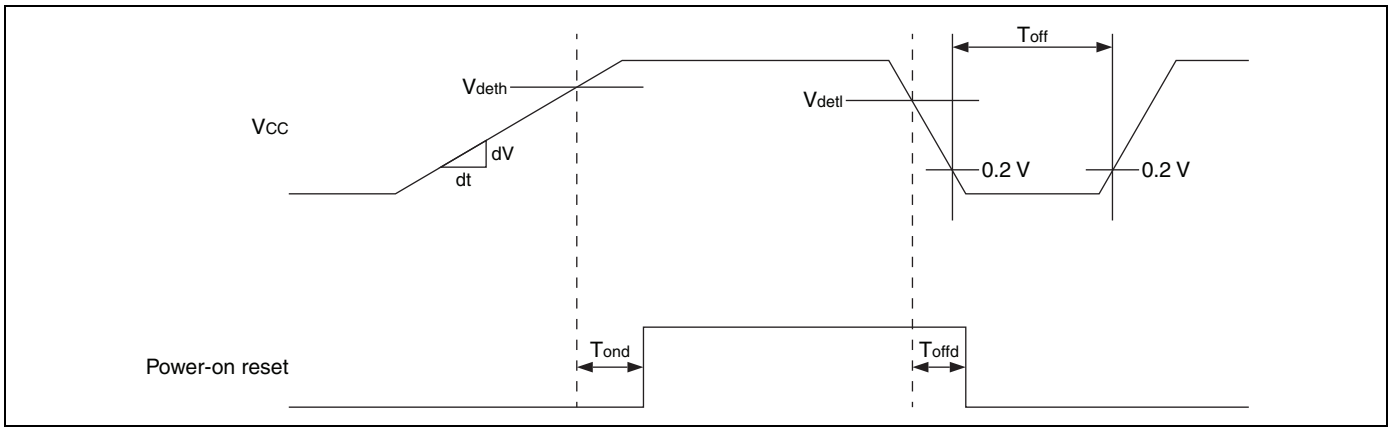
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*6		
Power supply current*7	I_{CC}	V_{CC} (External clock operation)	F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	4.2	6.8	mA	Except during Flash memory programming and erasing
				—	9.3	14.7	mA	During Flash memory programming and erasing
				—	6	10	mA	At A/D conversion
	I_{CCS}		F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	1.7	3	mA	
	I_{CCL}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25 °C	—	35	60	µA	
	I_{CCLS}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25 °C	—	2	7	µA	
	I_{CCT}		F_{CL} = 32 kHz Watch mode Main stop mode T_A = +25 °C	—	1	6	µA	
	$I_{CCMCRPLL}$	V_{CC}	F_{MCRPLL} = 16 MHz F_{MP} = 16 MHz Main CR PLL clock mode (multiplied by 4)	—	4.3	7.7	mA	
	I_{CCMPLL}		F_{MPLL} = 16 MHz F_{MP} = 16 MHz Main PLL clock mode (multiplied by 4)	—	4.1	7	mA	
	I_{CCMCR}		F_{CRH} = 4 MHz F_{MP} = 4 MHz Main CR clock mode	—	1.5	3	mA	
	I_{CCSCR}		Sub-CR clock mode (divided by 2) T_A = +25 °C	—	50	100	µA	

(Continued)

18.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply rising time	dV/dt	V_{CC}	0.1	—	—	V/ms	
Power supply cutoff time	T_{off}		1	—	—	ms	
Reset release voltage	V_{deth}		1.44	1.60	1.76	V	At voltage rise
Reset detection voltage	V_{detl}		1.39	1.55	1.71	V	At voltage fall
Reset release delay time	T_{ond}		—	—	10	ms	dV/dt ≥ 0.1 mV/µs
Reset detection delay time	T_{offd}		—	—	0.4	ms	dV/dt ≥ –0.04 mV/µs



18.4.6 LIN-UART Timing

*Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register : SCES bit = 0, ECCR register : SCDE bit = 0)

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3–t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 10	—	ns
SCK↓ → SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK↑	t_{IVSHE}	SCK, SIN		30	—	ns
SCK↑ → valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is disabled*2.*
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 0)

(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↑ → SOT delay time	t_{SHOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 – t_R	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK		t_{MCLK}*3 + 10	—	ns
SCK↑ → SOT delay time	t_{SHOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK↓	t_{IVSLE}	SCK, SIN		30	—	ns
SCK↓→ valid SIN hold time	t_{SLIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.

*Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2.*
(ESCR register : SCES bit = 1, ECCR register : SCDE bit = 1)

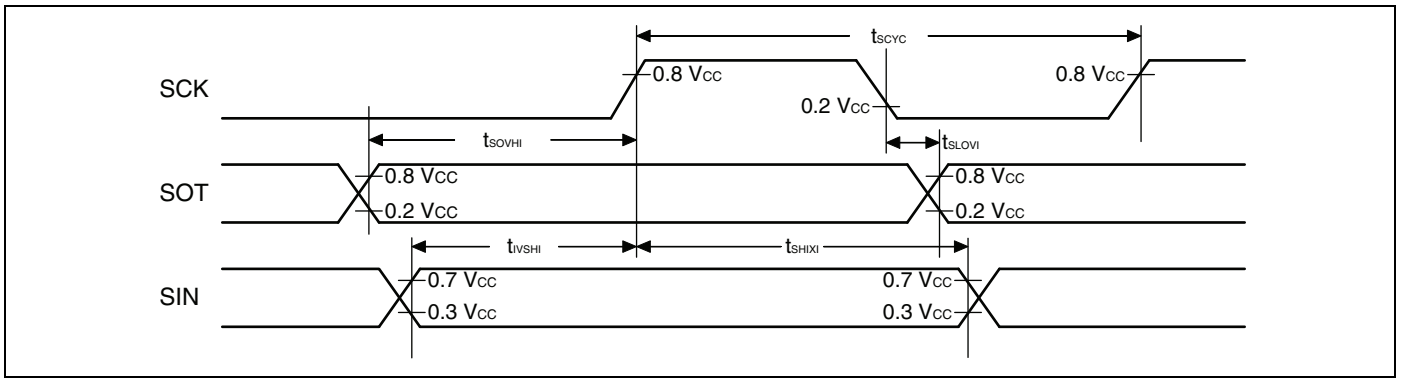
(V_{CC} = 3.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK↓ → SOT delay time	t_{SLOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK↑ → valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK↑delay time	t_{SOVHI}	SCK, SOT		3t_{MCLK}*3 – 70	—	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “18.4.2. Source Clock/Machine Clock” for t_{MCLK}.



18.6 Flash Memory Program/Erase Characteristics

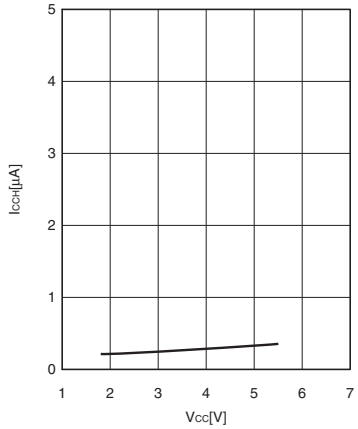
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.3*1	1.6*2	s	The time of writing “0x00” prior to erasure is excluded.
Sector erase time (32 Kbyte sector)	—	0.6*1	3.1*2	s	The time of writing “0x00” prior to erasure is excluded.
Byte writing time	—	17	272	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	1.8	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85 °C Number of program/erase cycles: 1000 or below
	10*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 1001 to 10000 inclusive
	5*3	—	—		Average T_A = +85 °C Number of program/erase cycles: 10001 or above

*1: V_{CC} = 5.5 V, T_A = +25 °C, 0 cycle

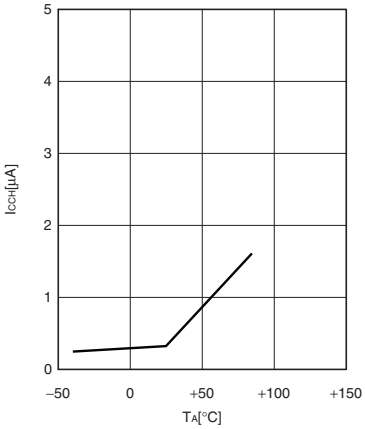
*2: V_{CC} = 1.8 V, T_A = +85 °C, 100000 cycles

*3: These values were converted from the result of a technology reliability assessment. (These values were converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85 °C.)

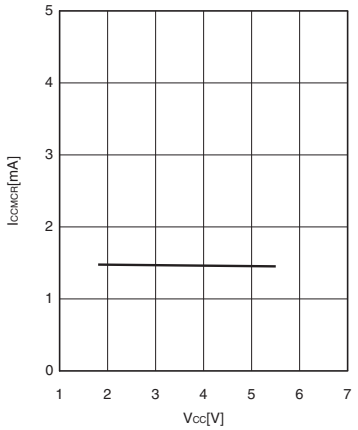
$I_{CCH} - V_{CC}$
T_A = +25 °C, F_{MPL} = (stop)
Substop mode with the external clock stopping



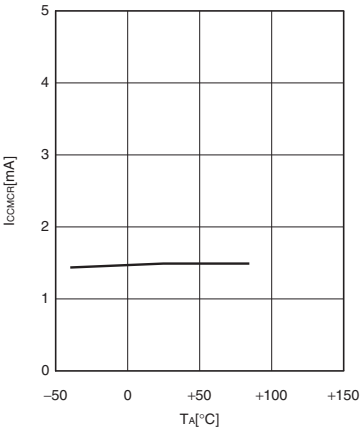
$I_{CCH} - T_A$
V_{CC} = 3.3 V, F_{MPL} = (stop)
Substop mode with the external clock stopping



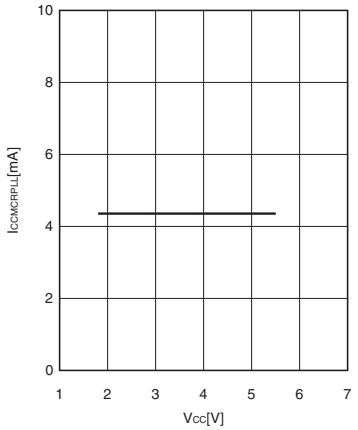
$I_{CCMCR} - V_{CC}$
T_A = +25 °C, F_{MP} = 4 MHz (no division)
Main CR clock mode



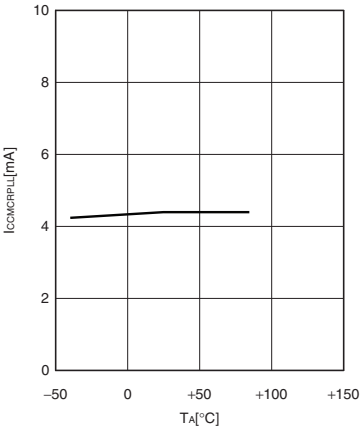
$I_{CCMCR} - T_A$
V_{CC} = 3.3 V, F_{MP} = 4 MHz (no division)
Main CR clock mode



$I_{CCMCRPLL} - V_{CC}$
T_A = +25 °C, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode



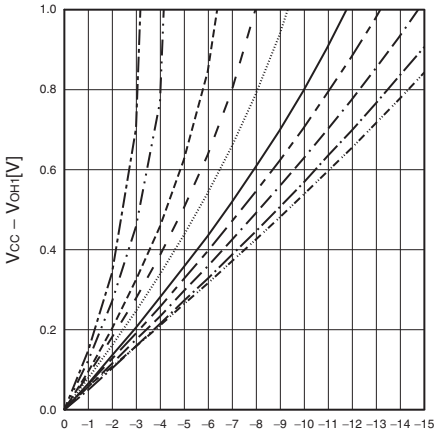
$I_{CCMCRPLL} - T_A$
V_{CC} = 3.3 V, F_{MP} = 16 MHz (PLL multiplication rate: 4)
Main CR PLL clock mode



(Continued)

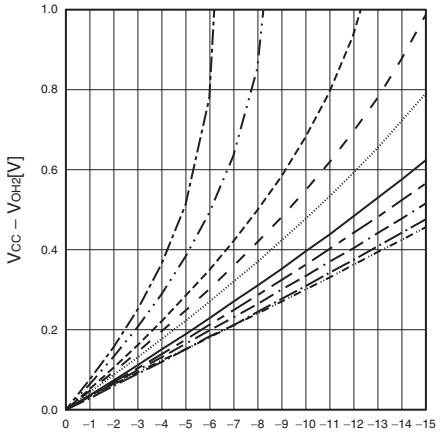
Output voltage characteristics

$(V_{CC} - V_{OH1}) - I_{OH}$
$T_A = +25\ °C$



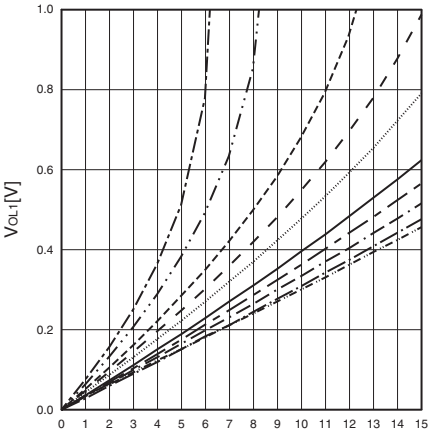
VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V

$(V_{CC} - V_{OH2}) - I_{OH}$
$T_A = +25\ °C$



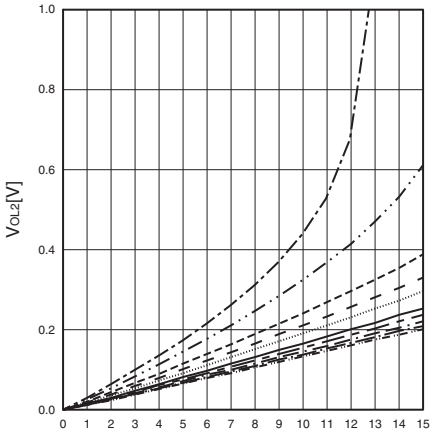
VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V

$V_{OL1} - I_{OL}$
$T_A = +25\ °C$



VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V

$V_{OL2} - I_{OL}$
$T_A = +25\ °C$



VCC = 1.8 V
VCC = 2.0 V
VCC = 2.4 V
VCC = 2.7 V
VCC = 3.0 V
VCC = 3.6 V
VCC = 4.0 V
VCC = 4.5 V
VCC = 5.0 V
VCC = 5.5 V